A 7GHz Fractional-N Sampling PLL with Differential Self-Normalized Sampling PD Achieving 83.0fs Integrated Jitter

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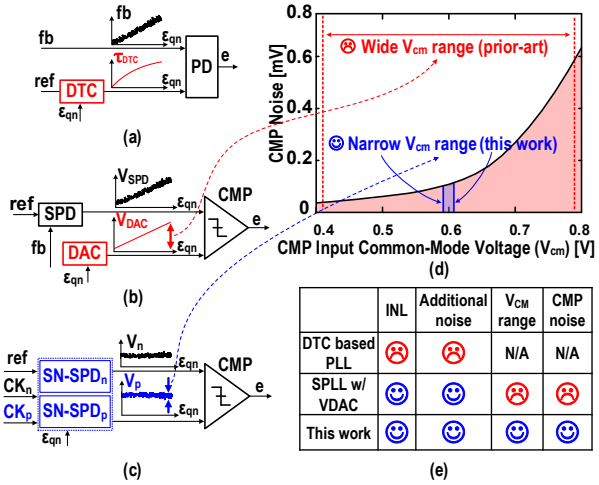
***Abstract*—This work presents a 7GHz sampling PLL using a differential self-normalized SPD, which suppresses fractional spur through the differential structure and reduces integrated jitter by fixing the comparator's common-mode voltage. Fabricated in 65nm CMOS, it achieves 68.5fs integrated jitter in integer-N mode, and 83.0fs integrated jitter with the worst-case fractional spur of -61.5dBc in fractional-N mode. With 100MHz reference and 15.6mW power consumption it achieves -239.7dB FoM$_{ref}$.**

***Keywords*—Fractional-N Synthesizer, Sampling PD, VCO, Digital PLL, 5G.**

I. Introduction

Applications such as high-data-rate communication in advanced wireless transceivers and high-precision ranging in modern radar systems demand low-jitter, low-spur fractional-N PLLs. To meet these requirements, conventional PLLs utilize a digital-to-time converter (DTC) to suppress the quantization noise (QN) of the delta-sigma modulator (DSM) as shown in Fig. 1 (a). However, such DTC-based PLLs often suffer from degraded spur performance due to the integral nonlinearity (INL) of the DTC. A common technique to improve the fractional spur of PLLs is dithering [1], which, however, does not inherently eliminate the DTC nonlinearity but rather spreads the spur energy. While dithering can reduce the fractional spur level, it typically comes at the cost of degraded in-band phase noise. Another approach is digital predistortion (DPD) [2-5], which can effectively compensate the DTC INL without penalizing the in-band phase noise of the PLL. Nevertheless, DPD requires substantial digital resources, thereby degrading the intrinsic power–jitter trade-off of the PLL. In recent years, analog methods have also been proposed to compensate DTC INL for an improved power-jitter trade-off. For instance, one work leverages the inherently opposite INL characteristics of differential DTCs for mutual cancellation [6], whereas another introduces tunable resistors to generate a reverse-concavity nonlinearity for INL compensation [7-8]. However, since QN cancellation is performed at the DTC before the PD, the noise generated during the DTC's delay generation cannot be suppressed by the PD gain, thereby degrading the phase noise. In some analog PLLs, benefiting from the large gain of the PD, the in-band phase noise can be significantly suppressed [9-10]. While in digital PLLs, by transferring QN cancellation from the phase domain to the voltage domain [11], these issues can be alleviated. As shown in Fig. 1 (b), the comparator inputs V_{SPD} and V_{DAC} are proportional to the DSM QN. In other words, the phase-domain QN is sampled into the voltage domain. The sampling PD (SPD) exhibits a large sampling gain, which allows the noise generated by the subsequent QN cancellation to be effectively suppressed, leading to lower PLL in-band phase noise. This enables the PLL to achieve improved jitter and spur performance. Yet, because V_{SPD} and V_{DAC} vary with QN, the comparator input common-mode voltage (V_{CM}) can be occasionally raised to levels where the comparator noise is significantly degraded, adding extra noise to the PLL as shown in Fig. 1 (d).

To simultaneously achieve low jitter and low spur without excessive digital resource overhead or added comparator noise, this work presents a sampling PLL based on a differential self-normalized sampling phase detector (SN-SPD). As shown in Fig. 1 (c), the output voltages of the SN-SPD, V_p and V_n, are kept constant regardless of quantization error (ε_{qn}), ensuring that the comparator always operates at a favorable V_{CM} for low noise. The proposed design achieves a worst-case fractional spur of –61.5dBc and an integrated jitter of 83.0fs. Fig. 1 (e) shows a comparison between prior art and the proposed design.



	INL	Additional noise	V_{CM} range	CMP noise
DTC based PLL	☹	☹	N/A	N/A
SPLL w/ VDAC	☺	☺	☹	☹
This work	☺	☺	☺	☺

Fig. 1. (a) DTC based PLL, (b) SPLL with DAC-based QN cancelation [11], (c) proposed SPLL with differential SN-SPD, (d) comparator noise vs. input common-mode voltage, (e) comparison of QN cancellation schemes between prior work and the proposed SPLL.

II. Proposed Sampling PLL with Self-Normalized SPD

A. Differential Self-Normalized SPD

The architecture of the proposed SN-SPD is shown in Fig. 2 (a). CK_p and CK_n control two PMOS switches to charge the bottom capacitors C_p and C_n, generating the output voltages V_p and V_n, respectively. CK_p and CK_n are derived from the reference and feedback signals, and thus encode the phase difference information between them. C_p and C_n are implemented as capacitor banks controlled by D_p and D_n,

which are proportional to ε_{qn}. As a result, V_p and V_n capture the phase information between the reference and feedback signals, and settle to a constant voltage when the PLL is locked. V_p and V_n are then fed into a 1-bit comparator to generate the phase error code e[k]. Unlike conventional DTC-based approaches, no MOS devices are actively charging or discharging the capacitors during the comparison, thereby reducing current noise. In addition, benefiting from the differential architecture, even-order nonlinearities are inherently canceled.

The operation of the SN-SPD can be simplified to the form shown in Fig. 2(b). Two matched branches (ref, CK_p/CK_n) charge variable capacitors C_p/C_n with a constant current I. With T_p=m+ε_{qn} and T_n=m-ε_{qn} (m=1.5), and C_p/C_n scaled accordingly, V_p/V_n settle to constant independent of ε_{qn}. The differential architecture suppresses INL without DPD, while high sampling gain and a low, well-controlled V_{CM} reduce in-band phase noise and comparator-noise penalty versus [6].

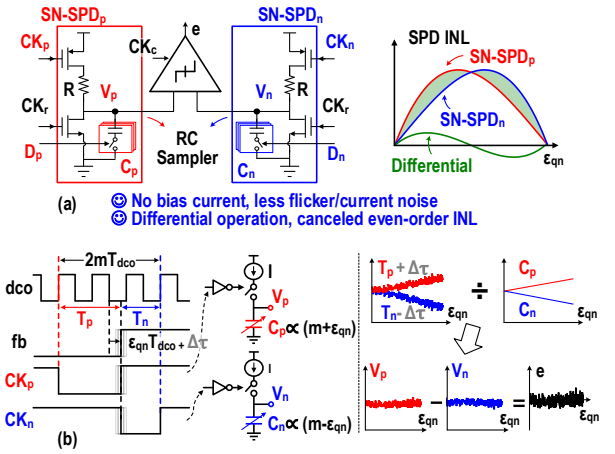


Fig. 2. Differential SN-SPD (a) circuit implementation, (b) conceptual operation.

B. Time-Domain Operation of the SN-SPD

The detailed operation of the proposed SN-SPD is illustrated in Fig. 3. The signals CK_p and CK_n, which control the charging of C_p and C_n, are derived from reference clock (ref), DCO clock (dco), and feedback clock (fb), with the implementation illustrated in Fig. 4 (bottom left). Signal CK_p is set to 0 at the first DCO rising edge after the rising edge of fb, and set to 1 at the rising edge of ref. Similarly, CK_n is set to 0 at the rising edge of ref, and set to 1 at the (2m+1)-th DCO rising edge after detecting the rising edge of fb. As shown in Fig. 2 (top), when CK_p and CK_n are low, the supply charges the corresponding capacitors C_p and C_n through a fixed resistor R, with the total charging time fixed at $2m \cdot T_{dco}$:

$$T_p + T_n = 2m \cdot T_{dco} \quad (1)$$

Where T_{dco} is the DCO period. The capacitance values C_p and C_n are controlled by the digital control words D_p and D_n, which are computed from the ε_{qn}. This allows C_p and C_n to scale proportionally with the charging times T_p and T_n. As shown in Fig. 4 (top) a mash1-1 DSM is employed in this work leading to $\varepsilon_{qn} \in [-1, 1]$. When $\varepsilon_{qn} > 0$, the charging time of C_p (T_p) becomes larger than that of C_n (T_n). To match this condition, the slope-generation block produces the corresponding digital control words D_p and D_n such that the capacitance of C_p is set larger than that of C_n, ensuring that the output voltages V_p and V_n remain constant after charging. Signal CK_c triggers the comparator to compare its inputs V_p and V_n, as shown in Fig. 4 (bottom left), where CK_c is derived by retiming CK_n with two DCO cycles. After each phase comparison between ref and fb, the discharge pulse CK_r, triggered by the falling edge of ref (as shown in Fig. 4), controls a NMOS switch that is shunted to ground switch to discharge C_p and C_n, thereby resetting the operating state of the SN-SPD. The tunable capacitors C_p and C_n are implemented as two-stage segmented capacitor banks. The coarse bank is a 64-unit thermometric array with a nominal resolution of ~25fF, while the fine bank is a 7-bit binary array with a nominal resolution of ~0.36fF. The fine bank can cover twice the resolution step of the coarse bank, which is required to cover one LSB of the coarse bank with enough margin. A fixed 200Ω resistor, instead of a PMOS current source, is used to charge C_p and C_n, eliminating the need for bias current and thereby reducing flicker noise to achieve lower overall noise. This configuration provides an equivalent DTC range of 330ps and a resolution of 74fs, which covers twice the DCO period ($2T_{dco}$= 285ps) with enough margin.

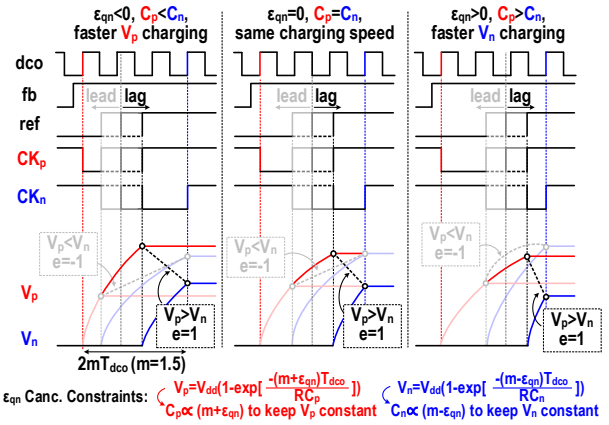


Fig. 3. Time domain waveforms of the key signals in the SN-SPD.

C. Control Word Generation and LMS-Based Calibration of the SN-SPD

Fig. 4 (bottom right) illustrates the generation of the control words D_p and D_n. First, the PLL frequency control word (FCW) is processed by a second-order DSM to generate ε_{qn}. The quantization error ε_{qn} together with the phase error e[k] are then fed into the slope-control block to calculate the capacitor control words D_p and D_n. Within the slope-control block, a least-mean-square (LMS) calibrator is employed to calibrate the digital-to-time conversion gain (K_{DTC}) of SN-SPD. Since both branches share the same supply, the voltage gradually drops while charging C_p, causing the subsequent charging of C_n to occur at a slightly lower supply voltage, which results in a mismatch between V_p and V_n. To address this, another LMS calibrator based on the correlation between ε_{qn} and e[k] is employed to calibrate the P and N branch gain mismatch (K_{mis}). Taking the K_{mis} into consideration, the digital-to-time conversion gains of the P and N branches are corrected to (2) and The capacitor control words are then generated as (3) , where D_{ofst} = $m \cdot K_{DTC}$ corresponds to the delay when ε_{qn}=0.

$$K_p = K_{DTC} - K_{mis}\ ,\ K_n = K_{DTC} + K_{mis} \quad (2)$$

$$D_p = D_{ofst} + K_p \cdot \varepsilon_{qn}\ ,\ D_n = D_{ofst} - K_n \cdot \varepsilon_{qn} \quad (3)$$

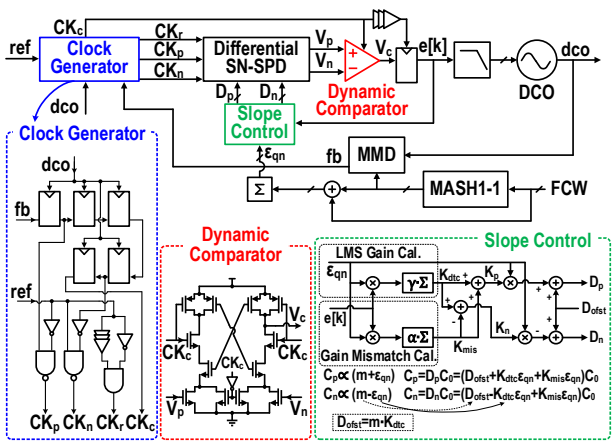


Fig. 4. Implementation of the fractional SPLL based on differential SN-SPD with the calibration on SN-SPD mismatch.

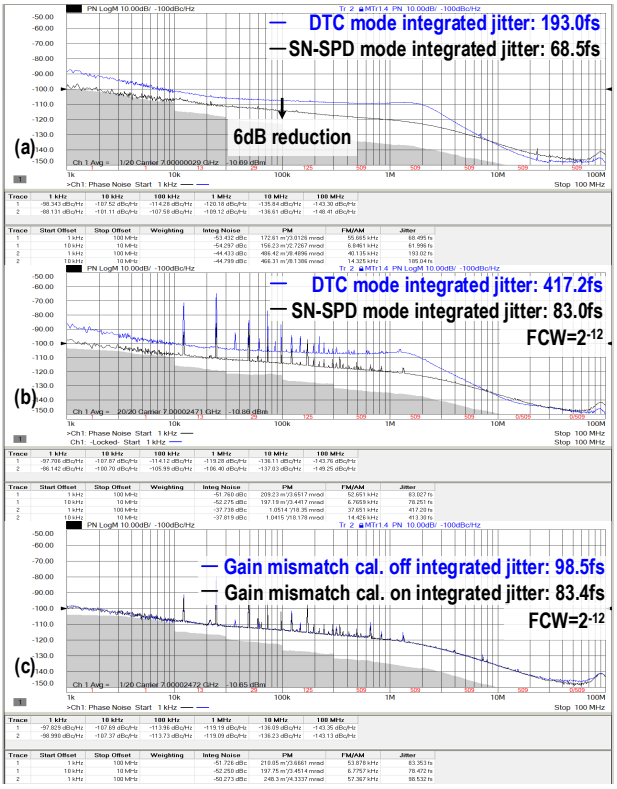


Fig. 5. Measured PLL phase noise: (a) integer-N, DTC vs. SN-SPD, (b) fractional-N, DTC vs. SN-SPD, (c) fractional-N, SN-SPD with gain mismatch calibration ON/OFF.

III. Measurements

Fig. 5 (a) and (b) shows the measured phase noise of the proposed PLL in both DTC mode and SN-SPD mode. In DTC mode, the integrated jitter becomes 193.0fs in integer-N mode and 417.2fs in fractional-N mode. By contrast, owing to the voltage-domain operation and the constantly low comparator V_{CM}, the proposed PLL in SN-SPD mode achieves an integrated jitter of 68.5fs over a 1kHz–100MHz integration bandwidth in integer-N mode, and a worst-case integrated jitter of 83.0fs in fractional-N mode near the integer channel, where the FCW is 2^{-12} corresponding to a fractional frequency of 24.4kHz. The improvements observed in SN-SPD mode over DTC mode can be attributed to the difference in phase-detecting schemes: with the proposed SN-SPD, the high differential sampling gain enables effective suppression of the PLL's in-band phase noise. In contrast, in DTC mode, an additional inverter stage is needed between slope-generation stage and the phase detector; the slope-dependent operation of this inverter aggravates INL of the DTC, thereby introducing more fractional spurs into the PLL. Fig. 5 (c) shows that gain mismatch calibration at FCW=2^{-12} reduces jitter from 98.5fs to 83.4fs, confirming that gain-mismatch calibration further improves the near-integer fractional-N jitter by mitigating the P/N-branch mismatch.

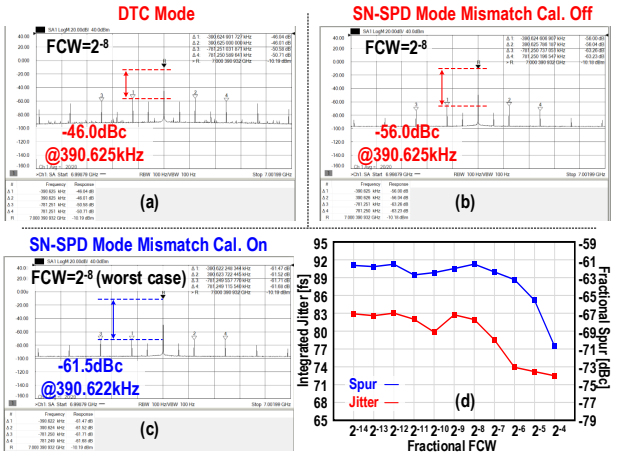
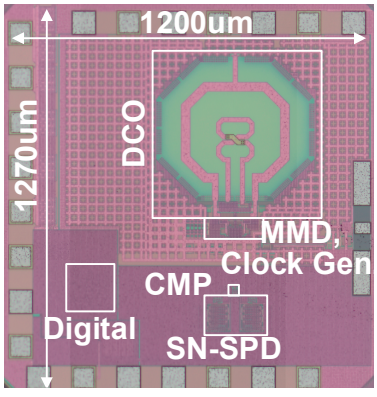


Fig. 6. Measured PLL fractional spur: (a) DTC mode, (b) SN-SPD mode before mismatch calibration, (c) SN-SPD mode after mismatch calibration; (d) fractional spur and integrated jitter versus different fractional channels in SN-SPD mode after mismatch calibration.

Fig. 6 shows the measured fractional spur results. Under the same conditions, the DTC mode exhibits a fractional spur of –46.0dBc. In SN-SPD mode, the proposed PLL achieves a –56.0dBc fractional spur when gain-mismatch calibration is disabled, which is further improved to –61.5dBc with gain mismatch calibration enabled, at an FCW of 2^{-8} which corresponding to a fractional frequency of 390.625kHz. Thanks to the gain-mismatch calibration, the additional spur degradation arising from the slope mismatch between the two differential branches can be effectively suppressed.



Block	Power [mW]
DCO&MMD	14.58
SN-SPD&CMP	0.69
Digital	0.36
Total	15.63

Fig. 7. Die micrograph and power breakdown.

As shown in Fig. 7, this work is implemented in 65nm CMOS process and occupies an active area of 0.3mm². Under 1V supply, the PLL power consumption is 15.6mW, of which the DCO & MMD consume 14.58mW, the SN-SPD & comparator consume 0.69mW, and the digital circuitry consumes 0.36mW.

TABLE I. COMPARISON TABLE WITH PRIOR-ART FRACTIONAL-N PLLS

	This Work	[11] Y. Shin ISSCC'24	[7] M. Rossoni JSSC'25	[8] D. Fagotti ISSCC'26	[1] S. Dartizio JSSC'23	[6] D. Xu JSSC'25	[2] M. Chae JSSC'25	[3] S. Jang JSSC'24
Process [nm]	**65**	40	28	28	28	65	40	40
Technique	**Diff. SN-SPD**	NL Replication VDAC	RCVS-DTC	SI RCVS-DTC	FCW Dither ICS-DTC	Fractional Divider PD-DTC	QEC-BBPD+DPD DTC	RLS-DPD DTC
w/ DTC INL DPD	**No**	No	No	No	No	No	Yes	Yes
Reference [MHz]	**100**	150	250	150	250	100	100	100
Output Freq. [GHz]	**6.5~7.5**	10.4~11.8	8.75~10.25	8.75~10.25	9.25~10.5	6.5~7.5	10~11.5	6.4~8.2
Fractional Spur [dBc]	**-61.5**	-65	-63.4	-64.3	-71.9	-62.1	-62.5	-68
Integrated Jitter [fs]	**83.0**	76	57.3	59.6	76.7	143.7	65	88
Integration Range [Hz]	**1k~100M**	10k~100M	1k~100M	1k~100M	10k~100M	10k~10M	1k~100M	1k~100M
Reference Spur [dBc]	**-63.3**	-67	-69.4	-	-70.5	-62.5	-63	-
Power [mW]	**15.6**	15.3	17.5	22.5	17.2	8.89	14.4	15.7
FoM* [dB]	**-249.7**	-250.5	-252.4	-251	-249.9	-247.4	-252.2	-249.1
FoM_{ref}** [dB]	**-239.7**	-238.7	-238.4	-239.2	-235.9	-237.4	-242.2	-239.1
Area [mm^2]	**0.3**	0.17	0.21	0.28	0.33	0.23	0.12	0.12

***FoM=10log((power/1mW)*(jitter/1s)^2) **FoM=10log((power/1mW)*(jitter/1s)^2)+10log(f_{ref}/10MHz)**

This work achieves an FoM of –249.7dB and an FoM_{ref} of –239.7dB. Table I. summarizes the performance of recent low-jitter, low-spur PLLs. Among DPLLs without DTC linearity DPD, this work achieves the lowest FoM_{ref}.

IV. CONCLUSION

This work presents a low-jitter fractional-N sampling PLL based on a differential SN-SPD. By fixing the comparator input common-mode voltage, the proposed SN-SPD ensures low comparator noise and enables improved in-band phase noise performance. In addition, the differential architecture inherently cancels even-order nonlinearities, effectively suppressing INL without requiring DPD. Fabricated in 65nm CMOS, the prototype achieves 83.0fs integrated jitter with a worst-case fractional spur of −61.5dBc in fractional-N mode. With a 100MHz reference and 15.6mW power consumption, the proposed PLL achieves a FoM_{ref} of −239.7dB, demonstrating its effectiveness for low-noise and low-spur applications.

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