Fabrication of Hybrid Channel CFET Stack by Innovative Wafer-to-Wafer Bonding and Nanosheet Patterning

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***Abstract*—We have investigated the fabrication of complementary field-effect-transistor (CFET) stacks using wafer-to-wafer direct bonding. We demonstrate the successful fabrication and patterning of CFET stacks comprising a Si channel for nFET devices, a SiGe channel for pFET devices and a SiO_2 middle dielectric isolation (MDI) layer. A defect-free 30 nm-thick SiN MDI is achieved through a combination of polishing-based surface preparation and direct bonding, highlighting the robustness of such an integration scheme. Furthermore, Atomic Diffusion Bonding (ADB) of SiO_2-SiO_2 and SiO_2-Si interfaces is explored. Using this approach, a Si-SiO_2-Si stack with ultra-thin SiO_2 layer (5nm) is successfully fabricated, opening new perspectives for the integration of alternative MDI materials for next-generation CFET technologies.**

Keywords*—Complementary field effect transistor (CFET), wafer-to-wafer direct bonding, middle dielectric isolation (MDI), atomic diffusion bonding (ADB).

I. Introduction

Three-dimensional (3D) stacking of transistors is considered as the next technological evolution to meet the Power, Performance, Area (PPA) requirements of future logic applications [1]. Monolithic complementary FET (CFET) technology, which vertically stacks Gate-All-Around (GAA) nFET and pFET devices, has already been demonstrated [2][3]. However, only Si channel-based CFET devices have been reported so far, despite the fact that compressively-strained SiGe channels exhibit higher hole mobility and, consequently, improved pFET performances [4]. In addition, the fabrication of middle dielectric isolation (MDI) via layer transfer prior to any patterning step offers several advantages, including the ability to stack a larger number of nanosheets before strain relaxation, the elimination of complex Ge-rich SiGe replacement processes, flexibility in MDI material and thickness, and compatibility with heterogeneous channel orientation (e.g. (110) for pFET and (100) for nFET) [3]. This work first focuses on the fabrication of a CFET stack using SiO_2-SiO_2 direct wafer bonding, followed by its patterning for active areas definition. SiN-SiN direct wafer bonding is also investigated as a SiN-based MDI facilitates subsequent integration. Finally, SiO_2-SiO_2 and SiO_2-Si pairs using an Atomic Diffusion Bonding (ADB) process are also studied, as this technique potentially allows full flexibility in terms of MDI materials and thicknesses.

II. Fabrication of CFET Stack by Layer Transfer

A. Fabrication of CFET stacks by means of SiO_2-SiO_2 direct wafer bonding

The process flow used for the fabrication of a CFET stack with a SiO_2-based MDI layer is shown in Fig.1. It relies on the parallel fabrication of two stacks on separate SOI substrates. The nFET stack consists in a Si channel layer sandwiched between two SiGe sacrificial layers, meanwhile the pFET comprises a SiGe channel layer enclosed by two Si sacrificial layers. Following direct wafer bonding of these two stacks, the Si carrier substrate and the buried oxide (BOX) of the donor wafer are removed using a Bond-and-Etch-Back (BESOI) process [5].

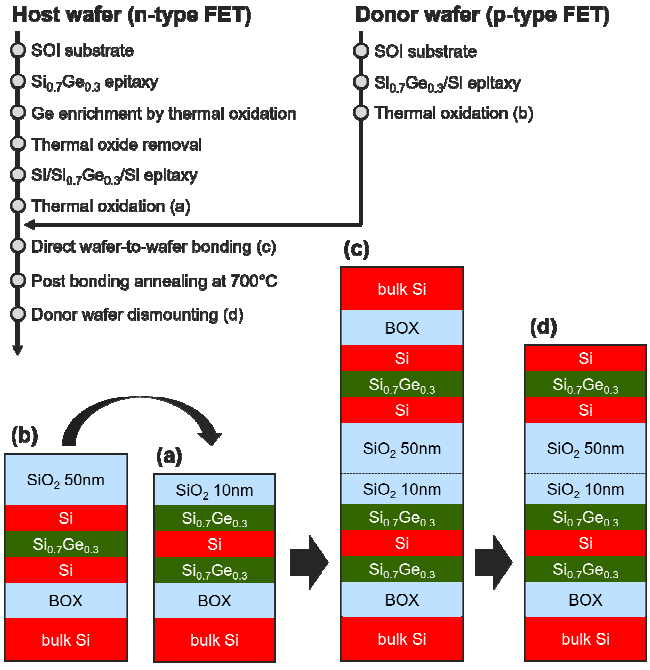

Fig. 1. Main steps of the process flow enabling the fabrication of a CFET stack by wafer-to-wafer bonding.

For the host wafer (Fig.1 (a)), dedicated to nFET, SiGe epitaxy is first performed on a SOI substrate, followed by a Ge enrichment process. This technique enables the translation of a SiGe layer epitaxially grown on a SOI substrate directly onto the BOX [6]. The Ge content of the

resulting SiGe-On-Insulator (SGOI) layer, as measured by X-Ray Diffraction (XRD, not shown), is close to 30%. The subsequently grown thermal oxide is then chemically removed. A Si/$Si_{0.7}Ge_{0.3}$/Si multilayer is epitaxially grown on the SGOI layer, where the $Si_{0.7}Ge_{0.3}$ layer serves as a sacrificial layer. The top Si layer is then fully oxidized at 700 °C in a wet atmosphere to form the SiO_2 bonding layer, which constitutes a part of the SiO_2-based MDI. The resulting thermal oxide is measured by spectroscopic ellipsometry and found to be 10 nm-thick.

As for the donor wafer, the SOI film is first thinned down to the targeted Si sacrificial thickness through a sequence of thermal oxidation followed by wet oxide removal. A $Si_{0.7}Ge_{0.3}$/Si bilayer is then epitaxially grown on top. A controlled portion of the Si cap is then oxidized in a wet ambient at 700 °C to form the bonding oxide, which constitutes the other part of the MDI. The grown oxide is 50 nm-thick, and the initial thickness of the epitaxially grown top Si layer is adjusted such that the remaining unoxidized Si corresponds to the targeted Si sacrificial layer thickness.

As hydrophilic molecular wafer bonding is highly sensitive to surface roughness, both donor and host wafers after the final oxidation process are characterized by atomic force microscopy (AFM) over 1 µm x 1 µm areas. As shown in Fig. 2, the root mean square (RMS) surface roughness is 0.17 nm and 0.15 nm for host and donor stacks respectively, which is low enough to enable high-quality wafer bonding.

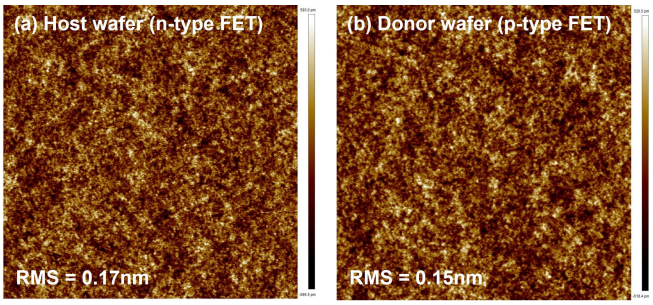

Fig. 2. 1µm × 1µm AFM scans of the host and donor wafers.

The host and donor wafers are chemically cleaned using standard DiO_3 and RCA processes, followed by an ethanolamine surface preparation to enhance adherence [7]. Wafer bonding is performed under vacuum using an EVG® 850 LT bonding equipment. A post-bond annealing is then carried out at 700 °C in a N_2 ambient to strengthen the bonding interface. The bonded wafers are inspected by scanning acoustic microscopy (SAM), confirming a void-free bonding interface (not shown).

The process sequence then includes grinding, selective wet removal of the remaining Si bulk using the BOX layer as convenient etch stop layer, and finally BOX removal via HF chemical etching. Cross-sectional transmission electron microscopy (TEM) images, completed by elemental analysis using energy dispersive X-ray (EDX) spectroscopy, are shown in Fig. 3. Crystalline quality is excellent and Si-SiGe interfaces are sharp. Moreover, the bonding interface is thin enough to be no longer visible at the end of the process flow.

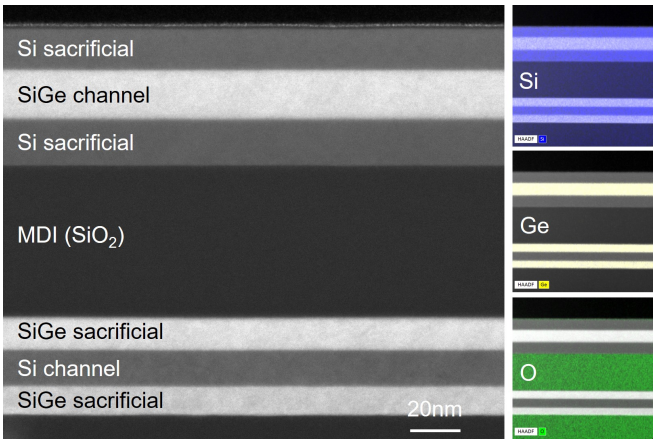

Fig. 3. Cross-sectional TEM image of the fabricated CFET stack with corresponding EDX maps for Si, Ge and O.

B. Fabrication of CFET stacks by means of SiN-SiN direct wafer bonding

The use of a MDI material less sensitive to the multiple dry and wet chemical treatments involved in the CFET flow, such as active patterning, inner spacer etching, and source/drain epitaxy pre-clean, is highly desirable. Furthermore, reducing the thickness of the MDI layer can help minimize the parasitic resistances and capacitances of the device. Accordingly, we investigated the fabrication of a CFET stack following a procedure similar to the one described above, but with a scaled SiN-based MDI layer.

SiN films are deposited at 700 °C on donor and host wafers by means of low-pressure chemical vapor deposition (LPCVD). The SiN film thickness range from 15 nm to 45 nm, targeting MDI thicknesses ranging from 30 nm to 60 nm. AFM measurements indicate a RMS surface roughness of around 0.3 nm, slightly higher than that of thermally-grown SiO_2 films. Standard pre-bonding cleaning processes are applied and wafer bonding is performed under either vacuum or a 40% He atmosphere. Post-bonding annealing is then performed at 600 °C or 700 °C.

As shown in Fig. 4, bonding under vacuum results in numerous and extensive bonding defects, whereas bonding under a 40% He atmosphere produces only limited defects. At first order, neither the SiN thickness nor the annealing temperature significantly affect the bonding quality (SAM images not shown).

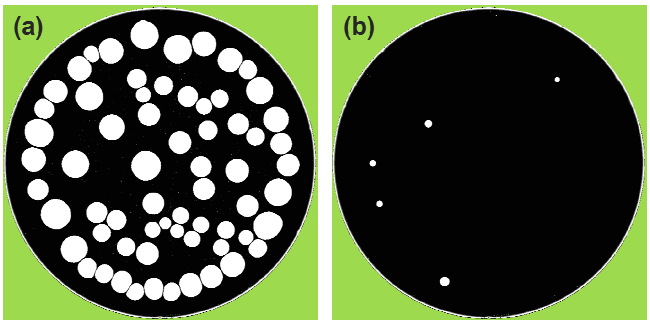

Fig. 4. SAM images after wafer-to-wafer bonding under (a) vaccum and (b) 40% He atmosphere.

Optimization of the bonding process was carried out using 15 nm-thick deposited SiN. A CMP step is introduced

on both donor and host wafers prior to pre-bonding cleaning to reduce surface roughness. The SiN film is thinned from 15 nm down to about 13 nm without degrading the within-wafer uniformity. As shown in the AFM 1 µm × 1 µm scans in Fig. 5, the RMS roughness is successfully reduced to 0.12 nm. Standard cleaning is then carried out followed by bonding under a 40% He atmosphere and post-bonding annealing at 700 °C. SAM observations confirm that void-free bonding was achieved, as shown in Fig. 6.

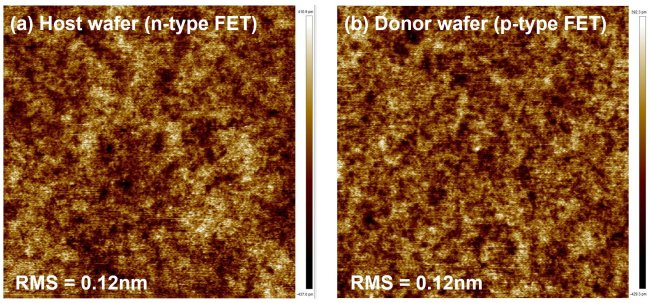

Fig. 5. 1µm × 1µm AFM scans of the host and donor wafers after SiN CMP (before bonding).

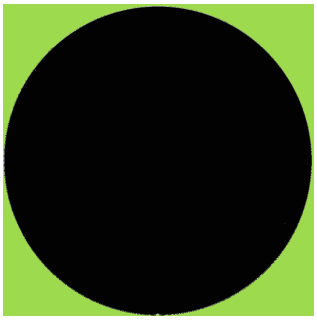

Fig. 6. SAM image of the SiN-SiN bonded CFET stack.

Fig. 7 shows TEM images with EDX mapping of the fabricated stack after donor wafer removal. Si and SiGe layers are of high crystalline quality. Oxygen is detected at the Si-SiN, SiGe-SiN and SiN-SiN bonding interfaces. Oxygen at Si-SiN and SiGe-SiN interfaces is coming from hydrophilic surface preparation prior to SiN LPCVD. The reduced oxygen content at the SiN-SiN bonding interface compared to the Si-SiN and SiGe-SiN interfaces, together with the limited thickness of this interfacial SiN_xO_y, prove that the CMP step prior to bonding does not significantly oxidize the SiN film while it substantially improves its surface roughness.

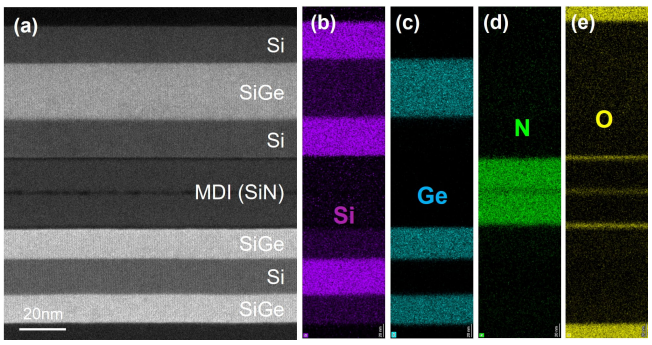

Fig. 7. (a) Cross-sectional TEM image of the CFET stack based on direct SiN-SiN wafer-to-wafer bonding, and (b)(c)(d)(e) corresponding EDX maps for Si, Ge, N and O elements, respectively.

C. *Si-SiO_2 and SiO_2-SiO_2 Atomic Diffusion Bonding for ultimate MDI layer flexibility*

Atomic Diffusion Bonding (ADB) is a covalent direct bonding process. It relies on the in-situ physical vapor deposition (PVD) of an ultrathin (few nm) semiconductor or metallic layer on both wafers. Keeping the deposited surfaces in an ultra-high vacuum environment, dangling bonds allow to create covalent bonds at room temperature when wafers are brought in contact. Assuming that the roughness of both surfaces is low enough, this technique enables the bonding of virtually any materials combination.

As an initial step in the context of CFET stack fabrication, SiO_2//SiO_2 and SiO_2//crystalline-Si ADB with amorphous Si deposition are investigated. The SiO_2 layers are 5nm-thick. The crystalline Si is deoxidized and passivated by silane bonds just prior to bonding [8]. The wafers are bonded using a BC7300 wafer bonding equipment from Canon Anelva. After bonding, an annealing at 700 °C was used to recrystallize the Si/Si bonding interface. Scanning Acoustic Microscopy (SAM) confirm that both bonded pairs are defect-free (Fig. 8). After removal of the donor wafer's Si carrier, the resulting stacks are characterized by TEM (Fig. 9).

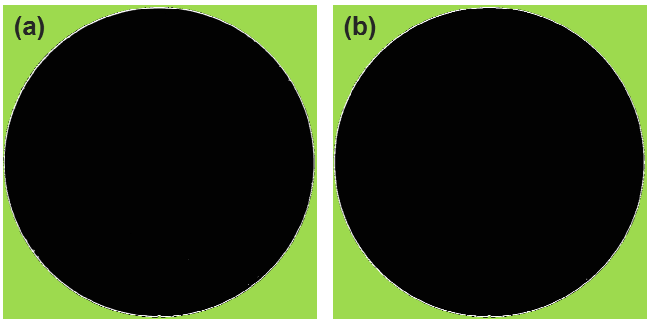

Fig. 8. SAM images of the (a) SiO_2-SiO_2 and (b) SiO_2-cristalline Si bonded wafers.

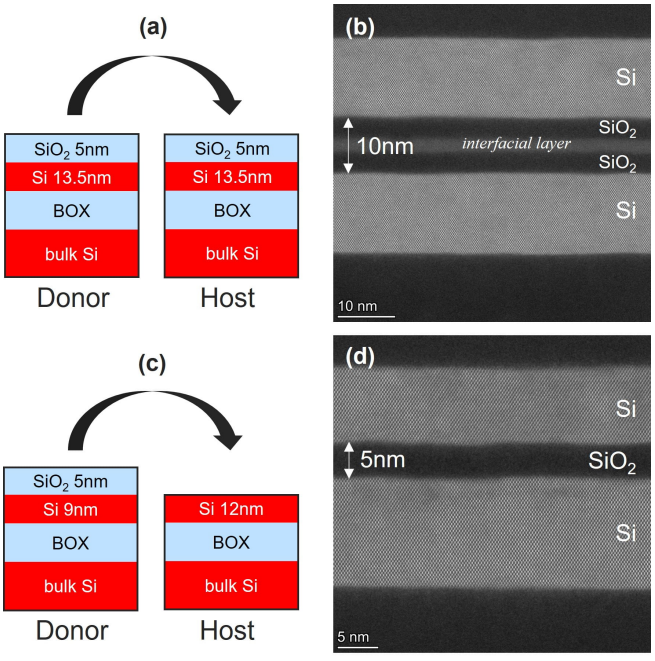

Fig. 9. Schematics and cross-sectional TEM image of SiO_2-SiO_2 ADB (a, b), and SiO_2-crystalline Si ADB (c, d).

As shown in Fig. 9, SiO_2-SiO_2 ADB results in the formation of a ~2.5 nm-thick interfacial layer. Fast Fourier transform (FFT) analysis of this layer (not shown) indicates that it is polycrystalline. In contrast, no interfacial layer is observed for SiO_2//cristalline-Si ADB, demonstrating that the deposited amorphous Si layers on both donor and host wafers are fully recrystallized by the post-bonding annealing (Fig. 10).

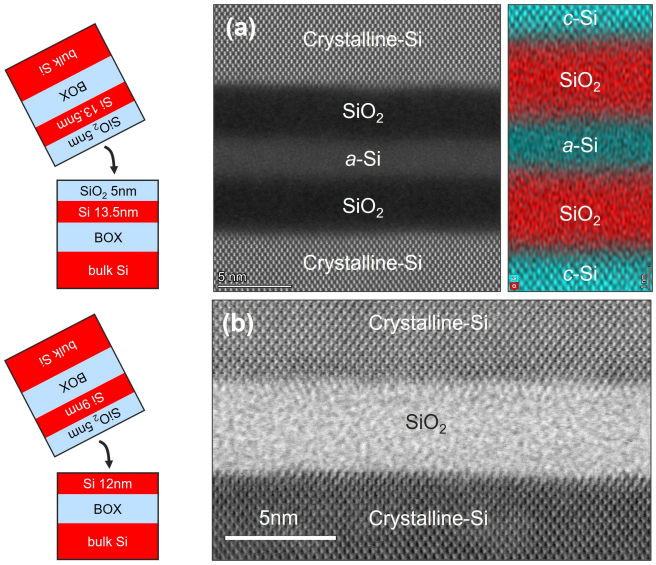

Fig. 10. Schematics and cross-sectional TEM images of (a) SiO_2-SiO_2 ADB and (b) SiO_2-crystalline Si ADB.

III. Active Patterning

The CFET stack featuring a SiO_2-based MDI layer is patterned using deep ultraviolet (DUV) lithography, followed by a three-step fin etch process to accommodate the heterogenous stack. Achieving a straight fin profile with the dielectric film in between the two Si-SiGe multilayers remains challenging.

While Si-SiGe multilayer fins exhibit a straight profile, the MDI layer is slightly curved, as shown in Fig. 11. It should also be noted that the bonding interface is laterally recessed over a few nm, indicating increased sensitivity to etching and/or polymer removal chemistries. Additionally, the landing on the BOX during the last of the three etch steps could be further optimized, as some minor BOX consumption is observed.

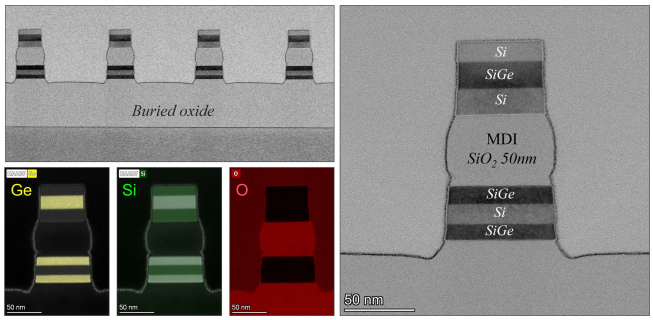

Fig. 11. Cross-sectional TEM images of the SiO_2 MDI CFET stack after fin patterning.

IV. Conclusion

In this work, we demonstrated the successful fabrication and patterning of CFET stacks integrating a SiGe channel for pMOS, a Si channel for nMOS, and SiO_2 MDI via a layer transfer approach. The slight curvature of the SiO_2 MDI can be addressed through further optimization of the etching process. In addition, alternative CFET stacks featuring a scaled SiN MDI were successfully fabricated. We showed that a CMP-based surface preparation combined with wafer-to-wafer direct bonding under a 40% He atmosphere is essential to achieve defect-free layer transfer. Furthermore, for the first time, a CFET-like Si/SiO_2/Si stack with an ultra-thin SiO_2 MDI thickness down to 5 nm was achieved using atomic diffusion bonding. Overall, this versatile layer transfer and bonding strategy represents a significant advancement toward innovative and highly scalable CFET stack technologies.

Acknowledgment

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