Physics-Based Compact Modeling of Parasitic BJT Induced On-BV and Its impact on Inverter Latch-Up Susceptibility in Hybrid CMOS technology

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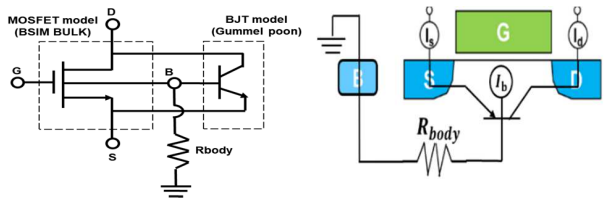
***Abstract*— This work presents a compact model of parasitic BJTs in MOSFETs to characterize the On-BV (On-Breakdown Voltage) phenomenon. The model integrates impact ionization and substrate resistance to accurately simulate the triggering mechanism of parasitic BJTs. When applied to CMOS inverters, it facilitates SPICE-based predictions of latch-up events. The simulation results demonstrate excellent alignment with experimental silicon data in fin-planar hybrid process, establishing a robust and validated methodology for analyzing latch-up phenomena at the device level in CMOS designs.**

Keywords—parasitic BJT, substrate resistance, On-BV, latch-up, hybrid CMOS technology

I. Introduction

Parasitic bipolar-junction transistors (BJTs) that arise unintentionally in bulk-CMOS processes are a well-known source of latch-up. When a high electric-field stress or an increased substrate resistance initiates a positive-feedback loop between the parasitic PNP and NPN devices, impact ionization and a rise in body potential forward-bias the BJT bases, creating a low-impedance VDD–GND path [1]–[3]. In fin-planar hybrid processes the body-well tap is deliberately left unsilicided to keep the silicidation temperature below 650 °C, thereby protecting temperature-sensitive fin structures and suppressing dopant diffusion [4], [5]. This unsilicided tap introduces a large substrate resistance (R_{body}), which lowers the latch-up trigger voltage by facilitating parasitic-BJT activation. Current compact latch-up models are primarily analytic, confined to partially-depleted SOI (PD-SOI), and have never been calibrated against silicon-based bulk data nor integrated into mainstream SPICE simulators [6]–[8]. Consequently, designers lack a physics-based, circuit-level tool for evaluating latch-up risk in fin-planar hybrid technologies. Our contribution embeds a Gummel-Poon BJT model directly into the BSIM-BULK MOSFET framework. The substrate resistance of the unsilicided well-tap is expressed as a layout-dependent parameter, extracted from dedicated test structures and incorporated as a SPICE subcircuit.

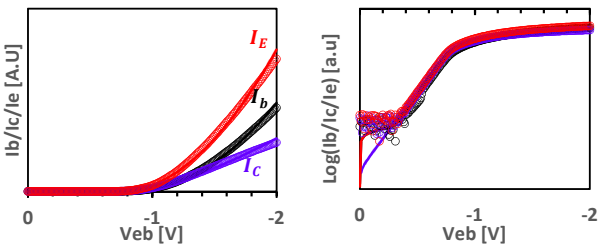
II. Compact Modeling of Parasitic BJT and Substrate Resistance Induced OnBV



(a) (b)

Figure 1. Circuit diagram of an N-type MOSFET showing the parasitic BJT model (a) and the vertical structure (b).

Fig. 1 (a) illustrates the proposed compact model, embedding a Gummel-Poon parasitic BJT within the BSIM-BULK MOSFET core model. The R_{body} component represents the substrate body resistance, which is the effective resistance between body to the well tab. And Fig. 1 (b) depicts the vertical cross-sectional view, highlighting the formation of the unintentional bipolar transistor structure comprising the source (emitter), body(base), and drain (collector) regions. Fig. 2 overlays the measured Gummel curves (symbol) with our SPICE simulation (solid), showing near-perfect agreement in both low and high injection regimes. The experimental data was gathered by negatively sweeping the source of and N-type MOSFET device. The gate bias is applied with sufficient negative (positive in case of P-type MOSFET) bias to minimize the channel current, thereby achieving pure parasitic BJT characteristics.



(a) (b)

Figure 2. Comparison of parasitic BJT measured data (dots) and model (lines) for Ib, Ic, and Ie (a), and the corresponding Gummel plot (b).

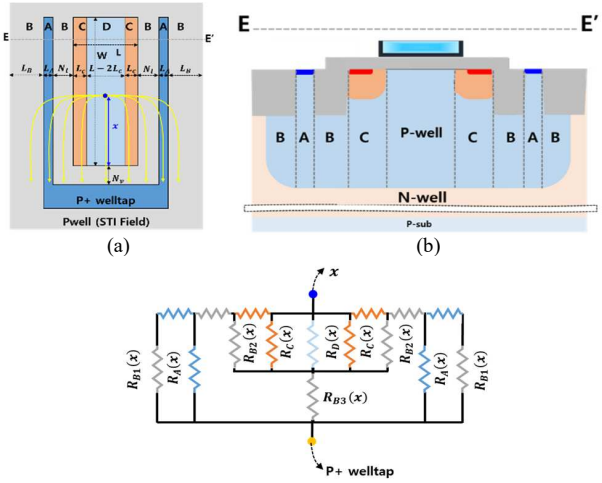
A key innovation lies in introducing R_{body}, a layout-sensitive substrate resistance accounting for three-dimensional current pathways between the body region and well-tap contact. In general, I_{sub} current is formed under poly of transistor and then reaches to the well-tab through in various directions. Therefore, we introduced a method of integrating R_{sh}, which can be seen effectively through each path, against x as follows:

$$R_{body} = \frac{1}{W}\int_0^W R_{eq}(x)\,dx \tag{1}$$

$$\frac{1}{R_{eq}(x)} = \frac{2}{R_A(x)} + \frac{2}{R_{B1}(x)} + \frac{1}{\frac{R_{B2}(x)}{2}\left\|\frac{R_C(x)}{2}\right\| R_D(x) + R_{B3}} \tag{2}$$

where W is the transistor width and $R_{eq}(x)$ is the sheet resistance of body region in terms of position dependent variable x which denotes that arbitrary position distance from location where the I_{sub} is generated under poly gate as

shown in Fig. 3 (a) and its vertical structure is depicted in Fig. 3 (b).



(a) (b) (c)

Figure 3. Substrate current (Isub) flow to the well-tap in the NMOSFET layout (a), its vertical cross-section (b), and the equivalent resistance network from an arbitrary position x to the well tap.

All elementary resistances are linear in the term ($x+N_v$):

$$R_A(x) = R_{shA} \cdot \frac{(x+N_v)}{L_A}, R_{B1}(x) = R_{shB} \cdot \frac{(x+N_v)}{L_B}$$
$$R_{B2}(x) = R_{shB} \cdot \frac{(x+N_v)}{N_l}, R_C(x) = R_{shC} \cdot \frac{(x+N_v)}{L_C} \quad (3)$$
$$R_D(x) = R_{shD} \cdot \frac{(x+N_v)}{(L-2L_c)}, R_{B3} = R_{shB} \cdot \frac{N_v}{(L+2N_l)}$$

Introducing the layout-dependent constants

$$A = \frac{2L_A}{R_{shA}} + \frac{2L_B}{R_{shB}}, S = \frac{2N_l}{R_{shB}} + \frac{2L_c}{R_{shC}} + \frac{L-2L_c}{R_{shD}} \quad (4)$$

The reciprocal of the equivalent resistance becomes

$$\frac{1}{R_{eq(x)}} = \frac{A}{x+N_v} + \frac{1}{\frac{x+N_v}{S} + R_{shB3}} \quad (5)$$

Inverting (4) and defining

$$u = x + N_v, c = R_{shB3} * S, \gamma = A + S, \delta = A * c \quad (6)$$

gives a single rational function

$$R_{eq}(u) = \frac{u^2 + cu}{\gamma u + \delta} \quad (7)$$

Dividing the quadratic numerator by the linear denominator, giving the final compact decomposition:

$$\frac{u^2 + cu}{\gamma u + \delta} = \frac{u}{\gamma} + \frac{cS}{\gamma^2} - \frac{AR_{shB3}^2 S^3}{\gamma^4} \frac{1}{\gamma u + \delta} \quad (8)$$

Substituting $u = x + N_v$ and evaluating the definite integral over [0, W] gives the closed-form expression for the average body resistance:

$$R_{body} = \frac{1}{W}\left[\frac{(W+N_v^2)-N_v^2}{2\gamma} + \frac{cS}{\gamma^2}(W) - \frac{AR_{shB3}^2 S^3}{\gamma^4} \ln\left(\frac{\gamma(W+N_v)+\delta}{\gamma N_v+\delta}\right)\right] \quad (9)$$

In general, EDA (Electronic Design Automation) tools such as LVS (Layout Versus Schematic) and PEX (Parasitic Extraction) cannot extract the substrate-region resistance; however, by incorporating the analytically derived R_{body} equation into a SPICE model, the impact of body resistance for each layout can be evaluated rapidly and accurately through simulation. Moreover, because the model is physically grounded for a variety of well and layout configurations, it can be readily extended to PD-SOI, Fin-FET, and GAA (Gate All Around) technologies in addition to bulk-CMOS processes.

III. ONBV CALIBRATION BASED ON SILICON WITH IMPACT IONIZATION, PARASITIC BJT AND SUBSTRATED RESISTANCE

When R_{body} is large due to the un-silicide well tap, this injection cannot be swiftly drained, causing the local body potential V_{body} to rise. Once V_{body} forward biases the base-emitter junction of the parasitic BJT, the device abruptly transitions to its On-BV state.

To capture this sequence, we reintroduced explicit impact ionization terms into the BSIM-BULK model and coupled them dynamically to the parasitic BJT via R_{body}.

Fig. 5 depict the measured (dot) and simulation result (line) for NMOSFET and PMOSFET of drain voltage versus drain current (a), source current (b), body current (c) and simulation of body potential (d) with various R_{body}, respectively. By parametrically sweeping R_{body}, we confirm that increasing well-tap distance systematically increases the body voltage, directly evidencing how R_{body} governs On-BV characteristics. The R_{body} value calculated from the measured TEG layout for NMOS and PMOS, which were confirmed to be close to the simulation R_{body} value corresponding to the actual silicon characteristics.

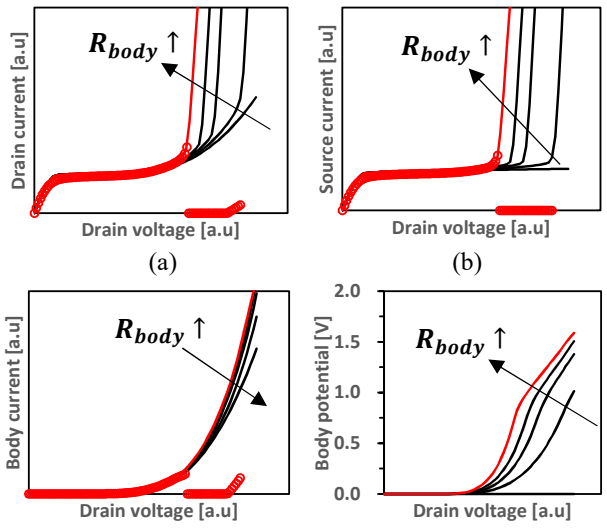


Figure 4. Measured (dots) and simulated (lines) drain-voltage characteristics versus drain (a), source (b), body current (c), and body potential (d) for N-MOSFETs with various R_{body}; extracted results are highlighted in red.

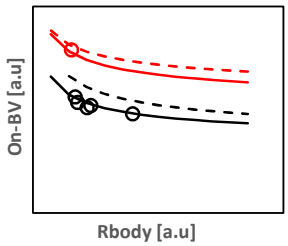


Figure 5. On-BV versus R_{body} for measured (symbols) and simulated results with various well-tap layouts; solid lines use the BJT model, dashed lines omit it (NMOS in black, PMOS in red).

Fig. 6 shows the comparison of the On-BV simulation results versus physically calculated R_{body} and measured silicon data with various well tab distance layout structures as depicted in Fig. 5. The On-BV characteristics are measured by drain voltage at specific source current that exceed some value. The close match confirms that the analytic R_{body} with parasitic BJT model accurately captures the layout dependent characteristics and triggering conditions of parasitic BJT activation.

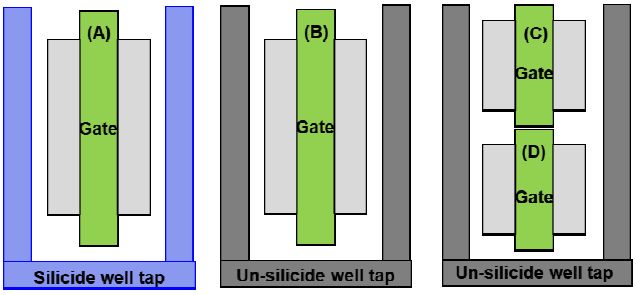


Figure 6. Layout structures used for measurement and R_{body} extraction (Fig. 7 reference): conventional type (A), hybrid CMOS type (B), and two FETs sharing a well tap.

IV. Analysis and Discussion of Inverter-Level Latch-up Simulation

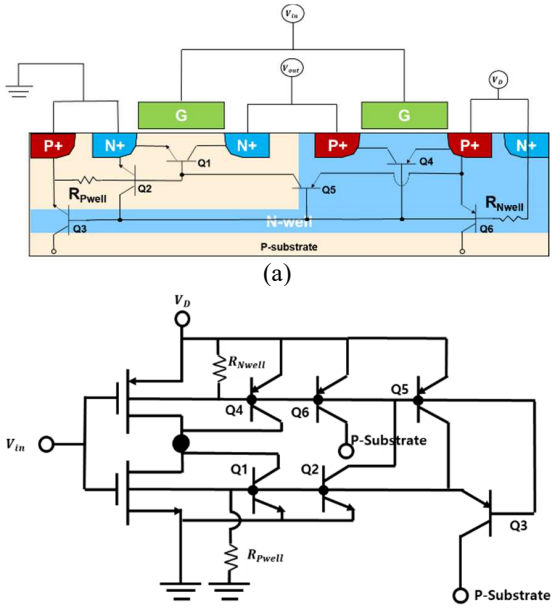


Figure 7. Vertical structure of a conventional inverter (a) and its circuit diagram (b) including all parasitic BJTs.

The full circuit level as shown in Fig. 8 (a), we embed the model into a CMOS inverter with all parasitic BJT formed by well structure. The equivalent circuit for this structure is as shown in Fig. 8 (b), and we will analyze through simulation how the P-well resistance of NMOS (R_{pwell}), N-well resistance of PMOS (R_{nwell}), and parasitic BJTs in this circuit affect the latch-up phenomenon during inverter operation. The characteristics for each BJT were reflected by fitting the Gummel-poon measured in the same well structure as the parasitic BJT modeled at the device level.

BJT	Alpha $\left(\frac{I_C}{I_E}\right)$		Beta $\left(\frac{I_C}{I_B}\right)$	
	Measured	Extracted	Measured	Extracted
Q1	0.69	0.658	2.22	1.924
Q2	0.943	0.928	16.47	12.97
Q3	0.897	0.893	8.664	8.351
Q4	0.556	0.54	1.254	1.175
Q5	0.042	0.049	0.044	0.052
Q6	0.802	0.793	4.054	3.82

TABLE I. Comparison of Alpha and Beta Characteristics for Parasitic BJTs Q1–Q6: Measured versus Extracted Values

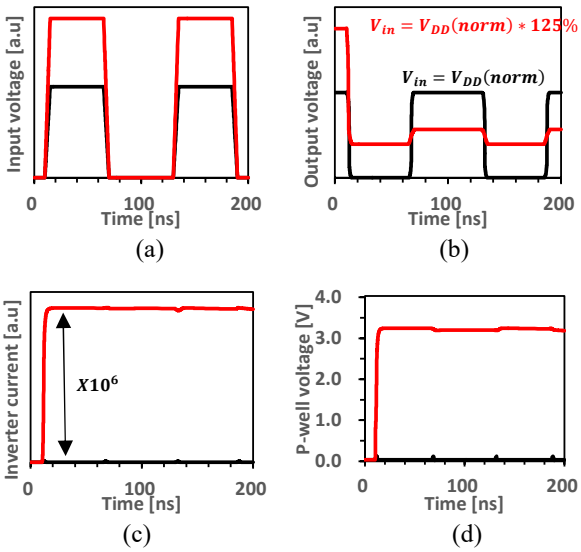


Figure 8. CMOS inverter simulation results: input voltage (a), output voltage (b), inverter current (c), and body potentials for P-well and N-well (d). (N/PMOS width = 1 / 1.68, input frequency = 8 MHz, rise/fall time = 10 ns, Vin = VDD(norm), VDD(norm) × 125 %)

Fig. 9 illustrates the simulation results of an inverter that contains parasitic BJTs. During normal operation, represented by the black curve, the input and output waveforms transition as expected, confirming correct inverter functionality. Conversely, when an unintended high-voltage event such as an ESD surge is applied, the well-body potential forward-biases the parasitic BJTs. The BJTs turn on abruptly, causing a rapid increase in the inverter current that exceeds the nominal current by more than 10^6 times. This current surge becomes even larger as the supply voltage (V_{DD}) is increased.

The latch-up condition is reached when the input and output voltages are equal to half of the supply voltage, i.e., $V_{in} = V_{out} = V_{DD}/2$, where the N-well and P-well body potentials are biased sufficiently to trigger the parasitic BJTs.

These observations underscore the susceptibility of CMOS inverters to latch-up under high-voltage stress and highlight the importance of robust protection strategies in preventing such catastrophic failure modes.

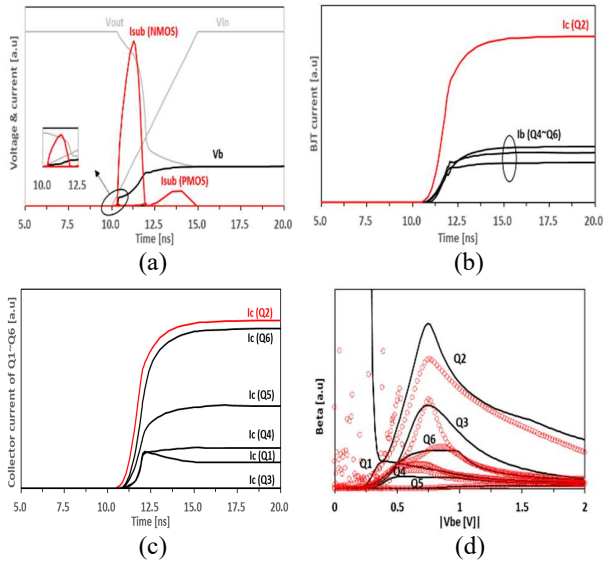


Figure 9. CMOS inverter simulation showing (a) input/output voltages (gray), body potential (black), Isub currents for N/PMOS (red); (b) base currents of Q4-Q6 (black) and collector current of Q2 (red); (c) collector currents of all BJTs, with VDD = VDD (norm) × 125 %; measured (symbols) and simulated (lines) base-emitter voltage versus β for all BJTs.

To investigate the trigger mechanism of latch-up, we analyzed the various circuit elements as shown in Fig. 12, focusing on the instant at which the inverter current exhibits a rapid increase.

When the input signal rises to $V_{in} * 25\%$, both the NMOS and PMOS transistors turn on, causing the output voltage to swing down to approximately $V_{out} * 70\%$. At this moment the I_{sub} is generated primarily by the NMOS device as shown in Fig. 11 (a). This I_{sub} flows through the p-well body resistance, biasing body potential (see Eq. (10)), which initially turns on transistors Q1 and Q2. Because Q2 exhibits a high current gain (β), its collector current rises abruptly. The rising collector node of Q2 is shared with the bases of transistors Q4-Q6, so the collector current of Q2 drives the base currents of Q4–Q6, thereby turning these BJTs on as depicted in Fig. 11 (b). The amplified currents of Q4–Q6 are fed back to the bases of Q1 and Q2, forming a positive-feedback loop that further accelerates the current increase.

After this rapid rise, the current reaches a peak and then settles to a constant value. This behavior originates from the bias of the BJTs entering the high-injection regime. In the high-injection region, phenomena such as the Kirk effect and increased contact resistance effect reduce the amplification efficiency, causing the current gain β to fall below unity as shown in Fig. 11 (d). Consequently, the positive-feedback action is suppressed, and the circuit stabilizes at a steady current.

V. Conclusion

This paper proposes a physics-based compact-modeling framework that augments the conventional BSIM-Bulk MOSFET formulation with the dynamics of parasitic BJTs and a layout-dependent substrate resistance. A closed-form expression for the effective body resistance, R_{body} is derived analytically by solving the three-dimensional current-flow network that links the bulk region to the well-tap contact. The derived R_{body} is then coupled to the impact-ionization model of the BSIM-Bulk device, enabling the model to predict the onset of the On-BV soft-breakdown event that precedes latch-up. Parameter extraction is performed with bulk-CMOS silicon data and agree with measured values. The complete model is realized as a user-defined element in a commercial SPICE simulator, allowing circuit-level simulations of CMOS inverters that faithfully reproduce both device-level soft-breakdown characteristics and the transient excursions of the bulk potential observed in silicon. Simulation results illustrate that increasing the well-tap spacing systematically raises the body potential, thereby reducing the voltage margin for latch-up and accurately capturing the latch-up trigger condition. Compared with conventional BSIM-Bulk models that omit the parasitic BJT, the proposed framework predicts latch-up currents up to six decades larger, providing a reliable quantitative metric for design-margin assessment. Consequently, the presented compact model offers designers an intuitive, silicon-validated tool for early-stage evaluation of latch-up susceptibility, facilitating layout optimization and robust circuit design in scaled fin-planar hybrid CMOS technologies.

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