Field-free Switching Spin-orbit Torque Device with Controllable Switching Polarity for Logic and Memory Applications

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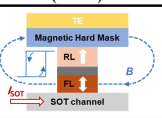
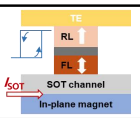
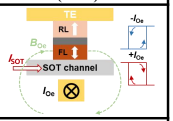
***Abstract*—Spin–orbit torque (SOT) based logic and memory devices with perpendicular magnetic anisotropy (PMA) have attracted significant attention due to their non-volatility, high speed, high density, and energy efficiency. However, the deterministic switching of perpendicular magnetization typically requires an external in-plane magnetic field, which is impractical for applications. Although various strategies have been proposed for field-free switching (FFS), most remain constrained by fixed switching polarity and a lack of operational flexibility. In this work, we propose a CMOS-compatible FFS scheme, termed Oersted-field-assisted (OFA), utilizing the Oersted field generated by currents in metal interconnects to enable controllable switching polarity. Based on the OFA scheme, multi-logic and complementary operations are experimentally implemented in single and dual Hall-dot devices, respectively. Furthermore, due to the programmable polarity, a 5T–4R MRAM cell based on OFA-p-SOT magnetic tunnel junctions (MTJs) is introduced, achieving high write parallelism. Our proposed OFA scheme is promising for efficient computing-in-memory and high-throughput memory applications.**

Keywords—spin-orbit torque, field-free switching, MRAM, high write parallelism, computing-in-memory

I. Introduction

Spin-torque driven logic and memory devices have attracted significant attention, due to their non-volatility, high speed and low power consumption and excellent endurance [1]. For example, the two-terminal magnetic random-access memory (MRAM) driven by spin-transfer torque (STT) has achieved large-scale commercialization in stand-alone and embedded memory applications [2]. However, STT-MRAM suffers from an intrinsic trade-off between switching-speed and device reliability, primarily due to its shared read/write path. As the next-generation technology, spin-orbit torque MRAM (SOT-MRAM) based on perpendicular MTJs (p-MTJs) emerges with fast switching speed, high density and more excellent endurance, due to its decoupling read/write path [3,4]. However, due to the high symmetry of conventional spin-source materials (such as Pt), the spin polarization generated by spin Hall effect lies in plane, and an external in-plane magnetic field is needed to break the symmetry for deterministic SOT switching of perpendicular magnetization [5], which limits the high-density integration of SOT devices.

TABLE I. Comparisons of OFA scheme with typical mass-producible FFS schemes

	Magnetic Hard Mask (MHM)	FM/HM/FM trilayer	Oersted-field-assisted (OFA)
Schematic			
Symmetry-breaking	Stray field	Unconventional SOT	Oersted field
Switching polarity	Fixed	Fixed	Controlled by the polarity of I_{Oe}

To address this issue, various field-free switching (FFS) strategies have been developed, including low crystalline symmetry SOT materials [6], wedge-shaped film [7], STT-assisted SOT [8], magnetic-hard mask (MHM) [9], and interlayer coupling [10,11]. However, these approaches provide a fixed SOT switching polarity, and lack flexibility for logic operations. For example, as shown in Table I, in MHM and interlayer coupling schemes, both of which are compatible with large-scale fabrication, the magnetization of in-plane magnetic layer is fixed, leading to fixed SOT switching behavior.

Here, we overcome this limitation by utilizing the Oersted field generated by currents flowing through metal interconnects, termed the Oersted-field-assisted (OFA) FFS scheme, and propose a novel SOT device based on the OFA scheme (Table I). This scheme is experimentally demonstrated in an OFA Hall-dot device, where the Oersted field is sufficient to electrically control the SOT switching polarity, thereby allowing AND and XNOR logic operations within a single device. Furthermore, in a dual OFA Hall-dot device, we demonstrate simultaneous writing of two dots and complementary logic operation. Finally, we propose a novel 5T–4R memory cell architecture based on OFA p-SOT-MTJs, which enables high write parallelism and significantly improves throughput and operational speed. These results show that the proposed OFA scheme holds potential for field-free and highly flexible operation, supports diverse devices for computing-in-memory (CIM), and offers high write parallelism for advanced memory applications.

II. OFA Hall-dot device

A. Device fabrication and characterization

We first fabricate a micron-sized OFA Hall-dot device on a 2-inch wafer using standard lithography and ion milling, based on a sputtered film stack with PMA: substrate/Ta

(1)/Pt (4)/Co (1.2)/Ta (3) (thickness in nanometer). As illustrated in Fig. 2(a), a 5-μm-diameter Co dot is patterned on a 10-μm-wide Pt channel, a benchmarked spin-source material. To generate the Oersted field B_{Oe}, a Ti (5)/Pt (100) metal wire (30 μm × 10 μm) is fabricated above the Co dot and electrically isolated from the underlying structure by a 60-nm-thick SiO_2 layer. The optical image of the fabricated OFA Hall-dot device is shown in the inset of Fig. 2(b).

The magnetization state of the Co dot is monitored via measuring the anomalous Hall resistance R_{xy}. As shown in Fig. 2(b), the R_{xy}-B_z hysteresis loop shows a clear square switching behavior, indicating strong PMA of the Co dot. The typical SOT switching behavior of fabricated OFA Hall-dot device is observed by applying current pulse I_{SOT} under different external in-plane magnetic field B_x, where the switching polarity is controlled by the direction of B_x (Fig. 2(c)).

B. Oersted-field-assisted field-free switching

To experimentally validate FFS in the OFA Hall-dot device, as shown in Fig. 2(a), we apply an auxiliary current pulse I_{Oe} to generate B_{Oe}, which is synchronized with the SOT current pulse I_{SOT}. As shown in Fig. 2(d), the FFS of magnetization can be observed when I_{Oe} and I_{SOT} are applied simultaneously. In addition, reversing the polarity of I_{Oe} leads to a corresponding reversal of the SOT switching polarity. This confirms that B_{Oe} generated by I_{Oe} effectively plays the same role as B_x for symmetry-breaking.

We then evaluated the roles of I_{Oe} in realizing FFS by comparing the dependence of critical switching current I_c on B_x (Fig. 3(a)) and I_{Oe} (Fig. 3(b)) . While I_c exhibits a modest dependence on B_x, it is significantly reduced by approximately 75% when comparing the case I_{Oe} = 80 mA (B_{Oe} = 5 mT) to the equivalent B_x = 5 mT. This discrepancy can be attributed to a reduction in the strength of PMA resulting from Joule heating induced by I_{Oe}.

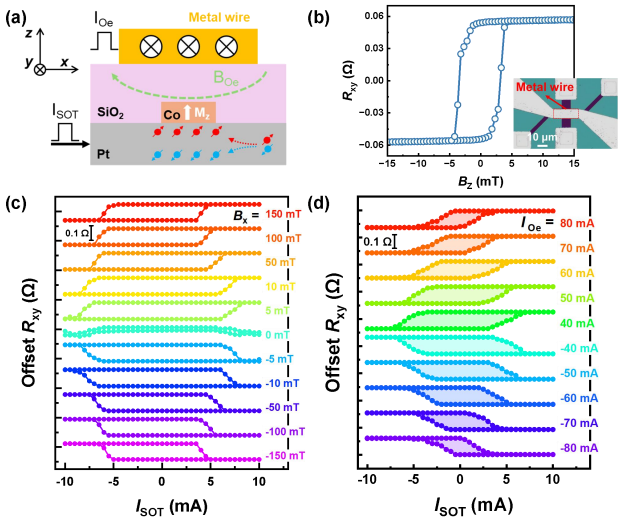


Fig. 2. (a) Schematic of OFA-Hall-dot device. (b) The hysteresis loop of anomalous Hall resistance R_{xy} of OFA Hall-dot device, and the inset is the optical image of the device. (c) The SOT switching loops under applying different external magnetic fields B_x. (d) The FFS SOT switching loops under applying Oersted field B_{Oe} generated by different I_{Oe}.

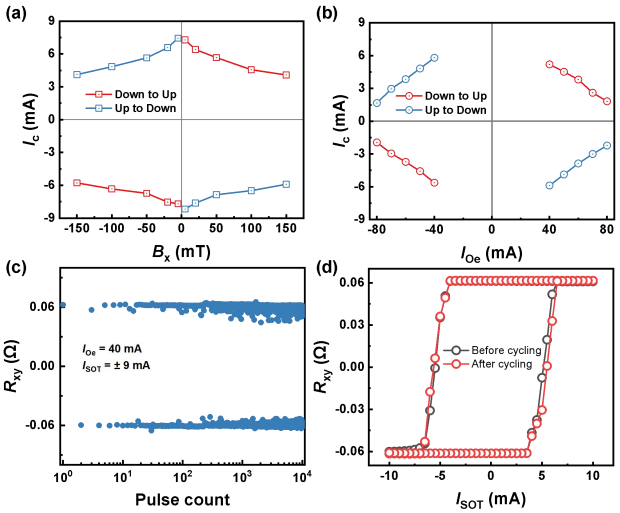
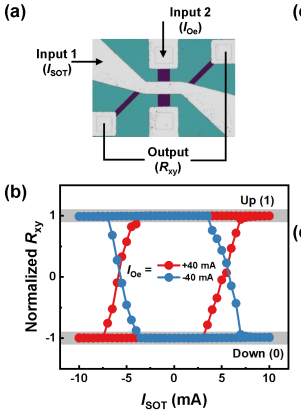


Fig. 3. The critical switching current *Ic* versus (a) B_x, and (b) I_{Oe}. (c) The FFS cycling test of OFA Hall-dot device. (d) The switching loops before and after the cycling test.

These results indicate that I_{Oe} provides both the Oersted field required for deterministic switching and a concurrent thermal reduction of the switching energy barrier. We note that the device shows excellent robustness, as evidenced by 10^4 successive cycles (Fig. 3 (c)). The switching loops before and after the cycling test are also compared (Fig. 3 (d)), confirming good endurance (> 10^4 cycles) and excellent repeatability of the OFA Hall-dot device.

C. Logic operations

Following the established FFS scheme in the OFA Hall-dot device, flexible logic operations can be realized using both I_{SOT} and I_{Oe} as two logic inputs. As illustrated in Fig. 4(a), I_{SOT} and I_{Oe} are defined as input 1 and input 2, respectively, while R_{xy} serves as the output. As shown in Fig. 4(b), the logic states '0' and '1' are defined by the magnetization direction of the Co dot, corresponding to downward magnetization (R_{xy} < 0) and upward magnetization (R_{xy} > 0), respectively.



(c)

	Input 1 (I_{SOT})	Input 2 (I_{Oe})	Output (R_{xy})
Initial state	-9 mA	+40 mA	Down (0)
AND	0 mA (0)	-40 mA (0)	Down (0)
	+9 mA (1)	-40 mA (0)	Down (0)
	0 mA (0)	+40 mA (1)	Down (0)
	+9 mA (1)	+40 mA (1)	Up (1)

(d)

	Input 1 (I_{SOT})	Input 2 (I_{Oe})	Output (R_{xy})
XNOR	+9 mA (1)	+40 mA (1)	Up (1)
	-9 mA (0)	+40 mA (1)	Down (0)
	+9 mA (1)	-40 mA (0)	Down (0)
	-9 mA (0)	-40 mA (0)	Up (1)

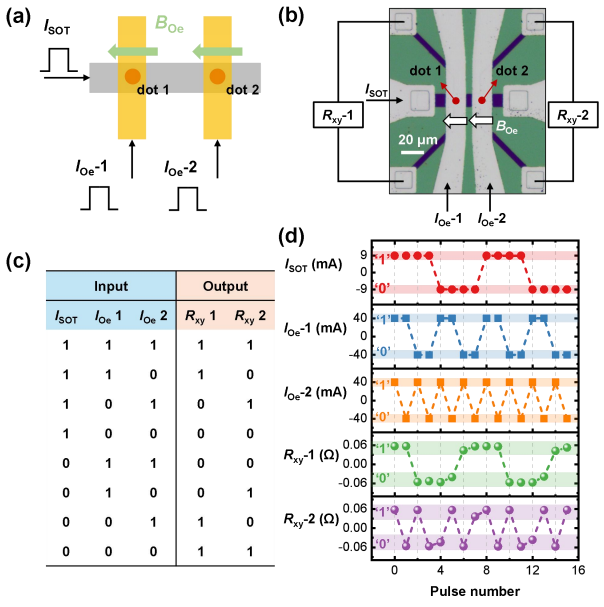
Fig. 4. (a) Schematic of the input and output in a single OFA Hall-dot device. (b) Definition of logic output '0' and '1'. The truth table of (c) AND, and (d) XNOR logic operations realized in a single OFA Hall-dot device.

By appropriately configuring the input–output mapping, a single OFA Hall-dot device can implement two logic functions: reconfigurable AND logic (Fig. 4(c)) and XNOR logic (Fig. 4(d)). In addition, CMOS-based AND and XNOR logic require six and ten transistors, respectively. In contrast, the OFA Hall-dot-based logic provides a compact way and is advantageous in terms of device area.

D. OFA dual-Hall-dot device

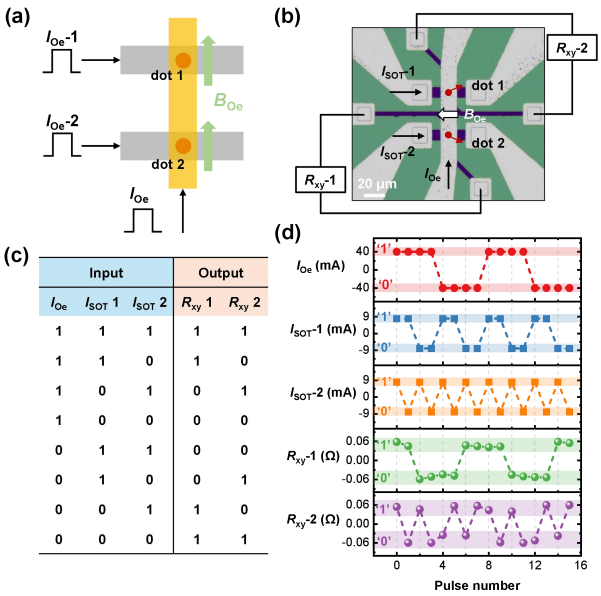
Integration of multiple dots with varying numbers of metal wire and SOT channel configurations offers a highly scalable memory architecture and flexible computing-in-memory frameworks. To validate the functionality, two types of OFA dual-Hall-dot devices are fabricated. The first configuration consists of two dots driven by a shared SOT channel and independently controlled by two metal wires (Fig. 5(a) and (b)), termed 2M-1S. As shown in Fig. 5(c) and (d), the switching polarity of each dot can be efficiently controlled by corresponding I_{Oe}, and the state of each dot can be programmed simultaneously in one cycle. The second configuration employs two independent SOT channels to switch two dots, while a single metal wire provides B_{Oe} (Fig. 6(a) and (b)), termed 2S-1M. In this configuration, the switching polarity of each dot can be efficiently controlled by corresponding I_{SOT}. Additionally, like the 2M-1S, the states of each dot can also be determined simultaneously in one cycle.

Moreover, as illustrated in Fig. 7(a) and (b), connecting the two metal wires head-to-tail, the opposite B_{Oe} can be generated over the two dots simultaneously, which naturally enables the complementary switching behavior. Fig. 7(c) and (d) show that the states of dot 1 and dot 2 are opposite under all configurations of inputs. This feature shows the strong potential of implementing efficient computing-in-memory [12,13].



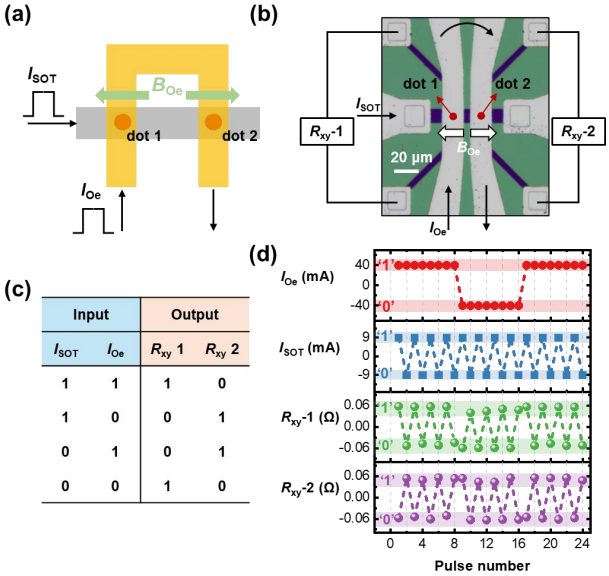
Input			Output	
I_{SOT}	I_{Oe} 1	I_{Oe} 2	R_{xy} 1	R_{xy} 2
1	1	1	1	1
1	1	0	1	0
1	0	1	0	1
1	0	0	0	0
0	1	1	0	0
0	1	0	0	1
0	0	1	1	0
0	0	0	1	1

Fig. 5. (a) Schematic and (b) optical image of the OFA dual-Hall-dot device with one SOT channel and two independent metal wires. (b) Truth table and (c) measured results of implemented operations in the 2M-1S device.



Input			Output	
I_{Oe}	I_{SOT} 1	I_{SOT} 2	R_{xy} 1	R_{xy} 2
1	1	1	1	1
1	1	0	1	0
1	0	1	0	1
1	0	0	0	0
0	1	1	0	0
0	1	0	0	1
0	0	1	1	0
0	0	0	1	1

Fig. 6. (a) Schematic and (b) optical image of dual-OFA-Hall-dot device with one metal wire and two independent SOT channels. (c) Truth table. (d) Measured results of operations in 2S-1M device.



Input		Output	
I_{SOT}	I_{Oe}	R_{xy} 1	R_{xy} 2
1	1	1	0
1	0	0	1
0	1	0	1
0	0	1	0

Fig. 7. (a) Schematic and (b) optical image of dual-OFA-Hall-dot device in complementary configuration. (c) Truth table. (d) Measured results of complementary operation in dual-OFA-Hall-dot device.

III. 5T-4R Cell Based on OFA-p-SOT-MTJs

Based on the ability to simultaneously write the states of two dots within one cycle (Fig. 5 and Fig. 6), we further extend this structure to devices with multiple p-MTJs. In a two-transistors and one-resistance (2T-1R) cell structure based on a conventional p-SOT-MTJ (Fig. 8(a)), only a single MTJ can be programmed in one write cycle (Fig. 8(b)), which fundamentally limits the write throughput. To mitigate this issue, based on the controllable switching polarity enabled by the OFA scheme, we propose a novel memory cell structure consisting of five transistors and four p-SOT-MTJs (5T–4R), as shown in Fig. 8(c). In contrast, in the proposed 5T–4R cell, four p-MTJs share one SOT channel, and can be written simultaneously within one write

cycle (Fig. 8(d)). This can significantly enhance the write parallelism and improve the effective write speed. For instance, assuming a write latency of 1 ns per cycle, in the proposed 5T-4R cell, four MTJs can be programmed in parallel within the same duration, resulting in an average effective write latency of 0.25 ns per MTJ. This corresponds to a 75% reduction in write latency for the same amount of data, demonstrating a substantial throughput advantage.

In addition, the 5T–4R configuration reduces the number of transistors when normalized per stored cell, leading to reduced cell area. The metal interconnects used to carry I_{Oe} can be implemented in the back-end-of-line (BEOL) layers and potentially reused from existing routing resources such as read bit-lines (RBL), ensuring good compatibility with standard CMOS processes.

Furthermore, the OFA scheme inevitably introduces additional energy consumption due to the generation of B_{Oe}. In our previous work [14], we combined experimental results and simulations to evaluate the energy consumption of the OFA p-SOT-MTJ. As the write pulse width decreases, the proportion of energy consumed by generating B_{Oe} relative to the total write energy decreases. For instance, at a write speed of 1 ns, the additional energy consumption accounts for only 9% of the total energy. Moreover, device optimization can further reduce this energy overhead. These advantages make the proposed OFA-based memory architecture a promising candidate for high-throughput and energy-efficient memory systems.

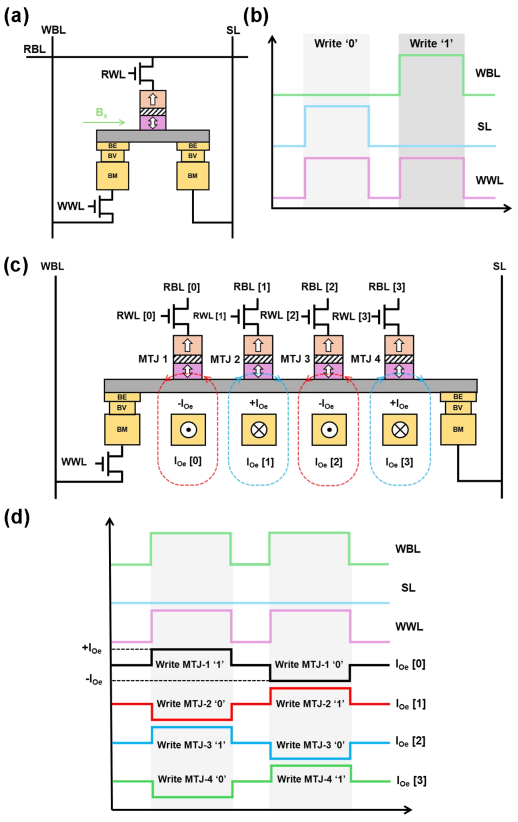


Fig. 8. (a) Schematic and (b) writing timing waveforms of 2T-1R cell structure based on a conventional p-SOT-MTJ. (c) Schematic and (d) writing timing waveforms of proposed 5T-4R cell based on OFA p-SOT-MTJs. The red and blue dashed lines with arrows represent the different directions of B_{Oe} generated by I_{Oe}.

IV. Conclusions

In this work, we propose an FFS scheme in spin–orbit torque (SOT) based devices, using the Oersted field generated by the current in metal interconnects. This CMOS-compatible scheme is experimentally demonstrated in a Hall-dot device, showing deterministic and controllable SOT switching polarity. Based on this capability, AND and XNOR logic operations are realized within a single OFA Hall-dot device. Furthermore, the OFA-dual-Hall-dot configurations enable multi-unit operation and complementary logic. Moreover, a 5T–4R memory cell based on OFA-p-SOT-MTJ is also proposed, achieving enhanced write parallelism and improved effective write speed. These results highlight the potential of the OFA SOT-based devices for high-speed memory and efficient computing-in-memory applications.

Acknowledgments

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