A 101 dB DR audio-band PPD-DSM with dynamically biased OTAs

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***Abstract*— This article presents a pseudo-pseudo differential (PPD) audio-band ADC with zero mean error encoding (ZMEE) based mismatch shaping and integrators with dynamically biased single-ended OTAs. It includes an optimized asynchronous SAR quantizer with series capacitor passive adder. It was fabricated in a 65-nm CMOS process and achieved 98.7 dB peak SNDR, 101-dB DR in a 20 kHz bandwidth, and 103.5 dB SFDR with a Schreier figure of merit (FoM$_S$) of 185.9 dB.**

Keywords—Analog-to-digital converter, delta-sigma (ΔΣ) modulator, digital-to-analog converter (DAC), dynamic element matching, mismatch shaping.

I. INTRODUCTION

The DSMs used in audio-band require high resolution and high energy efficiency. The high energy efficiency requirement has led to designs using pseudo-pseudo differential (PPD) architecture [1,3]. However, due to differential signal being processed in two phases, they require DT operation. Hence, the first integrator in such DSM often needs to provide surge of peak currents. This paper solves this problem using dynamically biased OTAs achieving state-of-art 185.9 dB FoM$_S$.

II. PROPOSED PPD-DSM

The proposed PPD DSM is shown in Fig. 1. In this 2nd order CIFF architecture, the differential input signal is processed in two phases (ϕ_1 and ϕ_2). The input is sampled using a pair of boosted sampling switches. The positive input signal is sampled onto the C_{DACP} at the end of ϕ_2 and the negative input is sampled onto C_{DACM} at the end of ϕ_1. During ϕ_1, C_{DACP} is connected to the first integrator and feedback for positive signal is applied to the bottom plates and the loop filter (constructed with delay-free integrators) settles within the phase. Towards the end of the phase (approximately 40 ns), the input feed-in signal and output of the loop filter is sampled inside the SAR quantizer to be passively added and converted to generate D_p. Similarly, the negative input signal is sampled in ϕ_1, and the loop filter processes it in ϕ_2. Towards the end of ϕ_2, the loop filter output and input feed-in signal are sampled and converted into the digital signal D_m. The feedback DACs are 9-bit capacitive DAC controlled by the output of zero mean error encoder (ZMEE), which is used for mismatch shaping [2]. In the ZMEE scheme, a running sum of the usages of each binary weighted DAC element is stored in a flip-flop. If the running sum is positive, an alternate encoding scheme is used otherwise normal encoding is used.

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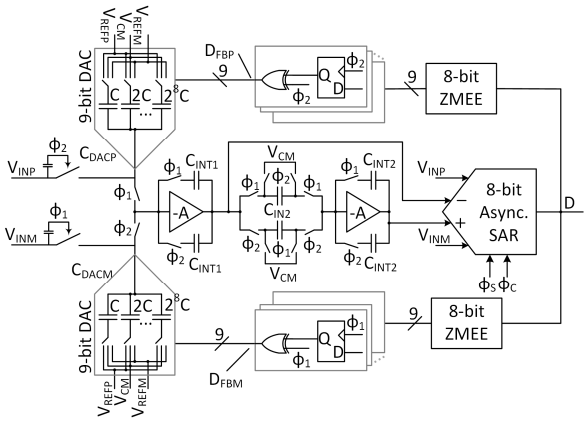

Fig. 1. Proposed 2nd order CIFF PPD-DSM with ZMEE mismatch shaping (C_{DACP} = C_{DACM} = 9.8 pF, C_{INT1} = 10.1 pF and C_{IN2} = C_{INT2} = 2 pF)

Such negative feedback results in bounded error contribution from each DAC element at the integrator output. Then the errors from each DAC element referred to the input of the integrator are first order shaped. The readers are referred to [2] for detailed description of the scheme. In such scheme, for 8-bit DAC implementation, a 9-bit tri-level DAC is required. When such feedback DAC is also used as the sampling capacitor, the feedback signal is reduced by a factor of two compared to the input. Therefore, feedback is double sampled to compensate for it. The double sampling is accomplished by storing D_p and applying its complement as feedback during ϕ_2 while a new positive signal is sampled onto the top plate of C_{DACP}. Similarly at the end of ϕ_2, the feedback for negative signal (D_m) is available and it is inverted and applied as feedback to C_{DACM} during ϕ_1, while a new negative signal is sampled onto the top plate. The digital outputs D_p and D_m are then subtracted in digital domain to calculate the final ADC conversion result. The benefit of the PPD architecture is that if the noise (such as flicker noise) and any other systematic errors (offsets) introduced in the DSM in ϕ_1 and ϕ_2 are the same, they will be cancelled while taking the difference. Therefore, schemes such as chopping and correlated double sampling are not required in order to cancel low frequency noise and offsets. The detailed timing diagram for the DSM is shown in Fig. 2. The output of the DSM, D, is referred to as D_p when it is DSM output for positive input signal (in ϕ_1) and D_m when it is for negative input signal (in ϕ_2).

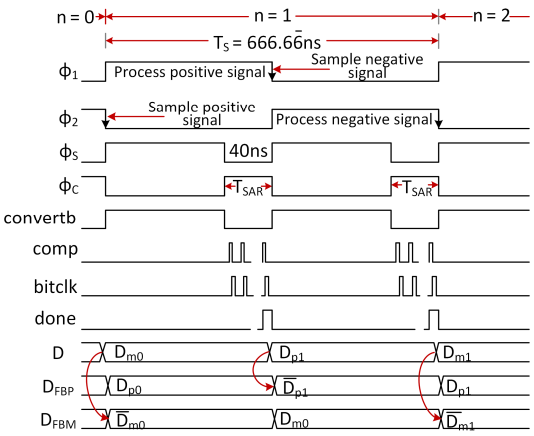

Fig. 2. Timing diagram (f_s = 1.5 MHz).

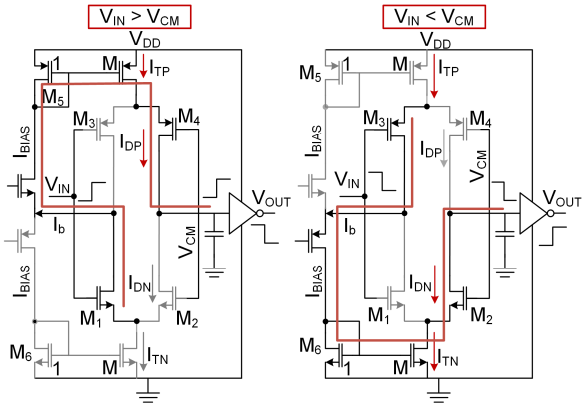

Fig. 3. Operation of proposed OTA when $V_{IN} > V_{CM}$ and $V_{IN} < V_{CM}$. The current flow and increase in bias current is shown in red.

A. *Dynamically biased OTA*

The power efficiency of the first integrator OTA is improved by using dynamic biasing. In a conventional differential pair, the large signal output current is given by:

$$I_{OP,N} = \pm\frac{kV_{IN}}{4}\sqrt{\frac{4I_{TAIL}}{k} - V_{IN}^2} \quad (1)$$

where, $k = \mu C_{OX} W/L$. In (1), the term inside the square-root decreases with increase in input magnitude. This factor represents the effect of reduction of bias current, which finally leads to saturation of output current. It also reduces the effective G_m as it contributes to the derivative of the output current w.r.t. input. The proposed OTA mitigates this issue by increasing bias current at the same rate as output current needs to be increased. The proposed OTA is realized as two-stage OTA with first differential stage followed by second single ended stage. One half of the output currents of the first differential stage is used to modify the bias current, while the other half is used for driving the second stage. This dynamically increases the bias current and directs it to the p-side or n-side of the first stage depending on the input polarity (Fig. 3). Then the bias current stays constant and hence G_m stays constant. In the proposed OTA, the large signal output current of the first stage is given by:

$$I_{OP,N} = \pm\frac{kV_{IN}}{2}V_{ov} \quad (2)$$

In (2), since there is no current saturating term (as in (1)), the output differential current simply becomes a linear function of the input. Therefore slewing does not occur even for a larger input. This continues until headroom limits further increase in bias current due to limiting of V_{gs} of M_5 and M_6. Such dynamic biasing helps improve G_m, unity gain frequency (UGF) and makes G_m constant across a wider input range. In addition, when used in switched capacitor circuits, the current drawn by the OTA increases during initial transient when large current needs to be supplied to the output capacitive load and relaxes to the nominal static bias current as soon as the output is settled. This eliminates slewing, improves settling time, and saves power.

With increase in G_m of the first stage, the non-dominant pole at the output of the first stage is pushed to higher frequency, and hence the loop bandwidth can be increased without degrading phase margin. The second integrator OTA is an $1/5^{th}$ scaled version of the first integrator OTA. Fig. 4 shows comparison of output current and effective G_m with that of conventional telescopic OTA biased with the same bias current.

B. *SAR Quantizer*

The output of the loop filter is sampled and quantized using an 8-bit asynchronous SAR quantizer. Inside the quantizer, the direct feed-in signal (connected to V_{IN1P} and V_{IN1M}) is sampled onto the bottom plate of a pair of 7-bit capacitive DACs. The loop filter output (connected to V_{IN2P} and V_{IN2M}) is sampled onto a pair of series capacitors (C_S). Fig. 5 shows the schematic of the SAR quantizer.

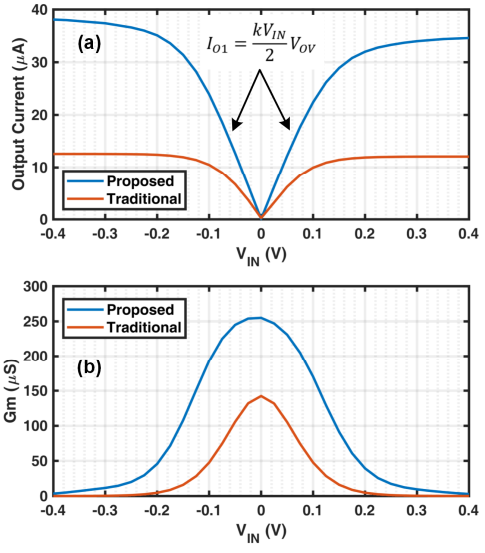

Fig. 4. Output current (a) and effective G_m (b) of first stage of the proposed OTA compared to an OTA with the same constant bias.

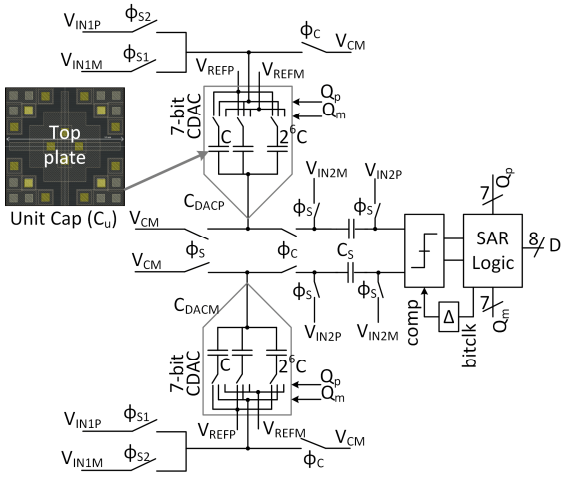

Fig. 5. The 8-bit asynchronous SAR ADC with passive signal addition (C_u = 1.1 fF and C_s = 100 fF).

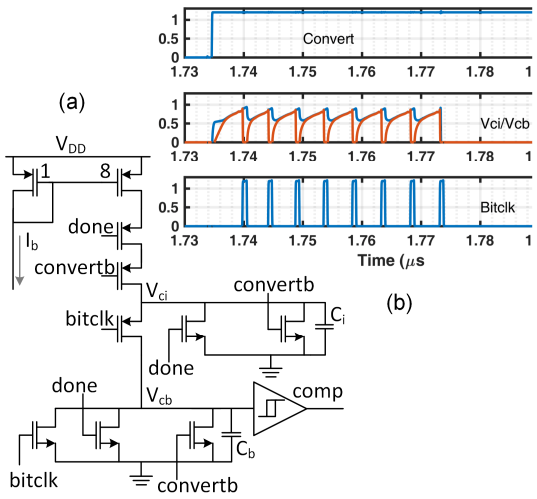

Fig. 6. (a) Proposed delay cell and (b) Time domain waveforms.

During the conversion phase, the voltage sampled onto C_s and the voltage sampled onto C_{DAC} are added by connecting them in series. This technique avoids need for active adders and hence saves power. The loop filter output is single-ended, however the feed-in signal is differential. Hence, the loop filter output is amplified (by 2x) by sampling it onto both series capacitors. In the conversion phase, the bottom plates of the C_{DAC} are connected to V_{CM} such that V_{IN} (input feed-in) appears on the top plate in ϕ_1 and $-V_{IN}$ appears in ϕ_2. Inside the asynchronous SAR, the bit clock is generated in a digital state machine with comparator done signal as the feedback to transition to next state. Then the comparator is strobed after a certain delay from transition to new state, allowing time for the DAC to settle. Inside the SAR quantizer, the bit clock is generated using a delay cell shown in Fig. 6(a). During the sampling phase, ϕ_C is 0 and hence *convertb* signal is 1. Therefore, capacitor C_b is discharged and since *bitclk* is also 0, capacitor C_i is also discharged. Although *done* is 0 at the beginning of the conversion, since *convertb* is high, there is no current flowing into either capacitors. When *convertb* goes low, during conversion phase, the $8\times I_b$ current flows onto both capacitors C_i and C_b. The capacitor C_i sets the initial delay between start of conversion phase and first comparison. This allows for additional settling time for DAC to settle. The capacitor C_b sets the successive delay for each bit cycle. After *convertb* goes low, the *comp* signal is generated when the capacitor voltage reaches the V_{IH} of the Schmitt trigger. The comparator is held in reset state when comp signal is not asserted such that both sides of the comparator are high. After comparison, the two outputs of the comparator will be different, indicating that comparison is done. This triggers assertion of *bitclk* and hence capacitor C_b is discharged while capacitor C_i keeps charging. This brings V_{cb} below V_{IL} of the Schmitt trigger and *comp* goes low resetting the comparator. This in turn makes *bitclk* go low and hence C_i and C_b are charge shared. Since C_b was discharged before charge sharing, it results in final voltage below V_{IH} of the Schmitt trigger and both capacitors starts charging again until the V_{IH} is reached. Fig. 6(b) shows the time domain waveforms.

The cycle continues until 8 comparisons are done; at which point, *done* signal is asserted until end of conversion phase such that the comparator is not clocked anymore. The DAC uses V_{CM} based switching scheme so that only 7-bit C_{DAC} is needed for 8-bit SAR. The C_{DAC} is constructed using a custom metal-oxide-metal unit capacitor (C_u = 1.1 fF) designed as a "cage" capacitor such that the top plate parasitic is reduced (Fig. 5 inset). The top plate of the cage capacitor is surrounded by bottom plate in all directions and hence top plate parasitic is significantly reduced. The SAR Logic is optimized using custom digital logic to save power. The SAR quantizer consumes only 2.4 µW from 1V supply when operated at 3 MHz sampling rate.

III. Measurement Results

The chip was fabricated in 65nm CMOS process and packaged in a 48-pin QFN. The PCB test board was built with LDOs and digital output buffers (SN74AUP3G04) to drive the logic analyzer. The chip was measured using input signal from the APx555 Audio Precision and output digital data was captured using TLA6204 Logic Analyzer. The clock was generated using Rigol DG822 signal generator. The measured output spectrum for input signal of -0.3dBFS is shown in Fig. 7. With mismatch shaping turned off, the SNDR is limited to 58.7 dB due to distortion. After enabling mismatch shaping the SNDR improves to 96.7 dB. The residual HD3 is at -103.6 dB, which is due to the first integrator OTA non-linearity. This non-linearity limits the SNDR to approximately 3 dB lower than SNR. This limitation comes from the fact that the OTAs operate at 1V supplies, which limits the benefits of dynamic biasing due to lack of headroom. The SNR is 99.6 dB and SNR-A (A-Weighted SNR) is 101.9 dB. The inset in Fig. 7 shows the results of a two-tone test with two sinusoids at -6dBFS amplitudes (19 kHz and 20 kHz). The IM3 products are below -89 dB, while IM2 is below -130dB.

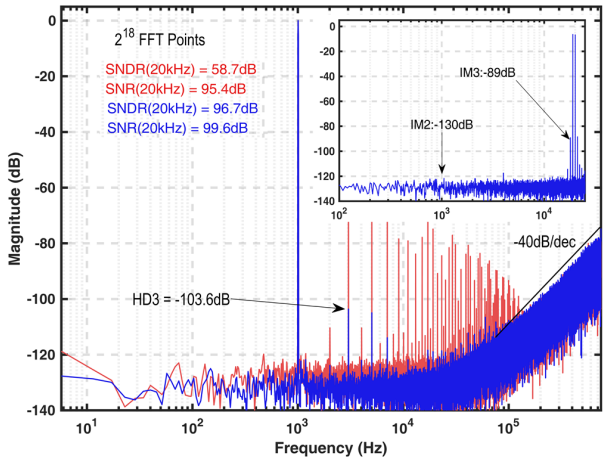

Fig. 7. Measured output spectrum of the DSM. (Red: Without mismatch shaping; Blue: With mismatch shaping). Inset shows two-tone test result with 19kHz and 20kHz input signals.

The chip uses 1.0V A_{VDD} and 1.2V D_{VDD} supplies. The total power consumption is 38 µW. The A_{VDD} (1V) power is 15.5 µW and D_{VDD} (1.2V) power is 22.2 µW including power used to drive the digital data off the chip. The power drawn from the reference was 9.1 µW. Fig. 8 shows the SNDR/SNR plot vs input signal and the pie chart showing power usages of various blocks. The peak SNDR is 98.7 dB at -0.7 dBFS, while the peak SNR is 102.1dB at -0.3 dBFS and the dynamic range is 101 dB. This results in Schreier Figure-of-Merit (FoM_S) of 185.9 dB and FoM_{DR} of 188.2 dB. Approximately 58% of the total power is used by the first integrator. The ZMEE logic consumes 4% of the total power. The first integrator power includes feedback DAC switching power and power drawn from both supplies.

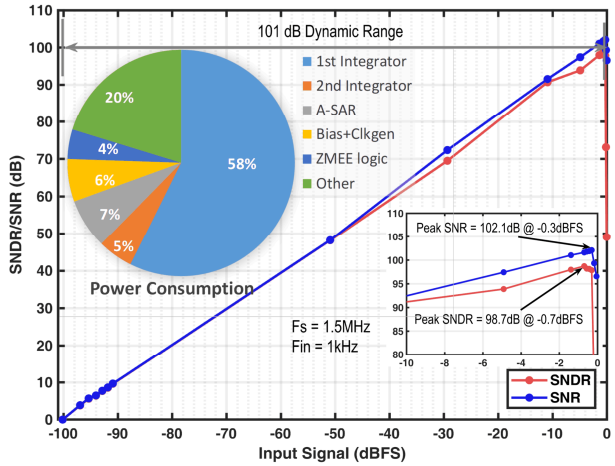

Fig. 8. Measured SNDR/SNR vs input signal. Insets show breakdown of power consumption and SNDR/SNR near full scale.

Table I shows the comparison of the performance with the state-of-art. The proposed DSM achieves similar performance for lower OSR, which facilitates audio system design with lower clock speed requirement. The proposed DSM achieves one of the best Figure-of-Merit in audio band DSM.

TABLE I. COMPARISON WITH STATE-OF-ART

	This work	**ISSCC'25 [1]**	**ISSCC'22 [3]**	**JSSC'20 [4]**	**VLSI'19 [5]**
Process	65nm	55nm	180nm	160nm	160nm
Supply (V)	1.2/1.0	1.0/1.2	1.8/1.1	1.8	1.8
Arch.	DT-PPD	PPD-Zoom	DT-PPD	DT-Zoom	CT-Zoom
DEM	ZMEE	DWA	DWA	DWA	DWA
SNDR (dB)	98.7	99.6	105.4	106.5	106.4
SNR (dB)	102.1		106.2	107.5	108.5
DR (dB)	101	102	108.8	109.8	108.5
Power (µW)	38	12.2	204	440	618
BW (kHz)	20	4	20	20	20
F_S (MHz)	1.5	1.0	5.8	3.5	5.16
OSR	37.5	125	145	87.5	129
FoM_S (dB)$^+$	185.9	184.8	185.3	183.1	181.5
FoM_{DR}(dB)*	188.2		188.7	186.4	183.6

$^+FoM_S$ = SNDR+10log10(BW/Power), $^*FoM_{DR}$ = DR+10log10(BW/Power)

The proposed DSM uses digitally synthesizable mismatch shaping scheme (ZMEE), which scales with process scaling. It reduces implementation complexities since it does not require multi-stage barrel shifters and analog muxes. Thanks to dynamically biased OTAs, the integrators settle with high accuracy even though the UGF of the integrator loop is only 4.3MHz, while the sampling frequency is 1.5MHz. For future improvements, the OTAs can be operated at higher supplies or implemented with lower v_{th} devices in order to fully benefit from dynamic biasing.

IV. CONCLUSION

In conclusion, a pseudo-pseudo differential DSM with ZMEE mismatch shaping and dynamically biased OTA was proposed. The innovations introduced reduced the power dissipation and resulted in excellent performance. The proposed architecture achieves one of the best Schreier FoM in audio-band DSM.

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