A ULP Event-Driven 5-40 MHz HBC SoC with 12.8 µs Wake-Up and Clock Recovery for Charging-Free Distributed Wearable AI

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***Abstract*—This work presents a human body communication ULP event-driven 5-40 MHz SoC integrating a clock-less wake-up receiver and a crystal-less clock-recovery unit. The architecture enables 0.25-5.8 µs clock-less wake-up with leakage-only listening for ULP high duty-cycled implantable and wearable AI nodes. With <9 pJ clock-less wake-up energy, and < 5µs clock recovery, we demonstrate a 45 µs system-level response from cold-start, enabling an aggressive always-off deep-idle operation with continuous wake-up monitoring.**

***Keywords*—Crystal-less, Clock-less, Wake-Up Receiver, Clock Recovery Unit, Ultra-Low-Power, Human Body Communication**

I. Introduction

In the ultra-low-power (ULP) body area network design, enabling distributed wearable artificial intelligence (AI) necessitates deploying complex inference capabilities across severely power-constrained, interconnected devices. Given the temporal sparsity of physiological anomalies, these systems remain idle for the majority of time. Consequently, maintaining a continuous reference clock and an active inference engine during idle periods becomes the dominant contributor to overall energy consumption. Achieving charging-free wearable AI therefore requires aggressive duty-cycling to amortize high active power consumption over long leakage-level idle periods, while maintaining negligible start-up energy and latency to enable instant data processing capability. Thus, the system remains deep-idle during inactive periods and transitions rapidly through clock recovery once adequate amount of data is collected, enabling efficient batch-based AI processing. Driven by growing demand for continuous, sparsity-aware sensing in these ULP wearables, recent solid-state works have introduced Wake-up receivers (WuRX) which duty-cycle high-power blocks into deep idle states, but maintaining a continuous timing reference for wake-up detection remains a dominant idle-power contributor [1,2]. Moreover, clocked WuRXs face a fundamental power-latency tradeoff: faster response requires a higher clock frequency and thus higher idle power. While prior works have introduced clock-less WuRX concepts [3,4] and crystal-less clock recovery units (CRUs) [3], their operation is limited to a single predefined frequency. Clock forwarding is employed in existing SOTA but further increases timing overhead and start-up energy [5], undermining its suitability for ULP, sparsity-driven wearable AI applications.

To address these challenges, this work presents a ULP 5-40 MHz event-driven architecture that not only integrates a clock-less wake-up receiver with a crystal-less clock-recovery unit but also incorporates additional peripheral circuitry to realize a complete, system-level solution. It covers full electro-quasistatic (EQS) human body communication (HBC) spectrum, enabling compatibility with existing HBC transmitter architectures, while avoiding on-chip DC-DC noise coupling at lower megahertz frequencies. The SoC remains leakage-powered and fully clock-less during idle and transitions to active mode only upon detecting a coded wake-up pattern. For a 5 MHz carrier, the SoC completes wake-up and carrier-frequency recovery in 12.8 µs and demonstrates an end-to-end response latency of 45 µs from the base-station request. Compared to [3], the proposed system shortens WuRX wake-up time by 13.8-222x and decreases the number of frequency-synchronizing CRU cycles by 3.5x. Furthermore, achieving >4x and >3.7x reductions in WuRX and CRU start-up energy ensures that the activation overhead remains negligible, preserving the overarching energy savings of duty-cycled burst processing. Finally, with wake-up robustness above 99%, this event-driven architecture achieves fast, reliable activation and enables leakage-only deep-idle operation for charging-free distributed wearable AI system.

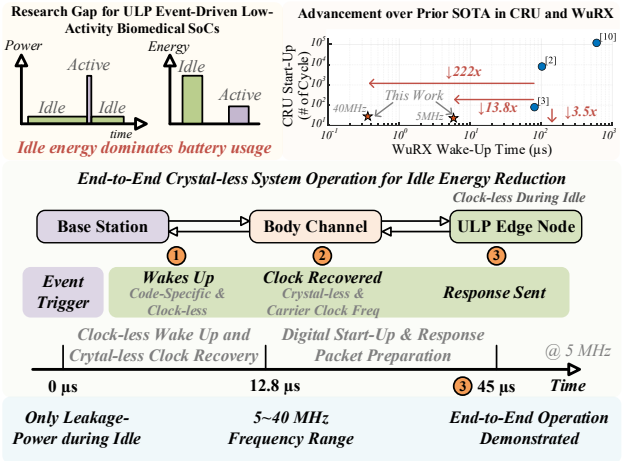

Fig. 1. System Concept of the Proposed Crystal-Less Event-Driven HBC SoC.

II. System Architecture

Conventional on-body sensor nodes rely on continuously running clocks to maintain timing continuity. The proposed system instead uses an event-driven architecture that stays clock-less during idle and activates its wake-up receiver and clock recovery only when interrogated by the base-station.

To realize this, the proposed system architecture is shown in Fig. 2. The received signal is first amplified by a 6-stage variable-gain amplifier (VGA) before reaching the clock-less WuRX. The WuRX operates entirely without an active clock and consumes only leakage power in the absence of input

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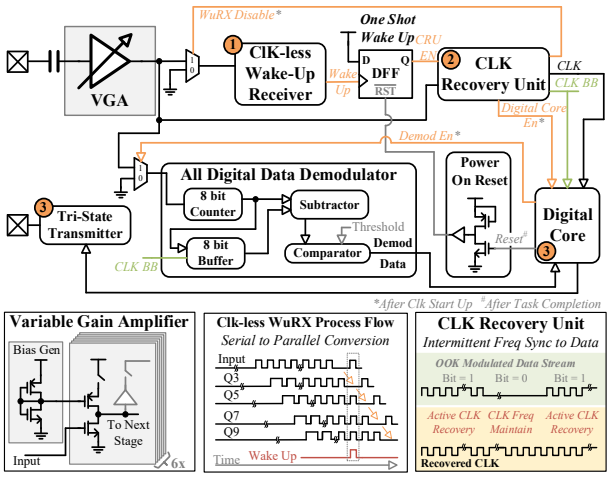


Fig. 2. End-to-End System Architecture of the proposed Clock-less and Event-Driven SoC.

activity. To correlate the input with a predefined wake-up sequence, the WuRX converts the serial input stream into a parallel word by introducing multiple one unit-interval (UI) delay stages. A combinational correlator then compares this word against the stored wake-up pattern. Once a match is detected, a wake-up pulse is generated to a delay flip-flop (DFF), which latches the event and initiates the start-up of the CRU.

The CRU rapidly recovers the carrier clock from the incoming signal, after which it disables the WuRX, enables the digital core, and provides a stable timing reference. Among the two operating modes, in the "ping-and-respond" mode, the digital core executes the predefined task and transmits the result back to the base-station through a tri-state transmitter (TX). After the transaction, the digital core resets the DFF, shutting down the CRU and reactivating the WuRX to return the system to its deep-idle state. In the continuous-demodulation mode, the digital core enables the all-digital demodulator while the CRU continuously recovers the carrier frequency from the on-off keying (OOK) data stream. During the "On" phase, the CRU locks to the carrier, and during the "Off" phase, it maintains the recovered frequency to ensure timing continuity.

III. Block-Level Circuit Implementation

A. Clock-less Wake-Up Receiver

The clock-less WuRX employs nine cascaded delay blocks, each generating a 0.5 UI delay to convert the incoming serial data stream into a parallel sequence for clock-less pattern correlation (Fig. 3). Each delay block has a reset-set flip-flop (RS FF) that automatically resets its output after a tunable delay determined by the discharge current of NMOS M1 and controlled by VTune. A frequency phase detector (FPD) compares the phase between the input signal and the output of the third delay stage (Q3) and adjusts VTune via negative feedback, enabling automatic locking of each stage to 0.5 UI of the carrier frequency. Combinational digital logic monitors the outputs of all nine delay blocks, selectively disables the FPD during intentional "0" intervals to prevent unnecessary tuning, and performs parallel pattern matching against the predefined wake-up sequence. To maintain detection integrity, a false wake-up protection mechanism leverages the interaction

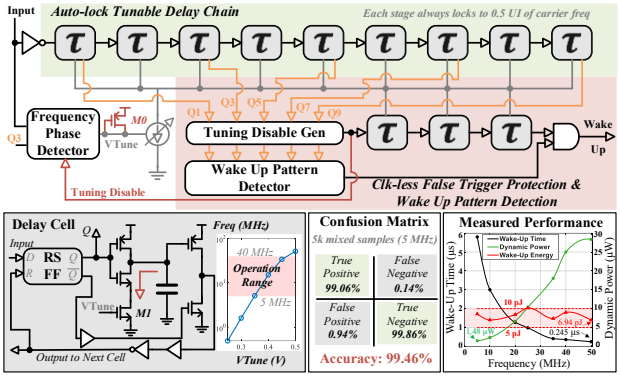


Fig. 3. Proposed Clock-less WuRX Architecture with Measured Results

between pattern detection and tuning-disable control to suppress spurious activations from incomplete or noisy transitions. All control logic is purely combinational, ensuring fully clock-less operation with no active running clock in idle mode.

Two circuit techniques improve both wake-up time and operating frequency range. A diode-connected PMOS (M0) trickle charges VTune to approximately 100 mV at start-up, ensuring a finite initial delay and enabling faster delay acquisition. This reduces minimum wake-up energy to 6.94 pJ, 4.8x lower than [3]. A larger NMOS (M1) further reduces the delay-cell RC constant, extending the delay-voltage characteristic to span 5-40 MHz (Fig. 3) across the full VTune adjustment range, 35x higher than the 1 MHz fixed frequency of the prior SOTA [3].

Wake-up robustness is also verified. Across 5k random test inputs at 5 MHz, the true-positive and true-negative rates exceed 99%, and the false-positive rate remains below 1%, yielding 99.46% overall wake-up pattern detection accuracy. Fig. 3 further shows the measured WuRX performance across 5-40 MHz, where the start-up energy remains consistent within 5-10 pJ, representing a 4x improvement compared with [3].

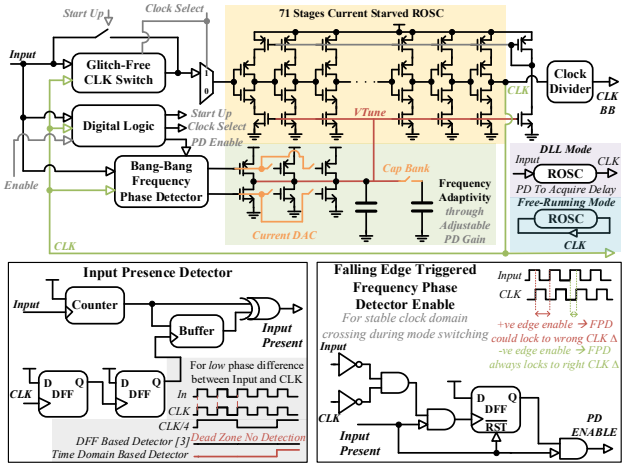


Fig. 4. Proposed Crystal-less Clock Recovery Unit with frequency range adaptive control, input presence detector and falling edge triggered FPD enable circuit.

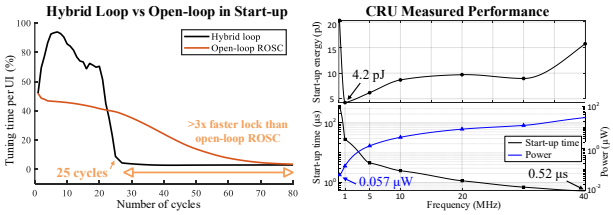


Fig. 5. (Left) The proposed hybrid loop achieves >3x faster start-up compared to open-loop ROSC in simulation. (Right) Measured start-up energy, latency and operational power against frequency.

B. Crystal-less Clock Recovery Unit

The CRU schematic is shown in Fig. 4. The core architecture consists of a reconfigurable current-starved ring oscillator (ROSC). The per-stage delay is proportional to the control voltage VTune. An FPD provides negative feedback to align the output frequency with the input automatically. The CRU performs two main functions. First, it recovers the carrier clock frequency from the OOK data stream by configuring the ROSC in an open-loop mode with the FPD enabled, mimicking a delay-locked loop (DLL) during the "On" period of the OOK signal. During the "Off" period, the ROSC is reconfigured into a closed-loop mode with the FPD disabled, holding VTune to preserve the recovered frequency.

A coarse time-to-digital converter (TDC) based input-presence detector replaces the conventional DFF scheme, which suffers dead zones when the input and ROSC frequencies are closely aligned. This can cause the CRU to enter open-loop just before the end of the "On" period, preventing timely return to closed-loop mode. The proposed TDC method counts input cycles and samples the count with a divided ROSC clock, ensuring reliable detection within the first four input cycles. Since open- and closed-loop transitions occur across two asynchronous clock domains, an edge synchronizer aligns FPD-enable transitions to the falling edges of both the input and ROSC clocks, ensuring reliable and deterministic switching.

The second function, fast start-up, is achieved through a hybrid closed-open loop mode that provides higher tuning efficiency than open-loop operation alone. This behavior is reflected in the measured tuning percentage per UI in Fig. 5. A programmable current DAC adjusts the FPD gain according to the operating frequency, which enables stable and rapid locking across the full 5-40 MHz range and allows operation down to 0.1 MHz. This approach provides fast frequency locking while maintaining wide-range operability.

Fig. 5 shows the measured characterization of the CRU. The start-up time, defined as the duration from CRU activation to locking to the carrier frequency, consistently decreases with frequency. It reduces from 4.6 µs at 5 MHz to 0.52 µs at 40 MHz. At 1 MHz, which is the lowest start-up energy point of 4.24 pJ, the proposed design is 6.6x lower than prior SOTA [3], supported by a 2.85x reduction in start-up time and a 2.32x reduction in power.

C. Variable Gain Amplifier

While the WuRX performs clock-less correlation to a specific input pattern and CRU recovers carrier frequency, the VGA amplifies the base-station signal transmitted through the human body channel. As reported in [6], the HBC channel loss

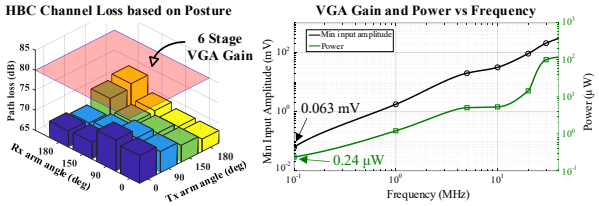


Fig. 6. Variable Gain Amplifier measured characterization.

varies with device placement and user posture, typically ranging from 65-75 dB, thereby requiring front-end amplification before reliable WuRX correlation.

A 6-stage VGA is implemented as shown in Fig. 2. Each stage is a common-source amplifier, and all stages share a self-biased inverter network that generates the bias voltage. The stages are individually power-gated when disabled to minimize leakage. Fig. 6 shows the measured sensitivity and power versus frequency. With all stages enabled, the amplification chain detects input signals as small as 61 µV at 0.1 MHz while consuming 235 nW, corresponding to an overall maximum sensitivity of -84 dBV when using high-impedance HBC input termination instead of the conventional 50 ohm termination [7]. This sensitivity supports the worst-case EQS HBC channel loss and provides a 28 dBV improvement over prior HBC SOTA [8].

IV. Measurement Results and Comparison

Fig. 7 shows the oscilloscope-captured waveform of the event-driven end-to-end operation with the measurement setup shown in Fig. 8. The IC is externally powered, and an arbitrary waveform generator (AWG) emulates the base-station by providing a 5 MHz input to the IC. During the first 7 µs, the AWG outputs a pure 5 MHz square wave for the clock-less WuRX to lock onto the carrier frequency. At 7 µs, the AWG transmits a specific wake-up pattern, which is detected by the WuRX and enables the crystal-less CRU. The CRU then starts up and locks to the incoming carrier (<3% of frequency variation) within 12.8 µs. After locking, the CRU disables the WuRX and activates the digital core to transmit data back to the

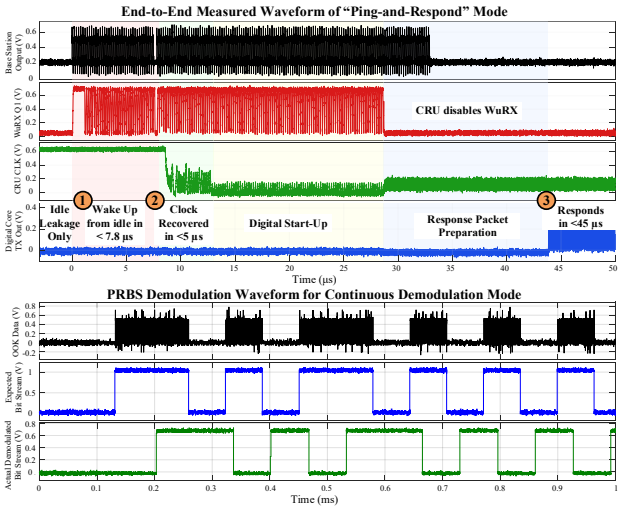
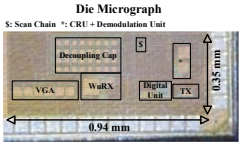


Fig. 7. Measured End-to-End waveform showing clock-less wake-up, crystal-less clock rssecovery and < 45 µs data response, with demodulated PRBS baseband.



Specifications	
Process	TSMC 65nm
VDD	0.49 – 1.2V
Die Area	0.33 mm^2
Active Area	0.069 mm^2
Frequency Range	5~40 MHz
Communication Channel	Human Body & Metallic Structure
Modulation Scheme	On-Off-Keying

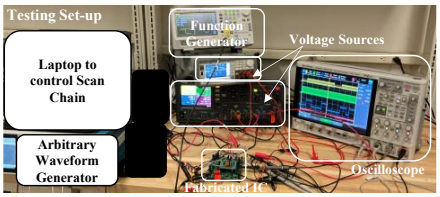


Fig. 8. Die micrograph, testing set-up and chip specifications.

TABLE I. COMPARISON WITH PRIOR STATE-OF-THE-ART

		This Work		ISSCC'25 [3]	JSSC'21 [10]	JSSC'16 [9]	JSSC'15 [2]	ISSCC'23 [1]	JSSC'20[4]
Analog Front End	Sensitivity	≥63 µV (-84 dBV*#§)		Not Reported	-86 dBm	NA	-62 dBm	-60.4 dBm	-80.9 dBm
	Power	0.235 ~ 118 µW			378 µW		30 µW	Not Reported	
	Operational Frequency	0.1 ~ 40 MHz		Up to 1 MHz	2.4 GHz		Up to 110 MHz	Up to 920 MHz	Up to 450.8 MHz
Clock Recovery	Crystal-less	Yes		Yes	Yes	Yes	Yes	NA	Yes
	Recovery through data stream								NA
	Operational Frequency	5 MHz	40 MHz	1 MHz	2.4 GHz	2~7 GHz	80 MHz		
	Power	1.36 µW	30.16 µW	351.7 nW	999 µW	22.5 mW^	10 µW		
	Start-Up Latency	4.6 µs	0.525 µs	80 µs	50 µs	600 µs	102 µs		
	Start-Up Energy	6.28 pJ	15.83 pJ	28.136 pJ	49.95 nJ	13.5 µJ	1.02 nJ		
	Demodulation Bit Error Rate	<10^{-3}		NA	<10^{-4}	<10^{-12}	<10^{-3}		
WuRX	Leakage-only Idle	Yes		Yes	No	NA	No		Yes
	Idle Power	352 nW§		191.6 nW	Not Reported		45 µW	17.8 nW	Not Reported
	Operational Frequency	5 MHz	40 MHz	1 MHz	2.4 GHz		80 MHz	4 kHz	450.8 MHz
	Power	1.48 µW	24.9 µW	425.5 nW	324 µW		45 µW	17.8 nW$^{\&}$	40 nW$^{\&}$
	Wake-Up Latency	5.8 µs†	0.36 µs†	80 µs†	600 µs		102 µs	2 ms	110 ms
	Wake-Up Energy	8.58 pJ	8.96 pJ	34 pJ	194 nJ		4.59 nJ	35.6 pJ	4400 pJ
Modulation		OOK		OOK	FSK	Not Reported	FSK	OOK	OOK
System End-to-End Demonstration		Yes		No	Yes	NA	Yes	Yes	Yes
Area (mm^2)		0.069		0.077	1.33	1.63	1	0.09	0.15
Technology		65 nm		65 nm	40 nm	65 nm	0.18 µm	65 nm	65 nm

*: Assume base station transmits at 1V; #: HBC high impedance termination; &: includes VGA power; $: includes all peripheral circuits (e.g., scan chain, bias gen); §: Highest sensitivity at 0.1 MHz; †: Standalone WuRX measurement; ^: whole system power.

base-station, completing the entire "ping-and-respond" sequence in < 45 µs. This result validates an ultra-low-power, event-driven architecture that enables instant wake-up and normally deep-idle operation for biomedical edge systems.

Fig. 7 also shows the measurement waveform of the continuous-reception mode. In this mode, the AWG sends an OOK-modulated pseudo-random binary sequence, and the CRU recovers the carrier frequency to generate the baseband demodulation clock. Together with the all-digital counter-based demodulator, the system reconstructs the data stream. The bit error rate (BER) was evaluated over 1k samples with no errors observed, corresponding to a BER below 10^{-3}. These results confirm correct data demodulation and demonstrate stable continuous carrier tracking without frequency drift or phase loss.

Table I summarizes the comparison against prior SOTA. The proposed crystal-less CRU covers 5-40 MHz, compared to a single 1 MHz frequency design in [3]. Compared with [9] which targets a different application and supports a broader frequency range, this work delivers a >100x faster clock recovery start-up at <1% of the power consumption. The clock-less WuRX consumes 352 nW of idle power, which is higher than [3], but it includes peripheral blocks such as scan logic and bias generation to support realistic always-on operation. Benefiting from a 13-222x faster wake-up, the WuRX achieves a wake-up energy of approximately 8.6 pJ across 5-40 MHz. Compared with single frequency designs, the wake-up energy is >3.5x lower than [1] and [3]. Compared with a 2.4 GHz WuRX and CRU design for BLE applications [10], despite 60x-480x lower in carrier frequency, this work achieves 11-95x and 103-1667x lower latency in clock recovery and wake-up. Fig. 8 shows the die micrograph and key specifications of the 65 nm TSMC CMOS IC with 0.069 mm^2 active area.

V. CONCLUSION

In summary, the proposed event-driven architecture enables 12.8 µs instant wake-up and clock recovery with normally deep-idle operation for ULP charging-free distributed wearable AI. The WuRX starts up in 0.36-5.8 µs with best-in-class energy, and the CRU recovers the carrier frequency in 0.52-4.6 µs while supporting 5-40 MHz operation. The end-to-end "ping-and-respond" demonstration confirms the viability of ultra-low-power, mostly-off yet constantly listening wearable AI systems.

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