A 7-bit 900-MS/s SAR-TDC Hybrid ADC with PVT Robust VTC/TDC and Offsets Compensation

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***Abstract*—This paper presents a 7-bit 900-MS/s hybrid SAR-TDC architecture implemented in 28-nm CMOS technology, designed to minimize calibration overhead. The proposed design employs a Pseudo Loop-Unrolled (PLU) SAR ADC for coarse quantization, which utilizes a voltage-to-time converter (VTC) as a shared dynamic amplifier for latches. This scheme effectively suppresses offset mismatches among multiple latches without the need for additional pre-amplifiers. To ensure PVT robustness, the backend utilizes a replica-based identical unit structure for both the VTC and the TDC, achieving a full-scale mismatch of less than 0.3 LSB across all corners. Furthermore, through early polarity decision, the proposed architecture ensures to generate reliable absolute time residue. A digital domain 2's complement logic is also proposed to correct code gap errors induced by folded inter-stage offset, eliminating the need for complex calibration. The prototype ADC occupies an active core of 0.00527 mm^2 and consumes 2.8 mW, achieving an SNDR of 41.0 dB and a Walden Figure-of-Merit (FoM) of 34.1 fJ/conv.-step.**

I. Introduction

As CMOS technology scales, the reduction in supply headroom makes it difficult to achieve a high signal-to-noise ratio (SNR) in voltage-domain ADCs. To overcome these constraints, time-domain converters (TDCs) have been investigated as alternatives by processing signals in the horizontal time domain [1], which offers superior operating speed in advanced technology nodes with shorter gate delays.

Despite these advantages, TDC performance is constrained by the nonidealities of the voltage-to-time converter (VTC), which suffers from limited dynamic range. Thus, hybrid architectures combining a robust voltage-domain quantizer for MSB decisions with a fine stage TDC presents a reasonable solution. In particular, architectures employing an energy-efficient SAR ADC for coarse quantization have been widely adopted [2], [3]. Fig. 1 shows a block diagram of a conventional SAR-TDC architecture. While SAR ADC is compact and energy efficient, its iterative conversion loop involving residue amplification, comparison (latching), and CDAC settling limits the conversion speed compared to the fine-conversion TDC. Furthermore, the gain error induced by the PVT sensitivity of VTC and TDC is significant to the performance. While previous work [3] has utilized PVT-tracking VTC and TDC to achieve gain matching, the structures between them are not perfectly identical, which requires careful design to ensure reliable calibration coverage. In addition, while the 1-bit folding architecture [2], [3], [4], [5] is preferred for hardware-efficient absolute time generation, the potential race condition between the polarity decision and the arrival of residue signal demands careful management of inter-stage errors such as offset, nonlinearity and metastability.

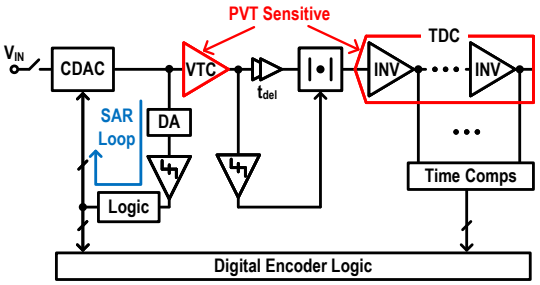

Fig. 1. Block diagram of conventional SAR-TDC

To address the aforementioned challenges of speed limitation in SAR and inter-stage nonidealities, this work proposes an improved SAR-TDC architecture. The proposed design employs a Pseudo Loop-Unrolled (PLU) SAR ADC combined with PVT robust VTC and TDC. Unlike conventional Loop Unrolled (LU) SAR ADCs that suffer from offset mismatches between multiple latches (comparators), the PLU SAR utilizes a VTC as a shared dynamic amplifier (DA) for the subsequent latches to suppress the offset mismatches. Also, in order to ensure PVT robustness, the proposed work employs identical unit-based structure for VTC and TDC to ensure PVT robustness. Furthermore, errors occurring during the generation of the absolute time residue are resolved through early polarity decision and simple digital logic. By incorporating these techniques, this work achieves a robust performance of SAR-TDC architecture that significantly minimizes the overall calibration burden.

II. Proposed PLU SAR with PVT robust VTC/TDC

A. Overall Architecture

The proposed 7-bit ADC architecture, illustrated in Fig. 2, consists of a 3-bit coarse PLU SAR ADC, a current-starved inverter (CSI) based VTC (CSI VTC), and a 4.5-bit fine CSI-based Vernier TDC with 1-bit folding. To facilitate the operation of the fine TDC, an inter-stage VTC is required to convert the residue voltage from the SAR ADC into time-domain signal. In this design, the VTC is implemented as a structural replica of the fine Vernier TDC using identical CSI cells (CSI TDC) for better full-scale matching between the VTC and TDC. Furthermore, rather than employing an extra pre-amplifier for the multiple latches in PLU SAR ADC, this work leverages the first-stage CSI of the CSI VTC as a shared pre-amplifier, thereby achieving hardware efficiency while reducing inter-stage

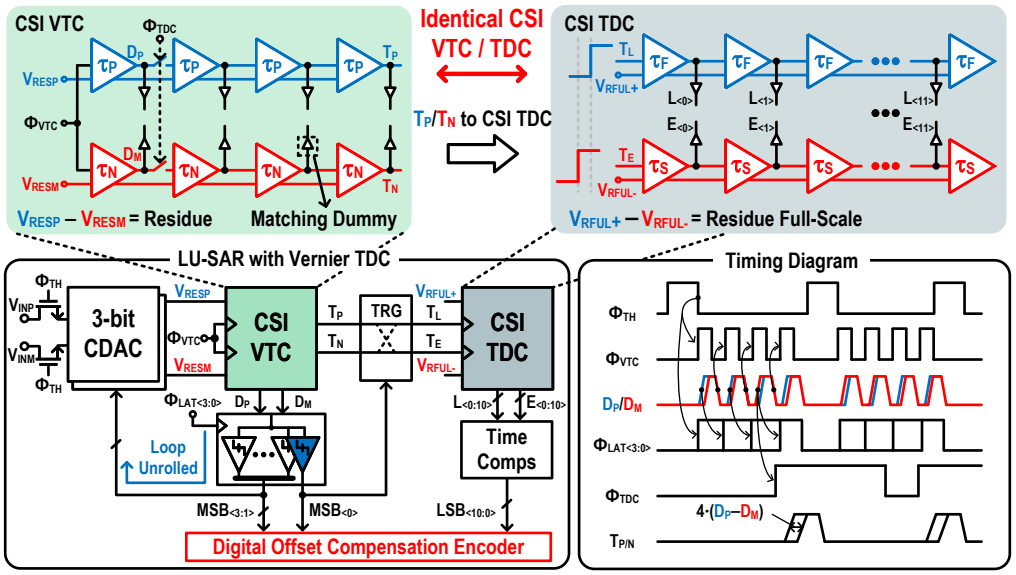

Fig. 2. Overall architecture of the proposed SAR-TDC architecture employing PLU SAR with an identical unit based VTC and TDC

offsets. However, signal propagation from the first-stage CSI to the subsequent CSI array of the VTC and TDC during the coarse SAR operation causes unnecessary power consumption, as these backend components are not required until the SAR phase is complete. To mitigate this issue, CSI unit cells incorporating series switches are inserted after the first-stage CSI to decouple the subsequent CSI VTC array from the first-stage CSI during coarse operation. Upon completion of coarse operation, the subsequent VTC array and fine TDC are activated when Φ_{TDC} transitions to high. During Φ_{TDC} clock phase, the first stage of the VTC is re-used as a voltage-to-time converter for the residue signal. Subsequently, the remaining VTC array amplifies time signal, after which a time residue generator (TRG) produces the absolute time residue for the fine conversion.

B. VTC/TDC based on Identical CSI units for PVT Robustness

The major bottleneck in Hybrid ADC architectures with TDC backend is the inherent gain mismatch between the voltage-to-time and time-to-digital conversion stages. Furthermore, because the VTC and TDC typically employ different topologies [2], [6], the entire system becomes highly sensitive to PVT variations. Fig. 3(a) shows that [3] pursues PVT robustness by establishing a proportional relationship between the discharging current sources of the VTC and TDC (αI_N, I_N). Nevertheless, due to the structural discrepancy between the pseudo differential VTC and the single-ended TDC, the PVT sensitivity of the charging current (I_P)-based delay within the TDC remains inevitable. To address this, the proposed architecture maintains the structural consistency by adopting a pseudo differential Vernier TDC, as shown in Fig. 3(b): specifically, the differential structures of both the VTC and TDC ensure that PVT sensitive charging current (I_P)-based delays are differentially canceled out. Moreover, the VTC and TDC employ identical CSI units (i.e., CSI VTC, CSI TDC), with their differential discharging current (I_N), designed to be proportional to the residue voltage ($V_{RESP} - V_{RESM}$) and the residue full-scale ($V_{RFUL+} - V_{RFUL-}$), respectively. One design concern is that, if the

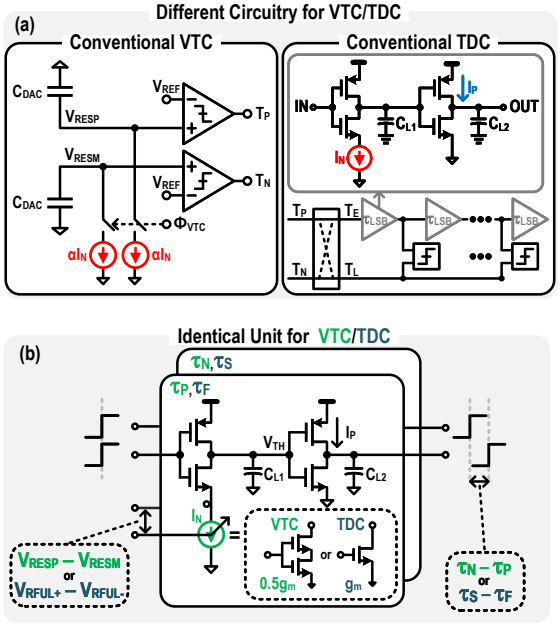

Fig. 3. VTC/TDC implementation of (a) Conventional (b) Proposed

VTC and TDC share an identical unit CSI, the number of unit CSIs for the VTC must be equal to that for the TDC to ensure full-scale alignment. This implies that, as the TDC resolution increases with more CSI units, the VTC latency also increases. To reduce the VTC latency penalty, the proposed architecture achieves full-scale matching by doubling the VTC gain, allowing the VTC to use only half as many unit cells as the TDC. In our implementation, we use only four CSI units for VTC while the TDC requires eight CSI units for 3-bit decision after 1-bit folding (However, it should be noted that the TDC is actually implemented with 12 CSI units including redundancy, i.e.,3.5b implementation).

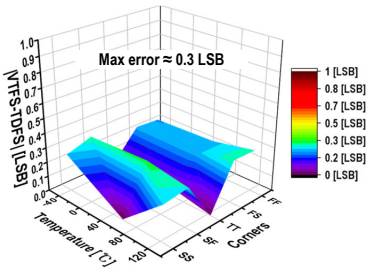

Fig. 4. Simulated absolute VTC/TDC full-scale mismatch across PVT variations

The unit VTC employs stacked discharging transistors to halve its transconductance and common-mode current compared to the unit TDC, effectively doubling the VTC gain. Detailed analytical expressions for the output difference of the unit TDC and unit VTC are provided in (1) - (3): First, the output difference of the CSI TDC, which means LSB in CSI TDC is defined as :

$$\tau_S - \tau_F \approx \frac{C_{L1}(V_{DD} - V_{TH})}{{I_C}^2} \cdot g_m(V_{RFUL+} - V_{RFUL-}) \quad (1)$$

where I_C and g_m denote the common-mode current and the transconductance of the discharging transistor within the unit TDC. V_{TH} refers to the logic threshold voltage of the subsequent inverter. Next, considering that the common-mode current and the transconductance of the unit VTC cell are reduced by half due to the stacked configuration of the discharging transistors, the output of the unit VTC is derived as :

$$\tau_N - \tau_P \approx \frac{C_{L1}(V_{DD} - V_{TH})}{(0.5I_C)^2} \cdot 0.5g_m(V_{RESP} - V_{RESM}) \quad (2)$$

From (1) and (2), the ratio of the unit VTC output to the unit TDC LSB is expressed as :

$$\frac{\tau_N - \tau_P}{\tau_S - \tau_F} \approx \frac{2(V_{RESP} - V_{RESM})}{V_{RFUL+} - V_{RFUL-}} \quad (3)$$

As depicted in Fig. 4, owing to the replica-based design, the proposed work reduces the absolute VTC and TDC full-scale mismatch within ~0.3 LSB across all PVT corners.

III. Solution to Inter-Stage Nonidealities

A. Time Residue Generator with Parallelized Polarity Decision

In TDC designs, a 1-bit folding architecture that process absolute value of time signal is preferred due to its advantage in conversion speed and area efficiency. In such an architecture, while MUX-based TRG [2] eliminates the dynamic inter-stage offset, which is major design issue in AND/OR-based TRG [3], it must ensure that the polarity decision is completed before the time signal arrives at the TRG input. This requirement introduces a risk of metastability to the polarity decision.

The proposed architecture overcomes this race problem of MUX-based TRG by leveraging the inherent characteristics of our multi-stage VTC configuration. As depicted in Fig. 5(a), while the first-stage unit VTC output (D_P/D_M) is being amplified through subsequent stages into T_P/T_N for the MUX-based TRG, the same D_P/D_M is used to determine the polarity, ensuring that the polarity decision is completed before the amplified time signal reaches the TRG input. This parallel operation provides a sufficient timing

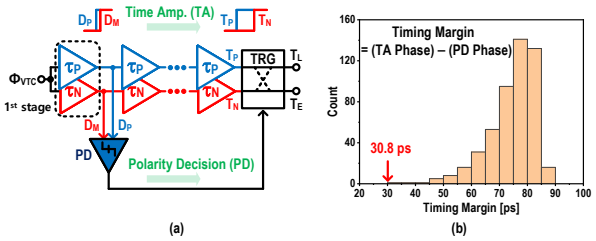

Fig. 5. (a) Parallel polarity decision and residue time amplification (b) Simulated timing margin distribution over 500 noise runs with zero differential input (D_P/D_M)

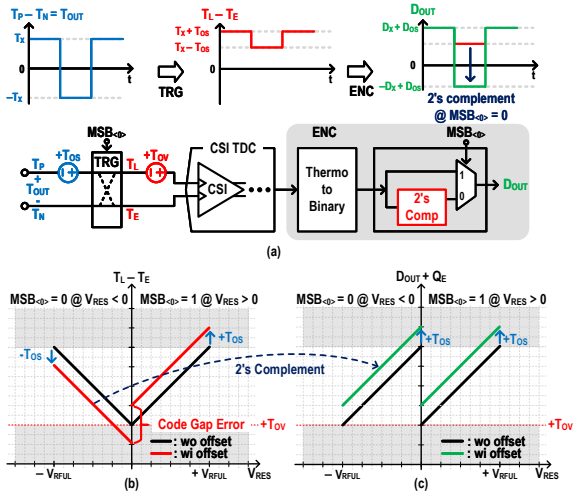

Fig. 6. (a) Block diagram of folded inter-stage offset alignment (b) TRG output example (c) Encoder output with quantization noise example

margin for polarity decision. The effectiveness of this approach is verified in Fig. 5(b), where a worst-case timing margin of 30.8 ps is confirmed through 500-run noise simulations with zero differential input.

B. Inter-Stage Offset-induced Code Gap Error Correction

In TDCs having a 1-bit folding architecture, the folding operation within the TRG inverts not only the input signal but also inter-stage offset based on the polarity decision ($MSB_{\langle 0 \rangle}$). Fig. 6(a) illustrates the signal transition waveforms through each block, assuming T_{OUT} toggles between $+T_X$ and $-T_X$. When the inter-stage offset (T_{OS}) exists, the TRG inverts T_{OUT} alongside T_{OS} whenever T_{OUT} is negative (indicated by $MSB_{\langle 0 \rangle}$ = 0). Consequently, the TRG outputs for $+T_X$ and $-T_X$ are translated into T_X + T_{OS} and T_X - T_{OS}, respectively. This polarity inversion in T_{OS} creates code gap error, whose size is equivalent to twice the inter-stage offset, as depicted in Fig. 6(b).

In order to tackle this problem, previous works relied on burdensome offset calibration. Motivated by the fact that typical voltage-domain architectures readily address inter-stage offset errors through redundancy and simple digital correction, this work proposes a simple digital domain error correction solution for 1b folding-based time-domain ADCs. First, an intentional offset ($+T_{OV}$) is introduced at the TDC input via unit TDC LSBs to ensure the CSI TDC can detect the code gap error,

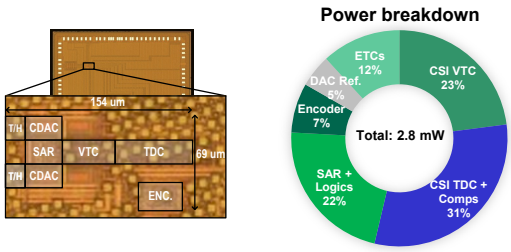

Fig. 7. Chip photo and Power breakdown

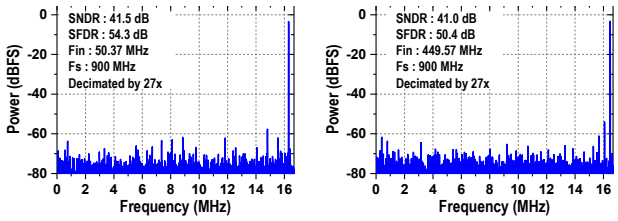

Fig. 8. Measured FFT spectrums (decimated by 27)

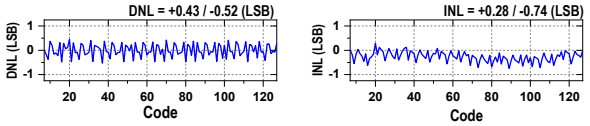

Fig. 9. Measured DNL and INL

even when T_L - T_E is negative. As illustrated in Fig. 6(b) and (c), a 2's complement operation is applied when $MSB_{\langle 0 \rangle}$ = 0 to reconstruct the non-folded code with $+T_{OS}$ from the folded code with $-T_{OS}$. By leveraging the symmetric property of 2's complement, the folded inter-stage offset is transformed into an ADC output offset preserving the linearity, making the inter-stage offset to appear as offset only when its effect is referred to the input.

IV. Measurement Results

The prototype ADC was fabricated in a 28-nm CMOS process, occupying an active core area of 0.00527mm² with a total power consumption of 2.8 mW, with further detail provided in Fig. 7. The measured FFT spectra at a 0.9 GS/s sampling rate are shown in Fig. 8. With a low-frequency input of 50.37 MHz, the converter achieves an SNDR of 41.5 dB and an SFDR of 54.3 dB. At the Nyquist frequency, the SNDR and SFDR are maintained at 41.0 dB and 50.4 dB, respectively. Fig. 9 shows that the measured peak DNL and INL are +0.43/–0.52 LSB and +0.28/–0.74 LSB, respectively. Fig. 10 illustrates the measured SNDR and SFDR across an input frequency sweep at 0.9 GS/s conversion rate, as well as a sampling frequency sweep with a 55.57 MHz input. Table I summarizes the performance of the prototype ADC and compares it with recently published hybrid time-domain ADCs. Our design achieves a Walden FoM of 34.1 fJ/conv.-step, demonstrating competitive performance with robustness, without any offset calibration.

V. Conclusion

This paper presented a 7-bit 0.9-GS/s Hybrid ADC in 28-nm CMOS technology. The shared VTC scheme suppresses offset mismatches of multiple latches in the PLU-SAR stage and alleviates

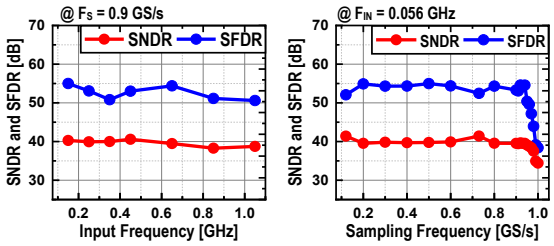

Fig. 10. Measured SNDR and SFDR across various input frequencies and sampling frequencies

TABLE I
Performance Summary and Comparison with State-of-the-Art ADCs

Parameter	This work	TCAS-II'17 [7]	JSSC'23 [5]	TCAS-II'24 [8]
Technology [nm]	**28**	40	22	28
Architecture	**SAR-TDC**	LU-SAR	4X TDC-SAR	FLASH-TDC
Resolution [bits]	**7**	6	7	6
Supply [V]	**1.0**	1.2	1.0/1.2	0.9
Fs [GS/s]	**0.9**	0.7	3.8	4.0
Power [mW]	**2.8**	0.95	6.0	8.1
$ENOB_{@Nyq}$ [bits]	**6.51**	5.5	6.0	4.79
FoM_W [fJ/c-s]	**34.1**	30	24.4	73.1
Offset Cal. Needed	**None**	Yes	Yes	Yes

*FoM_W = Power / (2^{ENOB} · f_s)

inter-stage offset. By employing identical unit-based VTC and TDC, the architecture achieves PVT insensitive VTC and TDC gain. Furthermore, the parallel polarity decision with time amplification ensures reliable time residue generation even under metastability. Additionally, the digital 2's complement logic successfully compensates the code gap errors caused by inter-stage offset. The prototype ADC achieves an SNDR of 41.0 dB and consumes 2.8 mW at 0.9-GS/s conversion rate with Nyquist input.

Acknowledgment

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