A 16 × 16 D-Band Reflection Amplifier Based Active Reflectarray for Multi-Gb/s NLOS Links

Yasir Shafiullah[#], Olli Kursu[#], Duy Tung Phan[#], Janne Aikio[$], Marko E. Leinonen[#], Mikko Hietanen[#], Timo Rahkonen[$], Ping Jack Soh[#], and Aarno Pärssinen[#]
[#]Centre for Wireless Communications, [$]Circuits and Systems, University of Oulu, Finland

***Abstract*—High data rate requirements in 6G systems have driven the use of sub-THz bands, where wireless links suffer from severe path loss and blockage. Active reflectarrays (ARAs) offer a promising solution for enabling non-line-of-sight (NLOS) links and improving coverage, but their implementation remains challenging due to integration complexity, power constraints, and scalability. This work demonstrates a scalable 2D 16 × 16 ARA operating in the D-band (155 GHz), using on-chip reflection amplifiers integrated with an LTCC antenna array. Each 22 nm FDSOI chip interfaces with four antenna elements. Experimental validation in an NLOS reflection configuration shows up to 5 dB of relative gain over passive operation. To evaluate the ARA in a sub-THz link, the array amplifies and reflects a 64-QAM modulated signal at different round-trip distances. At 0.7 m, the array improves the EVM from 7.8% (passive) to 6.6% (active) at a data rate of 8.4 Gb/s. At 1.1 m, it supports a 6 Gb/s link with 7.2% EVM, while consuming only 11 mW per element. To the author's knowledge, this is the first reflection-amplifier-based active reflectarray to demonstrate multi-Gb/s D-band NLOS links with improved EVM.**

***Keywords*—Active reflectarray, reflection amplifier, D-band, sub-THz, LTCC antenna array, non-line-of-sight communication.**

I. Introduction

Reliable coverage at mmWave and sub-THz frequencies remains challenging due to severe path loss and high sensitivity to blockage, which often limits practical deployments to line-of-sight (LOS) conditions. Creating reliable non-line-of-sight (NLOS) paths is therefore important for extending coverage and improving link robustness at D-band and beyond. Active relay style architectures based on LNA-to-PA chains with dedicated TX/RX antennas can provide strong link gain, but they typically incur larger silicon area, higher DC power, and scaling complexity when extended to large 2D arrays [1]–[4]. These trade-offs motivate alternative active surface implementations that can enhance link margin with lower per-element power and simpler integration with gain enhancement compared to passive counterparts.

Reflection amplifier (RA) based active reflectarrays offer a compact single-port approach by providing gain through controlled negative resistance, enabling the use of a shared antenna aperture for reception and re-transmission as demonstrated in Fig. 1. While RA concepts have been explored at lower frequencies [5], [6], their extension to D-band is not straightforward for low-power, scalable NLOS link enhancement. The present prototype focuses on link enhancement rather than full beam steering. Accordingly, the measurements emphasize NLOS reflection gain and data-link improvement under a fixed illumination geometry.

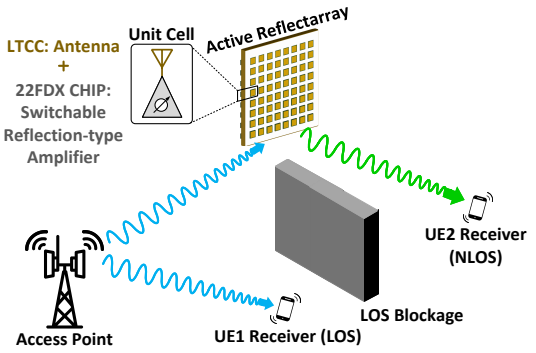


Fig. 1. Illustration of the active reflectarray based on reflection amplifiers

In this work, a 16 × 16 LTCC-integrated D-band active reflectarray operating around 155 GHz is demonstrated using low-power 22-nm FDSOI CMOS RA chips. In contrast to relay-style TX/RX surfaces, the proposed single-port RA-based architecture provides a compact and power-efficient alternative while still enabling measured 64-QAM multi-Gb/s NLOS link enhancement. The system achieves low power consumption per element together with higher reflection gain and lower EVM compared to a passive configuration. Section II describes the active reflectarray design, while Section III presents the measurement results.

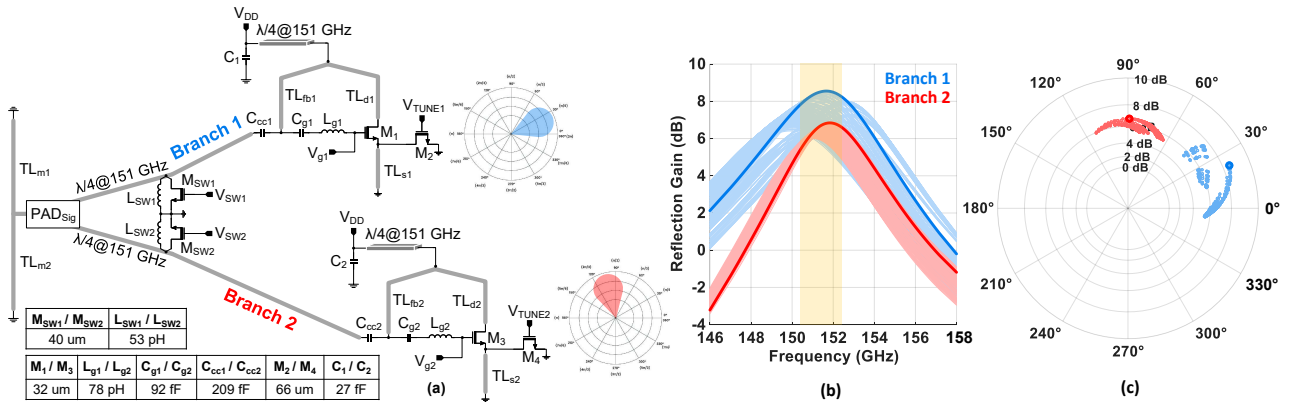
II. D-Band Active Reflectarray Implementation

A. Reflection Amplifier Circuit Design

Conventional amplifiers are two-port devices, whereas an RA is a single-port device that amplifies the reflected wave by presenting a negative resistance at its input. The reflection coefficient is defined as

$$\Gamma = \frac{Z_{\mathrm{amp}} - Z_{\mathrm{s}}^{*}}{Z_{\mathrm{amp}} + Z_{\mathrm{s}}} \tag{1}$$

where Z_{amp} denotes the input impedance of the RA and Z_{s} denotes the source (embedding) impedance presented to the RA. Reflection gain is obtained when the magnitude of the reflection coefficient exceeds unity ($|\Gamma| > 1$), which occurs when the real part of the RA input impedance is negative, $\Re\{Z_{\mathrm{amp}}\} < 0$. At the same time, self-oscillation is avoided as long as the total real part remains positive, $\Re\{Z_{\mathrm{amp}} + Z_{\mathrm{s}}\} > 0$. Stable RA operation requires that the negative-resistance condition is satisfied without meeting the oscillation startup criteria across process, voltage, and temperature corners. This negative-resistance condition can be realized using either cross-coupled transistor pairs [7] or



M_{SW1} / M_{SW2}	L_{SW1} / L_{SW2}
40 um	53 pH

M_1 / M_3	L_{g1} / L_{g2}	C_{g1} / C_{g2}	C_{cc1} / C_{cc2}	M_2 / M_4	C_1 / C_2
32 um	78 pH	92 fF	209 fF	66 um	27 fF

Fig. 2. (a) Schematic of the switchable reflection amplifier (SRA). (b) Simulated reflection gain versus frequency for Branches 1 and 2 under different tuning voltages (highlighted region marks the target operating range). (c) Simulated phase states of the reflected signal for the two branch selections at 151.5 GHz.

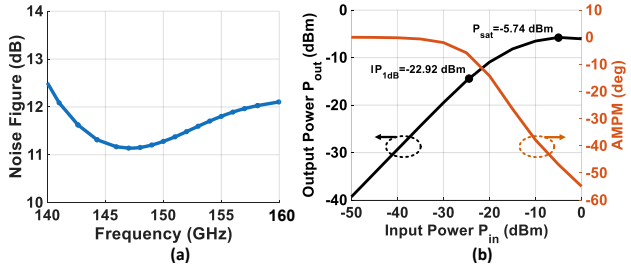


Fig. 3. Simulated at max gain configuration (a) Noise figure (b) Input referred 1 dB compression point, Psat and AMPM.

single-device negative-resistance topologies [5], [6]. Here in this paper single transistor based topology is utilized.

Reflection amplifiers often exhibit narrowband gain and a limited phase tuning range [5]–[7]. Previous work has demonstrated partial phase reconfigurability at D-band by tuning the negative impedance through transistor gate-voltage control [7], whereas switched-line phase shifters based on discrete components have been used to achieve full phase reconfigurability at lower frequencies [5]. However, at D-band, parasitic losses dominate, rendering switched-line phase-shifter implementations unsuitable for on-chip realization due to significant gain degradation. Hence, the proposed architecture is designed to offer a balanced compromise between gain and phase tuning. Fig. 2(a) shows the schematic of the switchable reflection amplifier (SRA). A single RF pad is split into two selectable branches, each connected to a dedicated RA. Path selection is realized using quarter-wave transmission lines together with frequency-tuned inductive switch networks ($\mathrm{M_{SW_1}/L_{SW_1}}$ and $\mathrm{M_{SW_2}/L_{SW_2}}$). The switches exhibit an OFF impedance of approximately 610 Ω and an ON impedance of approximately 10.2 Ω. By enabling one switch network at a time, the circuit selects the corresponding branch and activates the associated RA. The two branches incorporate different electrical line lengths, introducing an additional phase offset of approximately 50° between the two paths seen at the RF pad.

Each branch employs a negative-resistance core transistor (M1 in Branch 1 and M3 in Branch 2). The source transmission line $\mathrm{TL_{s1}}$ is used to set the effective negative resistance, while the drain and feedback transmission-line paths ($\mathrm{TL_{d1}}$ and $\mathrm{TL_{fb1}}$) are tuned to mitigate undesired self-oscillation and improve stability. Transistor M2 is placed in parallel with $\mathrm{TL_{s1}}$. By adjusting V_{tune1}, the effective source impedance is modified, enabling phase tuning while maintaining reflection gain. The operating frequency is adjusted through L_g and C_g. AC-coupling capacitors C_{cc1} and C_{cc2} are placed in both branches. With this configuration, the circuit can switch between two paths, achieving a simulated reflection gain of 5–8.5 dB at 151.5 GHz across different tuning voltages, as shown in Fig. 2(b). The two branches provide distinct phase states with an overall phase coverage below 120°, as summarized in Fig. 2(c) for V_{tune1} and V_{tune2}. The simulated noise figure in the maximum-gain configuration is approximately 11.4 dB, and the simulated input-referred P_{1dB} at 151.5 GHz is −22.9 dBm, as shown in Fig. 3(a) and (b). The circuit operates from a nominal 0.8 V supply and is EM simulated using Cadence EMX.

B. Prototype and Packaging

The SRA is implemented in a 22-nm FDSOI CMOS process, while the antenna array is realized on an 8-layer Ferro A6M-E LTCC stack with an overall thickness of approximately 650 μm. The LTCC substrate, with a relative permittivity of approximately 6 at the D-band, is selected for the antenna design due to its low-loss characteristics at high frequencies (loss tangent of 0.002). The antenna is a single-polarized patch antenna employing a capacitive feed to compensate for the parasitic inductance introduced by the thick feed via traversing the LTCC stack. Full-wave EM results obtained using CST Studio Suite indicate that the antenna achieves a wide impedance bandwidth from 132 to 166 GHz.

The flip chip IC with solder bumps and the LTCC antenna were co-simulated with Cadence Clarity to verify good matching, which is important for active reflectarrays. Oscillations can occur if the sum of the RA gain (including all the transmission line and antenna feed line losses) and the S11 is larger than 0 dB. In the EM model, ports are placed at the

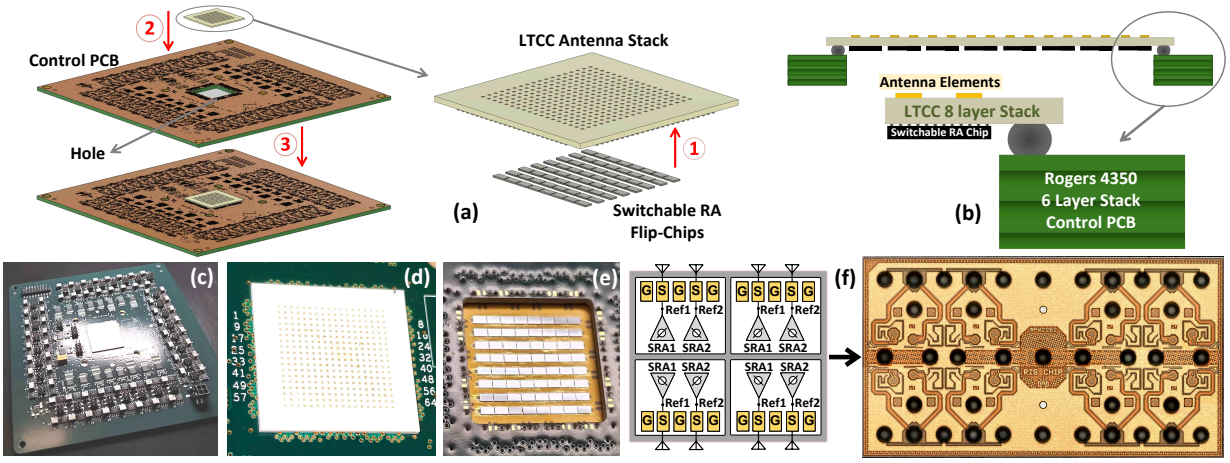


Fig. 4. System implementation of the 16×16 active reflector array. (a) 3D integration concept. (b) Cross-sectional stack-up. (c) Assembled module. (d) Front-side LTCC antenna. (e) Back-side integration of 64 CMOS RA chips. (f) 22-nm FDSOI chip block diagram and micrograph (1 x 1.82 mm).

ends of Branch 1 and Branch 2 on the RA side in Fig. 2 and matching with the antenna is co-simulated to be better than -11 dB over the entire band. Shorted symmetrical transmission line stubs $\mathrm{TL_{m1}}$ and $\mathrm{TL_{m2}}$ are used for matching at the GSG pads on the IC side.

The system-level integration is illustrated in Figs. 4(a) and (b). 64 flip-chip-mounted CMOS dies are assembled onto the backside of the LTCC antenna stack. The LTCC with integrated dies is BGA bonded to the control PCB, as shown in Fig. 4(c). The 16×16 LTCC antenna array is located on the front side (Fig. 4(d)), while the 64 ICs are mounted on the back side (Fig. 4(e)). Each chip occupies an area of $1.82\,\mathrm{mm}^2$ with four RA blocks that interface with four antenna elements. Each RA block provides two feed ports (Ref1 and Ref2), as shown in Fig. 4(f) to support phase-selectable operation on the antenna side whereas in this prototype, only the Ref1 port is utilized and connected to the antenna network. SPI buses are used for digital control.

III. Measurement Results

A. Reflectivity and Gain Measurements

The gain measurements were performed using a Keysight N5244B PNA-X with WR6.5 frequency extender modules for both the transmit and receive paths. Two horn antennas were used for the over-the-air (OTA) setup, shown in Fig. 5(a) and Fig. 5(b). For angular radiation-pattern measurements, the DUT was kept stationary, and both the TX and RX antennas were positioned in the far-field region. The TX antenna was fixed at $+16^\circ$ relative to the reflectarray boresight, while the RX antenna was rotated around the DUT to measure the angular response. After chip integration with the antenna array, the operating frequency shifted from the simulated 151.5 GHz to approximately 155 GHz $(+2.3\%)$. At this frequency, the array was measured in both the active and passive states. In the active state all elements were activated by turning on the RAs whereas in the passive state they were turned off. When Branch 1 and Branch 2 were activated individually, reflection gains of $4.2\,\mathrm{dB}$ and $4.5\,\mathrm{dB}$, respectively, were measured

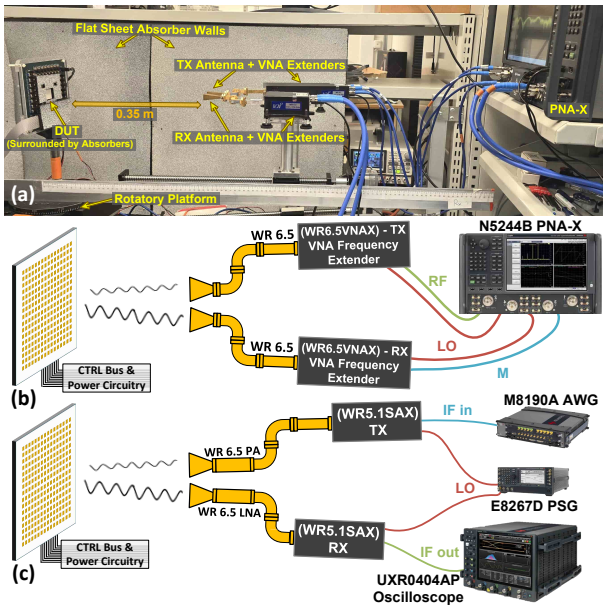


Fig. 5. Prototype measurement setups: (a) photograph of the over-the-air (OTA) S-parameter measurement setup, (b) corresponding block diagram, and (c) modulated-signal measurement setup.

relative to the passive case, as shown in Fig. 6, with only 11 mW per element. The result agrees well with simulation after accounting for 1.7 dB of two-way LTCC routing loss.

B. Modulated Signal Measurements

Keysight UXR0404AP oscilloscope with Spectrum Analyzer Extension Modules (SAX) covering the WR5.1 band was used for modulated measurements. The E8267D PSG and M8190 AWG were used for signal generation and were connected to the SAX/oscilloscope receiver. A WR6.5 PA and a WR6.5 LNA were used at the TX and RX, respectively. The complete measurement setup is shown in Fig. 5(c). The NLOS link performance of the active

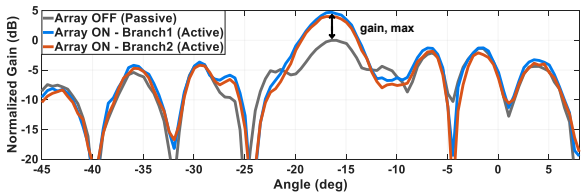


Fig. 6. Measured angular scattered-wave pattern at 155 GHz.

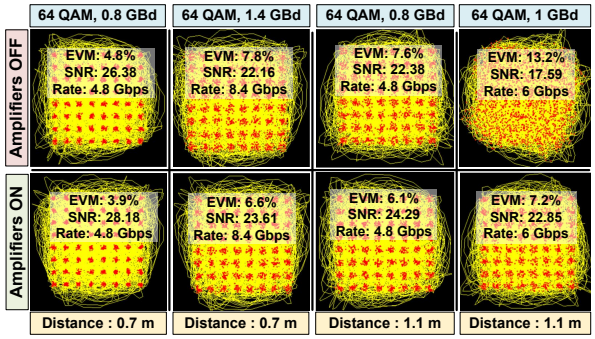


Fig. 7. Measured 64-QAM NLOS link at 0.7 and 1.1 m: passive vs. active

reflectarray was evaluated using a 64-QAM waveform at baud rates of 0.8, 1, and 1.4 Gbaud. Measurements were performed at total reflective link distances of approximately 0.7 m and 1.1 m. The measured EVM, SNR, and constellations are shown in Fig. 7. Activating the reflectarray consistently improves the link quality and reduces EVM by more than 1% under comparable conditions, while enabling reliable reception at higher baud rates. A maximum throughput of 8.4 Gb/s was achieved at a 0.7 m NLOS link distance. At the longer 1.1 m distance, the link degrades severely in the array OFF state at 1 Gbaud, whereas activating the array restores the link and enables a data rate of approximately 6 Gb/s (Fig. 7). These results highlight the benefit of the proposed active reflectarray in improving D-band NLOS link.

Table I compares state-of-the-art active and passive reflectarrays, including CMOS relay-style systems. This work achieves low DC power per element among the listed active implementations while providing approximately 4-5 dB of measured relative link-gain improvement in NLOS operation. 64-QAM measurements further demonstrate up to $8.4\,\mathrm{Gb/s}$ at a $0.7\,\mathrm{m}$ round-trip NLOS distance and $6\,\mathrm{Gb/s}$ at $1.1\,\mathrm{m}$ with the array activated having improved EVM and link robustness compared to the passive configuration. In this work, the single-port SRA and antenna interface matching limits the achievable gain, while two-port relay architectures have better TX–RX isolation to reach higher link gain. Although the proposed switchable RA architecture improves the phase range, the available phase tuning remains limited and therefore constrains the beam-steering capability.

IV. Conclusion

A scalable 16×16 active reflectarray operating around $155\,\mathrm{GHz}$ is demonstrated using 22-nm FDSOI CMOS RAs integrated with an LTCC antenna array. The prototype array provides approximately 4–5 dB of relative reflection gain enabling NLOS operation and supports 64-QAM links up to $8.4\,\mathrm{Gb/s}$ at a distance of $0.7\,\mathrm{m}$ NLOS, consuming only $11\,\mathrm{mW}$ per element. To the best of our knowledge, this is the first demonstration of an RA-based architecture supporting high-data-rate NLOS links with improved EVM in an NLOS scenario. This architecture offers a promising route towards compact and energy-efficient solutions, while improving sub-THz NLOS links for future wireless systems.

TABLE I
Comparison of State-of-the-Art Reflectarray Works

Param.	This work		ISSCC'25 [1]	RFIC'22 [2]	ISSCC'22 [8]	TMTT'17 [7]
Freq (GHz)	155		120	60	260	115-125
Technology	22nm FDSOI		22nm FDSOI	65nm CMOS	22nm CMOS	28nm FDSOI
Surface Type	Active		Active	Active	Passive	Active
Architecture	RA based		PA/LNA relay	PA/LNA relay	Switch based	RA based
Array Size	16×16		4×4	2x2	98x98	2x2
Antennas	On-LTCC		On-Chip	On-PCB	On-Chip	On-PCB
2D Scalability	Yes		Yes	Yes	Yes	Yes
Gain (dB)[§]	4–5		23.6	15	-3	14
NF (dB)[§]	11.4*		7.3	6.1	N/A	10.5–11.7
Psat (dBm)[§]	-5.7*		6.8	4.2	N/A	N/A
PDC (mW)[§]	11		100	55	0.1	6-20
Area (mm^2)[§]	0.45		1.56	1	0.32	0.305
Modulation	64QAM		64QAM	QPSK	N/A	N/A
Data rate	8.4 Gb/s	6 Gb/s	6 Gb/s	400 Mb/s	N/A	N/A
EVM	6.6%	7.2%	5%	9.44%	N/A	N/A
Link Distance[‡]	0.7 m	1.1 m	1.3 m	N/A	N/A	N/A

[‡]Round-trip distance, [§]Per element. *Simulated values.

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