A 12V-compliant Startup Rectifier for Current-Mode Receivers Achieving Triple-Supply Charging at 47× Lower Power

Amin Rashidi[1], Jesse Pasterkamp[1], Mario Konijnenburg[1], Wensi Wang[2], Nick Van Helleputte[3], Stefano Stanzione[1]
[1]*imec-Netherlands, Eindhoven, The Netherlands,* [2]*SuperVision (Beijing) Ltd, Beijing, China,* [3]*imec, Leuven, Belgium*
Email: Amin.Rashidi@imec.nl

Abstract— **This paper presents a 12V-compliant StartUp Rectifier (SUR) for current-mode wireless power receivers, enabling fast and reliable cold-start operation under extremely limited received powers. The proposed SUR incorporates a self-protected voltage multiplier with an adaptive voltage conversion ratio (VCR) ranging from 0.35 to 4, automatically adjusting to the AC voltage amplitude at the receiver (RX) coil. This adaptive behavior allows sufficient voltage build-up at RX amplitudes as small as 0.3 V to rapidly establish parallel resonance in the RX LC tank, while inherently limiting output levels to ensure safe operation at AC amplitudes up to 12 V. Fabricated in 130-nm BCD technology and occupying only 0.12 mm² of silicon area, the startup circuitry supports triple-output charging at 1.8 V, 5 V, and 12 V with as little as 9.2 mW at 6.78 MHz. This represents a 47× reduction in the required startup power compared to prior works based on series-resonance startup.**

Keywords—startup rectifier, wireless power receiver, current-mode rectification, cold-start circuit, multi-output power management.

I. Introduction

Miniaturized, batteryless neuromodulation implants reduce surgical trauma, extend operational lifetime, and lower system cost. The i-NYS system (Fig. 1, top) powered through inductive Wireless Power Transfer (WPT), and equipped with Bluetooth control, stimulates the extraocular rectus muscle, to treat congenital nystagmus. Such mm-scale multi-function implants require multiple supply rails with varying power demands and minimal off-chip components.

Voltage-Mode Rectifiers (VMRs) offer high Power Conversion Efficiency (PCE) [1-3] but fail to sustain the load voltage at low powers [2-3]. Current-mode rectifiers (CMRs) overcome VMR voltage thresholds by using LC tank current for energy delivery. Specifically, CMRs accumulate energy over multiple unloaded resonant cycles and subsequently transfer it to the output by breaking the resonance at the point of maximum coil current. Furthermore, CMRs support energy-efficient multi-level supply charging without off-chip matching or DC-DC converters [2-5]. Despite these advantages, CMRs conventionally target battery charging and lack cold-startup capability [6-8]. Starting from a fully discharged state presents two fundamental challenges for CMRs. First, a passive CMR is infeasible, since it relies on active circuits such as comparators and logic, making a VMR-based startup unavoidable for batteryless implants [2], [4], [9]. Second, CMRs need a resonance-breaking switch (S_{Res} in Fig. 1) in series to the RX tuning capacitor (C_{RX}). Failure to close S_{Res} during cold startup leads to a non-resonant condition with significantly lower Power Transfer Efficiency (PTE) and lower Power Delivered to the Load

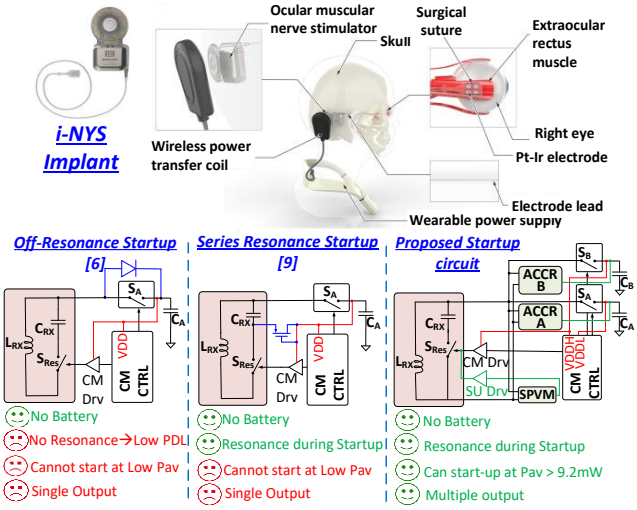


Fig. 1. (top) I-NYS implant for treating congenital nystagmus (bottom) SOTA and proposed startups for startup in current mode rectifiers.

(PDL). Therefore, as shown in the bottom of Fig. 1, non-resonant startup circuits demand significantly higher RX power and are often a long startup times due to low PDL (e.g., 58 s in [6]). Series resonance startup, as in [2], [4], [9], significantly improves PTE and PDL and thus startup speed. However, as shown in Fig. 2, only parallel resonance can sufficiently boost V_{RX} for passive charging of the outputs under low available power (P_{av}), which requires S_{Res} activation during startup. This work proposes a StartUp Rectifier (SUR) featuring a dedicated Self-Protected Voltage Multiplier (SPVM) for driving S_{Res} through positive feedback to quickly enable parallel-resonant charging during startup.

II. Architecture

Fig. 3 (top) illustrates the simplified block diagram of the full CMR, including the proposed SUR. The CMR generates three regulated supply rails —V_{DD1V8}, V_{DD5V}, V_{DD12V}—using a round-robin charging scheme to support all i-NYS functions. CMR logic allows V_{RX} to charge V_{DD12V} through a Schottky diode, which also charges the 12V rail during startup. Since the CMR relies on active circuits powered at 1.8V and 5V, SUR independently charges the rails before releasing Power-On Reset (POR) and initiating CMR operation. SUR consists of an SPVM followed by an SU Driver to close the S_{Res} switch, along with two AC-Coupled Rectifiers (ACCRs) for charging the supply rails (Fig. 3, bottom). With coil nodes (COILN/COILP) reaching up to 12 V to support V_{DD12V} charging, S_{Res} uses a 12V-rated

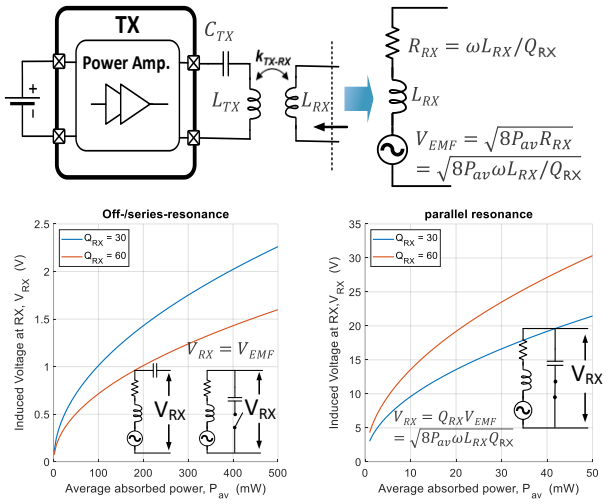


Fig. 2. (top) Simplified model link for weak coupling conditions, (bottom) V_{RX} for different off-, series- and parallel-resonance LC tank configurations for L=900uH and at frequency of 6.78MHz.

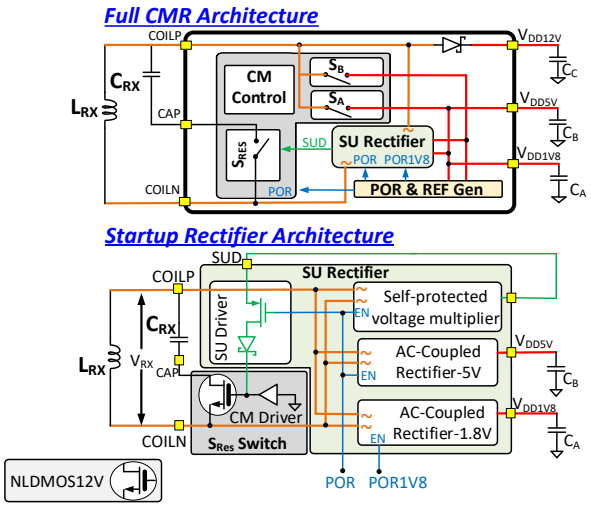


Fig. 3. (top) Full CMR architecture, (bottom) SUR block diagram.

NLDMOS device. The SU Driver bootstraps the S_{Res} gate leveraging its large gate-source capacitance. However, the NLDMOS employed for S_{Res} is limited to a 5V gate-to-source voltage rating; consequently, the DC output of SPVM at the SUD node must remain below 5 V to prevent device breakdown. To satisfy this requirement, the SPVM is designed with a tailored Voltage Conversion Ratio (VCR). A higher VCR (up to 4×) enables startup at V_{RX} as low as 0.3 V, while smaller-than-one VCRs prevent breakdown when V_{RX} reaches up to 12 V. Once resonance is established, ACCRs-coupled rectifiers charge the 1.8 V and 5V rails until POR signals disable them.

III. Circuit Implementation

Fig. 4 captures the implementation details of the proposed SPVM. The desired VCR profile of SPVM is designed by adopting a Differential-Drive Multiplier (DDM) architecture [10-11]. To minimize the required V_{RX} for the voltage boosting, 1.5-V LVT transistors are employed in a 6 stage DDM. After SPVM initiates the weak resonance by driving S_{Res}, the RX quality factor (QF_{RX}) rises, amplifying V_{RX} which in turn further increases the S_{Res} drive voltage through positive feedback (Fig. 4, bottom-right). To handle

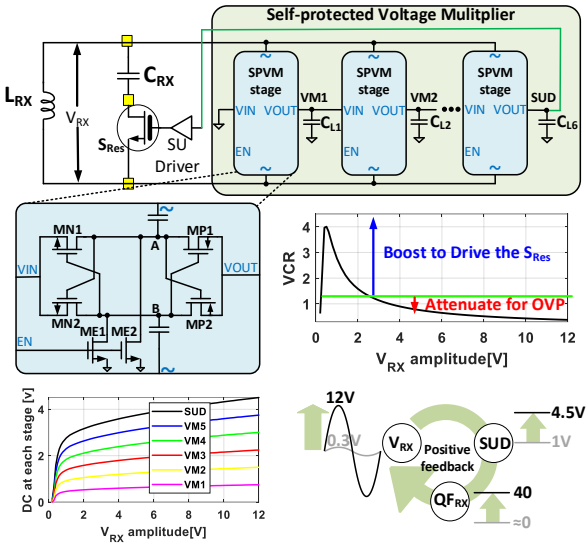


Fig. 4. (top) Schematic of SPVM and its VCR profile, (bottom) DC level at the output of each stage and illustration of Positive feedback.

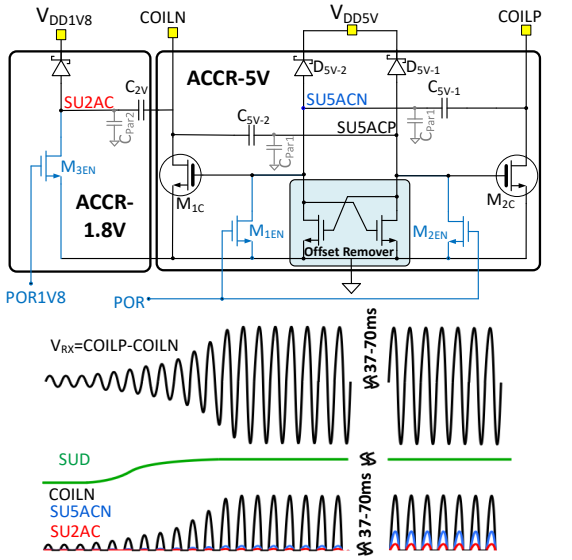


Fig. 5. (top) Schematic of AC-Coupled rectifiers (bottom) Important waveforms during startup.

high V_{RX} amplitudes, intrinsic reverse current of DDMs is leveraged to keep the voltage gain of each stage below the 1.5 V breakdown limit. Although the reverse current of DDMs is typically regarded as a drawback due to the associated efficiency loss, it does not pose a concern in this design, as the SPVM does not drive a significant resistive load. A 20-pF capacitor is added at the output of each stage of SPVM to suppress damaging voltage spikes.

The schematics of ACCR-1.8V and ACCR-5V are shown in Fig. 5. To avoid post-startup CMR efficiency degradation caused by excessive coil-nodes parasitics, V_{DD1V8} uses a half-wave ACCR (C_{2V}, D_{2V}). In contrast, V_{DD5V} employs full-wave rectification (C_{5V-1}, C_{5V-2}, D_{5V-1}, D_{5V-2}) and integrates ground commutation (M_{1C} and M_{2C}). M_{1C} periodically ties S_{Res}'s source to ground, enabling the bootstrap of the SU driver; without this mechanism, DC drift across the LC tank would require a gate voltage beyond the SPVM capability. Since the LDMOS devices cannot tolerate V_{GS}>5 V, the gates of M_{1C} and M_{2C} are AC coupled within ACCR-5V, and their AC swing is clamped by D_{5V-1}/D_{5V-2} to

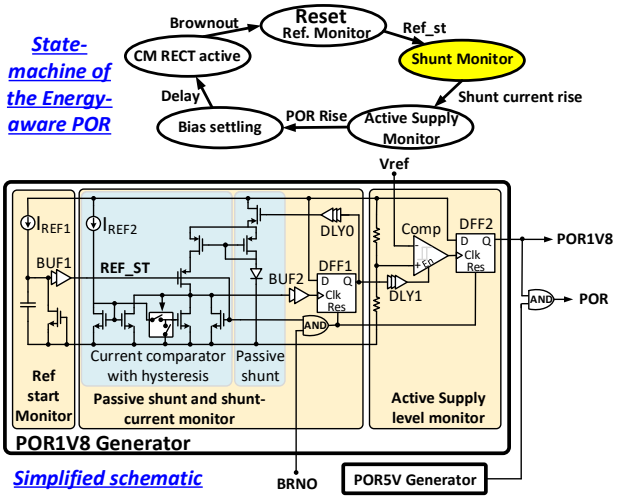
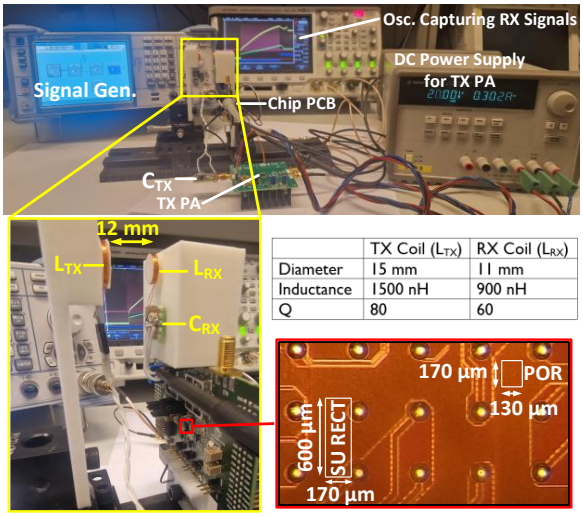


Fig. 6. (top) State machine, and (bottom) the simplified schematic of the implemented Energy-aware POR.



	TX Coil (L_{TX})	RX Coil (L_{RX})
Diameter	15 mm	11 mm
Inductance	1500 nH	900 nH
Q	80	60

Fig. 7. Photos of the measurement setup, and the fabricated chip.

the ACCR-5V's output plus one diode drop. ACCRs provide four benefits for SUR: (a) isolate DC levels for independent multi-rail charging; (b) clamp AC amplitude to each stage's DC output, enabling LV device ratings; (c) allow full disabling of ACCRs by shorting capacitors after POR; and (d) enable ground commutation. These benefits come at the cost of increased AC resistance introduced by the coupling capacitors in the startup power delivery path, which limits the maximum instantaneous power and, consequently, the startup speed. Fig. 5 (bottom) shows that SPVM aided by positive feedback drives the LC tank into full resonance within 100-300 µs, saturating V_{RX} and SUD. During the next 37–70 ms required to charge the µF-level storage capacitors, SU2AC and SU5ACN remain clamped to one diode drop above their ACCR output level.

Fig. 6 shows the POR circuit, where a passive shunt provides overvoltage protection until the reference generator settles. This approach protects downstream circuits in a batteryless system where startup is repeatedly invoked under varying coil-alignment conditions. A hysteresis-equipped current comparator monitors the shunt current to ensure sufficient overhead power. This energy-aware approach prevents immediate Brown-Out (BRNO) and POR–BRNO oscillations during startup or shortly after POR.

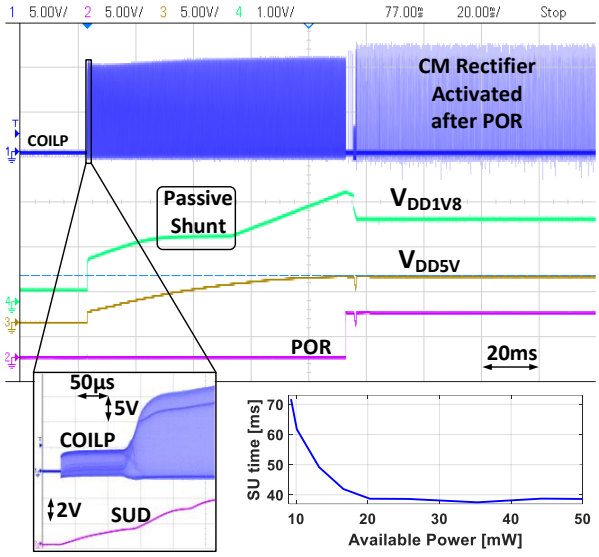


Fig. 8. Measured transient waveforms, and startup time vs. power.

IV. Measurement Results

The proposed circuits are fabricated in a 130 nm BCD technology and are successfully validated using the setup shown in Fig. 7, with 12-mm TX-RX coil separation. Fig. 8 shows transient measurements of the proposed SUR, achieving startup with only 9.2 mW available power at 6.78 MHz. Positive feedback drives SUD and V_{RX} concurrently, bringing the LC tank to full resonance within 250 µs. Due to low power, the energy-aware POR circuit holds V_{DD1V8} in passive shunt for ~30 ms; after 70 ms, both rails reach target levels, POR is released, and SUR is disabled. After a short bias-settling delay, the main CMR takes over. Startup time ranges from 37–70 ms for 9.2–50 mW is shown in Fig. 8, bottom-right. Fig. 9 compares V_{RX} across power levels with the test switch (S_{test}) open or closed between SPVM output and the SUD node. With S_{test} open (off-resonance startup), V_{RX} remains insufficient even at 100 mW; when closed as proposed, resonance and positive feedback boosts V_{RX} above 5 V even at 2 mW. Loop gain is measured at ~1mW available power by opening the loop at SUD and applying DC to the SU driver while monitoring SPVM output (Fig. 10). Gain > 1 for SUD at 1–3 V confirms positive feedback.

Table I compares this work with the recently reported self-startup CMRs. Since prior works do not report the minimum P_{av} required for self-startup, and because P_{av} depends on the coil inductance, quality factor, and link frequency (Fig. 2), a direct comparison is challenging. To enable a fair comparison with passive series-resonant startup circuits in [2], [4], and [9], a series-resonant rectifier using BAT40 Schottky diodes is implemented and measured in the same measurement setup as the proposed chip. The proposed SUR achieves triple-output charging with P_{av}=9.2 mW, which is 47× less than the series resonance approach. Although the ACCR's AC resistance increases startup time in this work, the proposed approach achieves a 10× smaller startup-circuit area than the other HV-compliant design in [5] by using LV devices. In contrast, [5] uses HV LDOs, HV bandgap references, and bulky power switches to charge the 1.8 V and 4.5 V supply rails during startup.

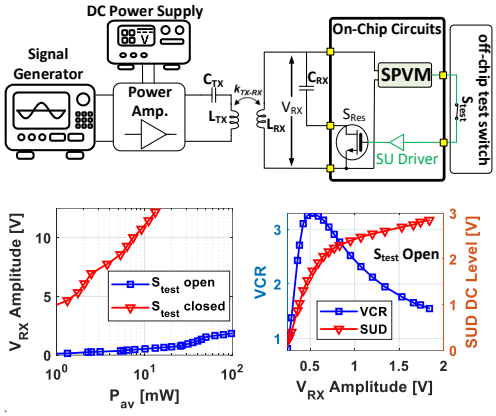


Fig. 9. (top) Measurement setup. (bottom left) V_{RX} Versus Pav for open and closed S_{test}.(bottom right) VCR and DC level at SUD when S_{test} open.

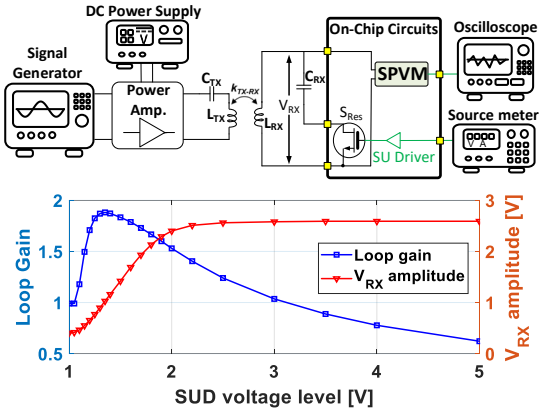


Fig. 10. Loop gain measurement at $P_{av}\cong$1mW by opening the loop at SUD and applying DC to the SU driver while monitoring SPVM output.

TABLE I. Comparison with state-of-the-art

	This work	*Mimicking series res. SU*	*[9] JSSC 2017*	*[2] JSSC 2026*	*[4] TCAS-I 2023*	*[5] JSSC 2022*	*[6] TCAS-II 2020*
Tech. [nm]	130 BCD	COTS*	350	180 BCD	180	180 BCD	180
WPT Method	CM	VM	Hybrid	Hybrid	CM	CM	CM
RX res. mode	parallel	series	parallel	series	series	parallel	parallel
Application	Batt. free stim	Fair comp.	Batt. free implants	Retina implant	NA	RF-US relay	battery charge
Self-startup	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Startup strategy	SPVM + ACCRs	Series res.	Series res.	Series res.	Series res.	HV SU LDOs	Off res.
V_O at SU [V]	12, 5, 1.8	3.4	2V	1.2, 2	1.2	32, 4.5, 1.8	1.2
V_O Comp. [V]	12	5	3.3	2	3	29	1.2
No. of V_O	3	1	1	2	2	3	1
Freq. [MHz]	6.78	6.78	1	40.68	6.78	40	13.56
L_{RX} radius [mm]	5.5	5.5	15	4	1.15	24	12.5
Min P_{av} [mW]	9.2	430†	NA	NA	NA	NA	NA
SU time [ms]	37-70	0.1-0.2	4.2	0.3	0.8	0.24	58000
SU Area (mm^2)	0.12	NA	NA	0.13§	NA	1.2§	NA

* Replicating the series-resonance SUR similar to [9],[2] and [4] using BAT40 Schottky diodes § Estimated from the floorplan figure
† 430 mW for V_{Rect}= 3.4V (minimum required for the startup of the designed 12V- compliant CMR), and 140mW for V_{Rect}=1.8V

V. Conclusion

A triple-output startup rectifier for current-mode WPT receivers under limited RX power is presented. The proposed SPVM and SU driver circuits boost V_{RX} amplitudes from 300 mV to directly drive a 12V-rated resonant switch, thereby enabling rapid and safe initiation of parallel resonance through positive feedback. After resonance is established, two ACCR circuits simultaneously and independently charge output rails with a small area overhead of 0.12 mm². Implemented in a 130 nm BCD process, the prototype delivers 1.8 V, 5 V, and 12 V rails with a minimum available power of 9.2 mW and a startup time of 37–70 ms, thereby alleviating the startup burden compared with series-resonant approaches and enhancing robustness for compact batteryless receivers.

References

[1] A. Rashidi, K. Laursen, S. Hosseini, H.-A. Huynh, and F. Moradi, "An Implantable Ultrasonically Powered System for Optogenetic Stimulation with Power-Efficient Active Rectifier and Charge-Reuse Capability," *IEEE Trans. Biomed. Circuits Syst.*, vol. 13, no. 6, pp. 1362–1371, Dec. 2019, doi: 10.1109/TBCAS.2019.2949154.

[2] T. Lu and S. Du, "A 40.68-MHz Dual-Output Wireless Power Transfer System for Millimeter-Scale Biomedical Implants," *IEEE J. Solid-State Circuits*, vol. 61, no. 3, pp. 963–976, Mar. 2026, doi: 10.1109/JSSC.2025.3617375.

[3] Y. Ou-yang *et al.*, "A 40.68-MHz Fully-Integrated Voltage/Current-Mode Dual-Output PMU for Wireless Neural Implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 20, no. 1, pp. 41–56, Feb. 2026, doi: 10.1109/TBCAS.2025.3591228.

[4] D.-H. Yao, T.-N. Liu, M. Takamiya, and P.-H. Chen, "A 6.78-MHz Wireless Power Transfer System With Dual-Output Resonant Current-Mode Regulating Rectifier and Transmission Power Regulation," *IEEE Trans. Circuits Syst. I*, vol. 70, no. 12, pp. 4986–4998, Dec. 2023, doi: 10.1109/TCSI.2023.3299865.

[5] E. So, P. Yeon, E. J. Chichilnisky, and A. Arbabian, "An RF-Ultrasound Relay for Adaptive Wireless Powering Across Tissue Interfaces," *IEEE J. Solid-State Circuits*, vol. 57, no. 11, pp. 3429–3441, Nov. 2022, doi: 10.1109/JSSC.2022.3171233.

[6] C.-J. Kuo and S.-I. Liu, "A 13.56 MHz Current-Mode Wireless Power Receiver With Energy-Investment Capability," *IEEE Trans. Circuits Syst. II*, vol. 67, no. 2, pp. 205–209, Feb. 2020, doi: 10.1109/TCSII.2019.2905279.

[7] S.-H. Lee *et al.*, "Voltage-Boosted Current-Mode Wireless Power Receiver for Directly Charging a Low-Voltage Battery in Implantable Medical Systems," *IEEE Trans. Ind. Electron.*, vol. 66, no. 11, pp. 8860–8865, Nov. 2019, doi: 10.1109/TIE.2018.2873525.

[8] H. S. Gougheri and M. Kiani, "Current-Based Resonant Power Delivery With Multi-Cycle Switching for Extended-Range Inductive Power Transmission," *IEEE Trans. Circuits Syst. I*, vol. 63, no. 9, pp. 1543–1552, Sep. 2016, doi: 10.1109/TCSI.2016.2579258.

[9] H. Sadeghi Gougheri and M. Kiani, "Self-Regulated Reconfigurable Voltage/Current-Mode Inductive Power Management," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3056–3070, Nov. 2017, doi: 10.1109/JSSC.2017.2737138.

[10] K. Kotani, A. Sasaki, and T. Ito, "High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3011–3018, Nov. 2009, doi: 10.1109/JSSC.2009.2028955.

[11] G. Chong *et al.*, "CMOS Cross-Coupled Differential-Drive Rectifier in Subthreshold Operation for Ambient RF Energy Harvesting—Model and Analysis," *IEEE Trans. Circuits Syst. II*, vol. 66, no. 12, pp. 1942–1946, Dec. 2019, doi: 10.1109/TCSII.2019.2895659.