A 56-Gb/s 60-GHz CMOS Broadband Linear Bi-Directional Amplifier Supporting Large-Scale B5G/6G Phased-Array Transceivers

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***Abstract*—This article presents a broadband linear differential bi-directional amplifier targeting 60-GHz large scale phased-array transceiver applications. To achieve compact integration, the transmitting (Tx) and receiving (Rx) paths share a common matching network (M.N.), while the gate–drain capacitance of the off-mode transistor functions as a neutralization capacitor to enhance gain and stability in both Tx and Rx modes. Furthermore, peaking inductors are introduced at each transistor gate to align the required source and load impedance of the Tx and Rx paths, thereby simplifying the M.N. design and improves linearity. Implemented in 65 nm CMOS process, the proposed bi-directional amplifier delivers a saturated output power of 10.5 dBm and achieves an output 1 dB compression point (OP_{1dB}) of 8.3 dBm at 64-GHz in Tx mode, consuming 103 mW under a 1-V supply. In Rx mode, an input 1 dB compression point (IP_{1dB}) of -10.1 dBm and a minimum noise figure (NF) of 5.1 dB is achieved, with 78mW power consumption. Under 16-QAM OFDM modulation with a 14-GHz bandwidth, a maximum data rate of 56 Gb/s is demonstrated, verifying its effectiveness in compact and high-speed 60-GHz phased-array front ends.**

***Index Terms*—Millimeter-wave, CMOS, Bi-directional, Amplifier, Broadband, Transceiver, Fifth-Generation (5G), Beyond 5G (B5G), Sixth-Generation (6G).**

I. Introduction

The unlicensed 60-GHz millimeter-wave (mmW) band offers up to 14 GHz of continuous bandwidth, positioning it as a key enabler for B5G/6G multi-gigabit short-range communications [1], [2], [3], [7]. To compensate for the severe free-space path loss at this frequency, large-scale phased-array architectures have become indispensable [1], [4], [5], [6]. Integrated 4, 8 or 16 elements within one single chip has been a commonly adopted configuration.

In large-scale phased-array transceivers, such as 16-channels within a single chip, the passive distribution network—including a four-stage power divider and routing paths—imposes over 20 dB of aggregate insertion loss between the common node and each RF element. In Tx mode, the driver amplifier preceding this network must therefore deliver an OP_{1dB} exceeding 8 dBm to maintain sufficient equivalent isotropic radiated power (EIRP), while providing adequate linearity margins for high peak-to-average power ratio (PAPR) modulations such as 64-QAM. Conventional

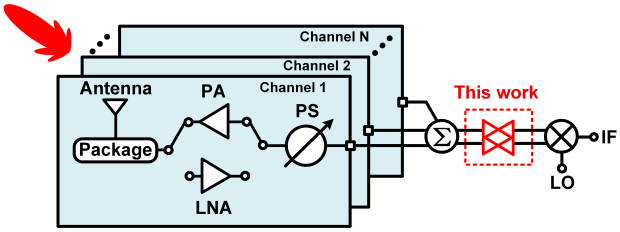


Fig. 1: (a) Bi-directional amplifier in a mmW transceiver.

solutions employ on-chip T/R switches with separate Tx and Rx M.N., but at 60 GHz in 65-nm CMOS process, a series–shunt switch typically introduces 2–3 dB of insertion loss, demanding higher driver output power and hence greater DC consumption under a stringent 1-V supply. Moreover, the duplicated M.N. double the silicon footprint, conflicting with the strict half-wavelength spacing ($\approx$ 2.5 mm) required at 60 GHz.

This work presents a compact differential bi-directional amplifier targeting large-scale 60-GHz phased-array transceivers, as shown in Fig. 1. The Tx and Rx paths share a common M.N., while a self-neutralization mechanism—simply realized with a single cross section at the drain of Tx transistors—enhances gain and stability without additional passive components. Series peaking inductors at the transistor gates further realign the divergent Tx/Rx optimal impedance to make better matching. Implemented in 65-nm CMOS process, the three-stage amplifier achieves a measured OP_{1dB} of 8.3 dBm (Tx mode) and IP_{1dB} of -10.1 dBm (Rx mode) with a core area of 0.25 mm^2. Wideband measurements confirm a 56-Gb/s data rate with 16-QAM over 14-GHz bandwidth. Section II describes the circuit design, Section III presents measurement results, and Section IV concludes this work.

II. Proposed Bi-Directional Amplifier Design

A. Self-Neutralized Bi-Directional Core

Conventional TRx front-ends employ on-chip T/R switches to alternate between Tx and Rx modes, requiring separate matching networks for each path. The neutralized bi-directional amplifier topology is first introduced in [9],

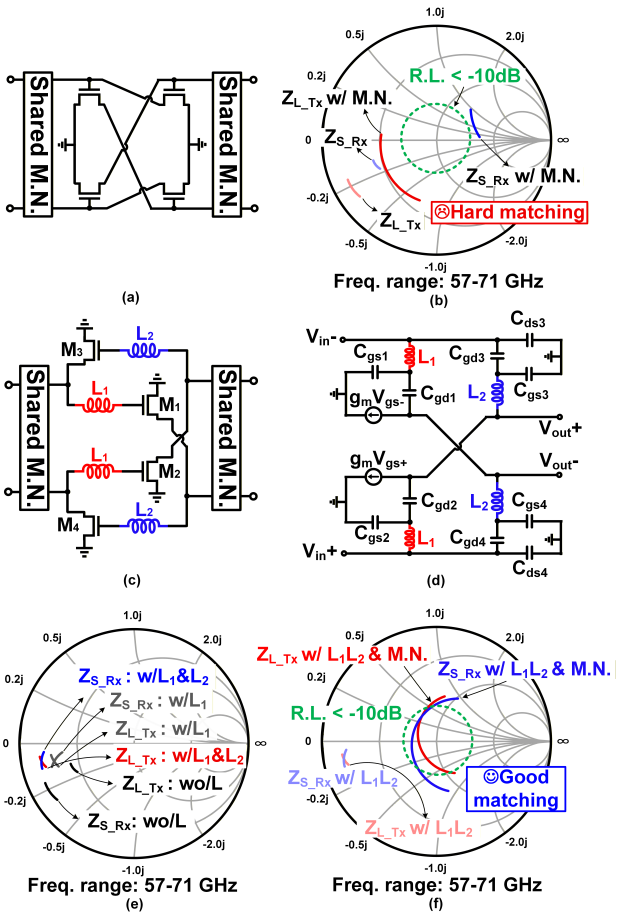


Fig. 2: (a) Conventional neutralized bi-directional core [9]; (b) Impedance matching situation for Z_{L_Tx} and Z_{S_Rx} in the conventional bi-directional core; (c) Proposed neutralized bi-directional core with peaking inductors for impedance alignment; (d) Tx mode small signal equivalent circuit of the proposed bi-directional core; (e) Impedance alignment effect of Z_{L_Tx} and Z_{S_Rx} with peaking inductor L_1 and L_2; (f) Impedance matching situation after impedance alignment.

which is shown in Fig. 2(a). It eliminates the T/R switch by sharing one M.N. for both Tx and Rx transistors, saving approximately 50% of silicon area. When identically sized Tx and Rx transistors are used, the neutralization condition is inherently satisfied, suppressing reverse feedthrough and improving both gain and stability.

The present work extends this topology to 60-GHz with three main differences. First, series peaking inductors are introduced at the transistor gates to realign the divergent Tx/Rx optimal impedance for a shared M.N.; their design and benefits are detailed in Section II-B. Second, mode selection is performed by gate-bias switching rather than tail-current switching, eliminating the voltage headroom consumed by tail transistors. Third, the differential neutralization path is realized simply by placing two single-ended bi-directional cores side

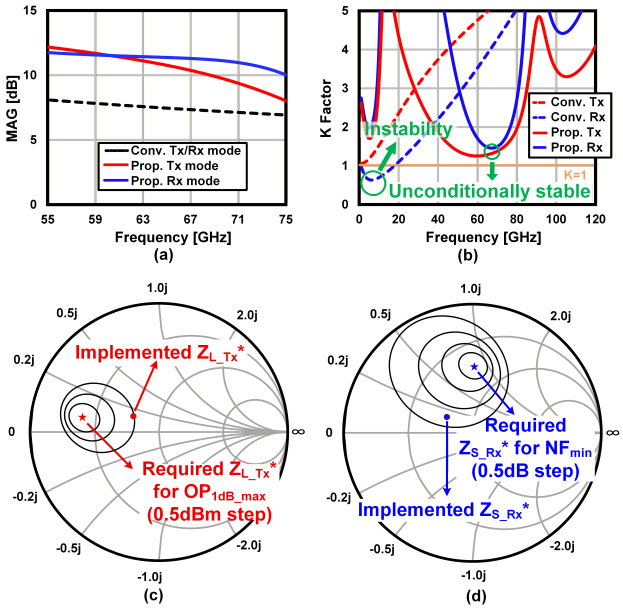


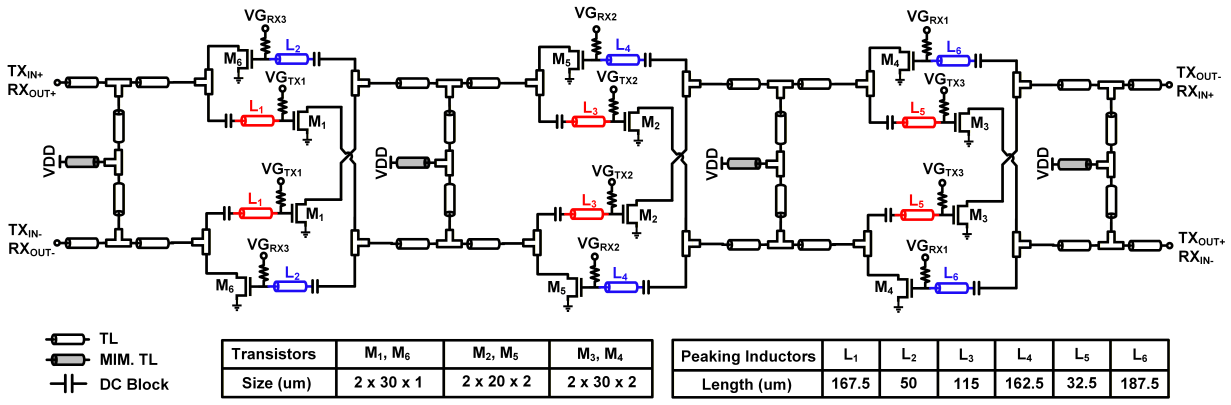
Fig. 3: (a) Comparison of Tx/Rx MAG between conventional core and proposed core; (b) Comparison of stability between conventional core and proposed core; (c) Tx mode $Z^*_{L\_Tx}$ and (d) Rx mode $Z^*_{S\_Rx}$ created by L_1 and L_2 at 64-GHz.

by side and crossing the inner-side drain connections, without any custom-drawn layout structures. This straightforward implementation allows the entire circuit to be constructed exclusively from in-house characterized standard unit cells and provides high-confidence simulation-to-measurement correlation at the target frequency band.

B. Peaking Inductors

To share the M.N. between Tx and Rx paths, the source impedance for the Tx mode (Z_{S_Tx}) and the load matching impedance for the Rx mode (Z_{L_Rx}) must be closely aligned, or higher return loss (R.L.) will be introduced to either path, and vice versa for Z_{L_Tx} and Z_{S_Rx}. Fig. 2(c) are shown as an example of the bi-directional core with a size of $120\mu m$, the Z_{L_Tx} and Z_{S_Rx} are widely separated without peaking inductors.

To resolve this issue, peaking inductors L_1 and L_2 are introduced exclusively at the gates of Tx/Rx transistors in series, to pull Z_{S_Tx} and Z_{L_Rx} clockwise on the Smith chart. Schematic of the proposed core is shown in Fig. 2(a) and its small signal equivalent circuit is shown in Fig. 2(b). As depicted in Fig. 2(c), this mechanism successfully aligning Z_{S_Tx} and Z_{L_Rx} much closer. Similarly, the series inductor L_2 pulls the Z_{L_Tx} and Z_{S_Rx} closer on the Smith chart. As shown in Fig. 2(d), with a shared M.N., load matching of Tx mode and source matching of Rx mode can be both matched into the circle where R.L. is less than -10 dB. While without proposed technique, R.L. can hardly goes under -10 dB for both paths.



Transistors	M_1, M_6	M_2, M_5	M_3, M_4
Size (um)	2 x 30 x 1	2 x 20 x 2	2 x 30 x 2

Peaking Inductors	L_1	L_2	L_3	L_4	L_5	L_6
Length (um)	167.5	50	115	162.5	32.5	187.5

Fig. 4: Full schematic of the proposed bi-directional amplifier.

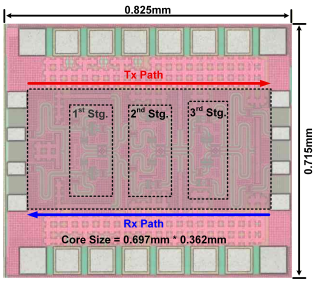


Fig. 5: Microphoto of fabricated chip in 65-nm CMOS process.

In addition, for Tx mode, Z_{S_Tx} and Z_{L_Rx} hardly changes with the changing of L_2 as the off-mode path always shows a high impedance, vice versa for L_2 in Rx mode. Although the asymmetric peaking inductors introduce a slight neutralization imbalance, the resulting enhancement in forward gain far outweighs this penalty. To verify the theory, simulation results of max available gain (MAG) of the transistor cores with a size of $120\mu m$ are shown in Fig. 3(a). A 3/4 dB improvement for Tx/Rx mode is achieved compared with conventional design. Stability is also improved due to gain suppression in low frequency band as shown in Fig. 3(b). Actual implementation of the matching for Tx mode $\mathrm{OP_{1dB}}$ and Rx mode NF optimization is show in Fig. 3(c) and (d).

C. Full Schematic of the Bi-Directional Amplifier

Fig. 4 presents the complete schematic of the proposed three-stage bi-directional amplifier. Transistors M1–M3 function as the Tx devices, with gate widths of 60 μm, 80 μm, and 120 μm, respectively, while M4–M6 serve as the corresponding Rx devices with identical dimensions. The peaking inductors and M.N. are implemented as transmission lines.

III. Simulation and Measurement Results

The proposed 60-GHz broadband bi-directional amplifier is fabricated in TSMC 65-nm CMOS process. Fig. 5 shows the prototype microphoto. The chip occupies an area of 0.825mm × 0.715mm, including RF and DC pads. The core area is of 0.697mm × 0.362mm.

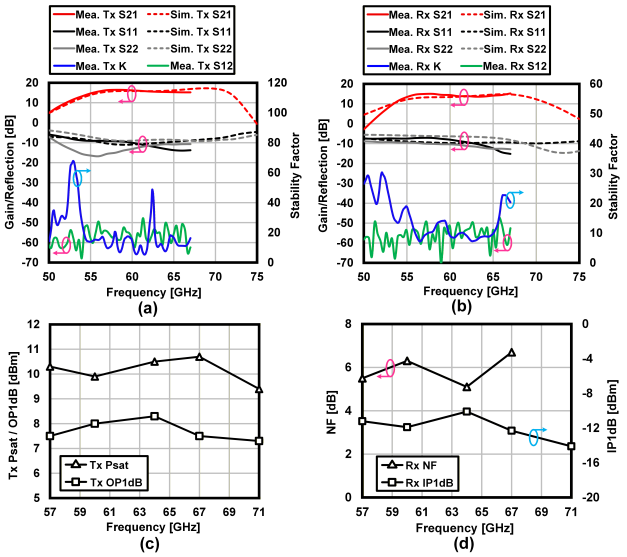


Fig. 6: (a) S21, S11, S22, S12 and K of Tx mode. (b) S21, S11, S22, S12 and K of Rx mode. (c) Measured $\mathrm{OP_{1dB}}$ and P_{sat} of Tx mode. (d) Measured $\mathrm{IP_{1dB}}$ and NF of Rx mode.

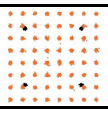
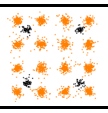
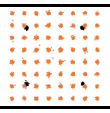
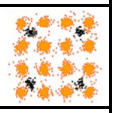
A. Small Signal

Small signal measurements results are summarized in Fig. 6. The measured 3-dB bandwidth is from 54-GHz to 67-GHz, with a peak small signal gain of 16.1/15.3 dB in Tx/Rx mode. The performance over 67-GHz is not measured due to the equipment limitations.

B. Continuous Wave Large Signal

In large signal measurements, the measured Tx mode $\mathrm{OP_{1dB}}$ and saturated output power is 8.3 dBm and 10.5 dBm separately at center frequency. The performance at other frequencies is also measured and summarized in Fig. 6(c). The Rx mode $\mathrm{IP_{1dB}}$ and NF across the band of interested is also summarized in Fig. 6(d), which maintains around -12 dBm and 6 dB respectively.

TABLE I: Summarized modulated signal measurement results of proposed amplifier in Tx and Rx mode

Operation Mode	**Tx Mode @64-GHz**		**Rx Mode @64-GHz**	
Modulation Mode	OFDM–A			
MCS	19	10	19	10
Modulation Scheme	64QAM	16QAM	64QAM	16QAM
Bandwidth /GHz	2	14	2	14
Data Rate /Gb/s	12	56	12	56
Constellation				
EVM	-31.7dB (2.6%)	-20.6dB (9.3%)	-31.1dB (2.8%)	-18.5dB (11.9%)

C. Modulated Signal

Following the 5G NR FR2-2 specifications, which support up to 2-GHz channel bandwidths, the proposed amplifier was characterized using 64-QAM OFDM signals to verify its wideband linearity, as shown in table I. At a center frequency of 64 GHz, it achieves an EVM of 2.6% in Tx mode and 2.8% in Rx mode, fully compliant with the 64-QAM constellation requirements while enabling a 12-Gb/s data rate. Furthermore, to demonstrate its potential for future B5G/6G application scenarios, carrier aggregation was evaluated across a 14-GHz span. Utilizing 16-QAM OFDM signals, the amplifier achieves measured EVMs of 9.3% (Tx) and 11.9% (Rx), corresponding to a ultra-high data rate of 56 Gb/s for 60-GHz bi-directional designs. Comparison of this work among other state-of-art V-band designs is summarized in table II.

IV. Conclusion

This article has presented a linear, broadband differential bi-directional amplifier for 60-GHz large-scale phased-array transceivers. Peaking inductors are implemented at the gate of transistors for impedance alignment of both Tx and Rx path. Neutralization is simply realized by a cross-section instead of complex custom layout. Implemented in a 65-nm CMOS process, the amplifier delivers a measured $\mathrm{OP_{1dB}}$ of 8.3 dBm for Tx and a measured $\mathrm{IP_{1dB}}$ of -10.1 dBm for Rx at center frequency, consuming 103 mW for Tx and 78 mW for Rx under 1-V supply. In modulation signal measurements, the proposed amplifier achieves EVMs of 2.6% (Tx) and 2.8% (Rx) for 64-QAM. With 16-QAM modulation and 14-GHz bandwidth, an ultra-high data rate of 56 Gb/s is achieved. The results validate the significant potential of proposed amplifier for next-generation B5G/6G ultra-high-throughput mmW communication systems.

TABLE II: Performance Comparison of State-of-art Bi-directional amplifiers

	This Work	**[2]**	**[3]**	**[5]**
Process	**65-nm CMOS**	65-nm CMOS	65-nm CMOS	130-nm SiGe
Gain (Tx/Rx) /dB	**16.4/15.3**	24.0/22.0	15.0/18.0	14.7/14.1
Bandwidth /GHz	**57–71**	57–66	34–59	59–61
Tx $\mathrm{OP_{1dB}}$ /dBm	**8.3**	N/A	-3	7.2
Rx $\mathrm{IP_{1dB}}$ /dBm	**-10.1**	-30[a]	N/A	-13.5
Rx NF /dB	**5.1**	5.4	8.4	4.6
Core Size /mm^2	**0.25**	0.44	0.44	0.40

a: Estimated from figure.

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