295~318GHz, 32-unit Planar Phased Array RX with Mixer-first RF Unit and IF Current Combiner

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***Abstract*—>300 GHz frequency offers broadband spectrum for high-speed wireless data link and sensing. To overcome the increasing path loss, large-scale phased arrays are in demand. This paper presents a 295~318 GHz, 32-unit, λ/2-spaced planar phased array receiver (RX), featuring low noise mixer-first RF unit and broadband IF current combiner. Firstly, to achieve low noise nearby 300 GHz, a 3rd subharmonic mixer (SHM), co-designed with an inductor-less IF LNA, is proposed. A lower conversion loss of SHM is achieved by a higher IF impedance of 200Ω, which also reduces the NF of LNA. The SHM is fed by an on-chip patch antenna with superstrate, presenting >50% antenna efficiency. To avoid the loss of RF or IF beamformer, a LO beamformer, utilizing a 7-bit digital-to-time converter (DTC) and a ×9 multiplier chain, is adopted. Secondly, voltage-mode IF networks suffer from limited bandwidth due to the high parasitics of the long on-chip IF wiring. This work adopts a 16-to-1 current-mode IF combiner, which achieves broadband current recombining through a low impedance cascoding scheme. The 32-unit (16×2) phased array RX consists of two 16-unit (8×2) chips, fabricated by 65nm bulk CMOS process. Measurements of the 32-unit RX array at 315GHz show an equivalent isotropic conversion gain (EICG) of 28 dB and an equivalent isotropic noise figure (EINF) of 0.6 dB. It supports an H-plane beam scanning angle of ±55°. A 8Gbps wireless transmission has been demonstrated.**

Keywords—65nm-CMOS, large-scale, λ/2-spaced, phased array, terahertz, wide-angle scanning.

I. Introduction

>300 GHz frequency band provides abundant unlicensed spectrum for ultra-high-speed data transmission, holding promise for next-gen wireless comms and high-res sensing. Due to severe path loss degradation, phased array tech is highly demanded [1-6]. Yet large-scale λ/2-spaced phased arrays remain challenging above 100 GHz, particularly beyond 300 GHz. Near 300 GHz, λ/2 spacing (~0.5 mm) severely restricts per-unit circuit area, hindering λ/2 array implementation [1,3]. Moreover, in THz band, mixer-first RXs suffer large conversion loss and high NF [1,2,3,7,8]. Although recent studies have demonstrated the feasibility of implementing CMOS-based amplifiers in the THz band, they often come with high power consumption and large chip area [10]. Further, IF bandwidth presents a primary challenge: the limited layout area in the THz band prevents conventional power combining from being implemented, while the parasitic effects of long transmission lines restrict the IF bandwidth in voltage-mode combining [5,6].

To address these issues, as shown in Fig. 1, this work implements a 295~318 GHz, 32-unit planar phased-array RX with a beam scanning angle of ±55° and a 3-dB beamwidth of 5°. Each RX unit consists of a 3rd SHM for down-conversion and an inductor-less IF LNA. It also integrates an on-chip patch antenna with a superstrate, which achieves an

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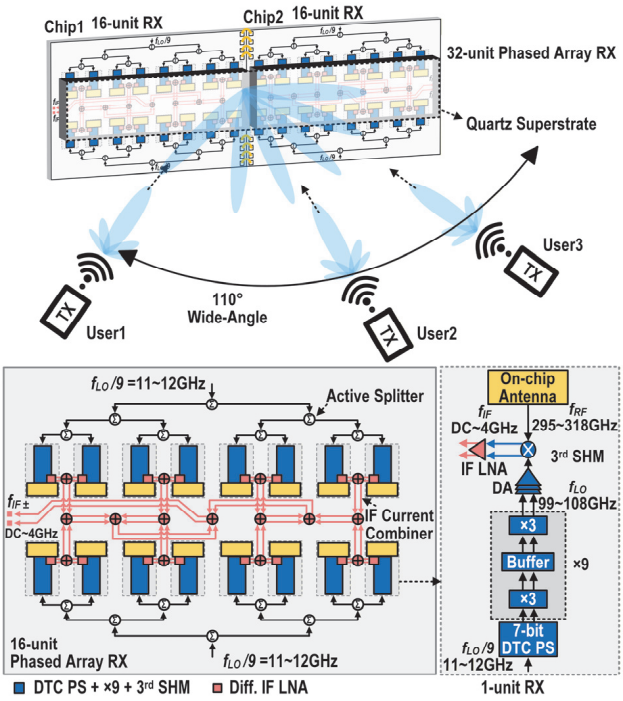


Fig. 1. Architecture of 295~318GHz, 32-unit phased array RX.

efficiency greater than 50%. The 3rd SHM is driven by a LO based on a ×9 multiplier, achieving high conversion gain and thus optimal noise performance. For IF signal combining, an on-chip active current combiner is adopted, realizing broadband IF current combining without using large-area low-frequency matching. Beam scanning is realized by applying phase shifts to an 11~12 GHz signal from active splitter through a 7-bit DTC, thus avoiding link losses caused by RF beamformer [4] and bandwidth limitations caused by IF beamformer [9].

II. Circuits of Phased Array Rx

A. Mixer-first RF Unit with 3rd-SHM, IF LNA, LO Chain

The 1-unit RX core architecture and signal chain are illustrated in Fig. 2. The scheme first employs a 3rd SHM for down-conversion. 3rd SHM's RF input is matched using an on-chip transformer to an on-chip antenna, which is an on-chip patch antenna based on 100um-thick quartz superstrate with a simulated gain of approximately 3 dBi (>50% antenna efficiency). This design optimizes power transfer while effectively suppressing LO fundamental and harmonic leakage. Specifically, filtering capacitors C_0 introduced at the center taps of the transformers connected to 3rd SHM core differential pair further improve LO leakage rejection and common-mode rejection. The mixer core utilizes NMOS

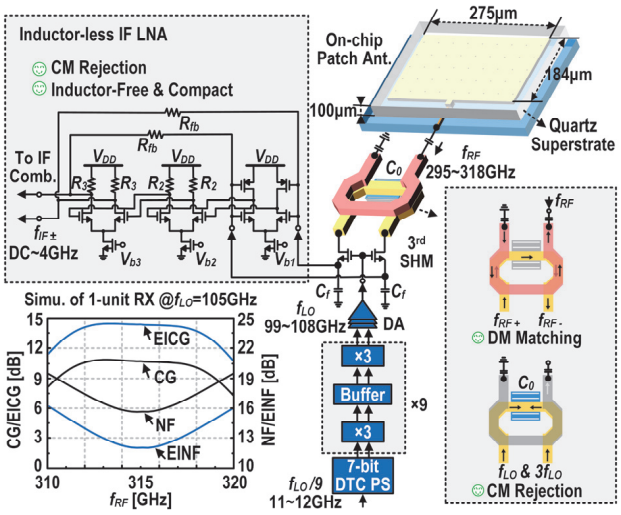


Fig. 2. Schematic of 1-unit RX with patch antenna, 3rd SHM and IF LNA

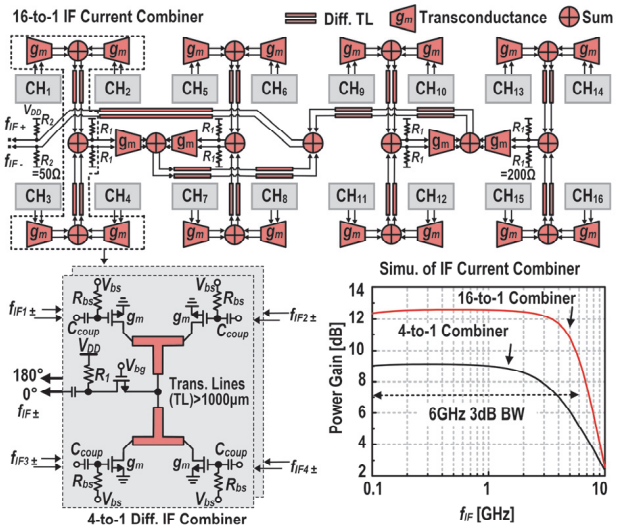


Fig. 3. Schematic of 16-to-1 IF current combiner

differential pairs, with a 200 fF capacitor C_f connected in parallel to ground at their source nodes, providing a high-frequency, low-impedance path for leakage components of the RF and LO signals. This stabilizes the operating point of the switching transistor, thereby enhancing conversion gain, noise figure (NF). The 3rd SHM employs a higher IF impedance of 200 Ω to reduce its conversion loss, which also contributes to lowering the LNA's NF.

The down-converted IF signal is amplified by an inductor-less, three-stage differential transimpedance amplifier (TIA)-based IF LNA. Its fully differential operation provides good common-mode noise rejection, while the inductor-less design significantly improves chip area utilization, facilitating system integration. As shown in Fig. 2 ,the simulated per-unit conversion gain of 3rd SHM and LNA peaks at 10.9 dB, with a minimum NF of 15.6 dB. Considering the antenna gain, the peak EICG is 14.4 dB, and the minimum EINF is 12 dB.

In this design, the 105 GHz LO signal is generated through a dedicated path that integrates phase shifter, cascaded ×9 multiplier chain, and drive amplifier (DA). First, a phase shifter based on a 7-bit DTC performs digital phase modulation on the input signal. Subsequently, the signal enters a three-stage cascaded ×9 frequency multiplier chain: the first stage is a frequency tripler, the second stage is a buffer amplifier, and the third stage is another frequency tripler, ultimately outputting a 105 GHz LO signal. Inter-stage matching is achieved using transformers to provide broadband matching and suppress even-order harmonics. To drive 3rd SHM, the multiplier's output is fed into a three-stage DA to enhance drive capability. Matching between the DA stages is implemented using transmission lines and capacitors. The final DA performs differential-to-single-ended conversion and matching, delivering approximately 2.5 dBm of drive power to 3rd SHM at the 105 GHz LO frequency.

B. Broadband 16-to-1 IF Current Combiner

The IF current combiner is designed for efficient signal summation from multiple units. As shown in Fig. 3 , This design is based on a two-stage "4-to-1" combining architecture, ultimately achieving on-chip combination of signals from 16 units. The core of each stage of combiner employs a low impedance common-source common-gate (CS-CG) cascode amplifier structure. Specifically, the input IF voltage signal is first converted into a current signal by the CS transistor. This current signal is transmitted via a long transmission line—approximately 1 mm in the first-stage "4-to-1" combiner and about 3 mm in the second-stage "4-to-1" combiner—and converges into the subsequent CG transistor for current-mode summation. The combined current is then converted back to a voltage output via load resistors. The common-gate stage exhibits a low input impedance ($1/g_m$), which significantly reduces the RC time constant at the node of the long transmission line, thereby facilitating the extension of the system bandwidth. Fig. 3 indicates a simulated power gain of 12.6 dB and a 3 dB bandwidth of DC to 6 GHz for the16-to-1 combiner. The first-stage 4-to-1 combiner drives a 200 Ω load, the second stage is designed for a 50 Ω load to match the off-chip transmission line impedance. This discrepancy in load impedance explains why the gain progression from 4-to-1 to 16-to-1 does not follow the theoretical 6 dB increase. This active IF current combiner enables signal current summing with balanced bandwidth and noise. Current-domain summing also reduces matching loss and area for low-frequency structures.

III. Measurement Results

The 8×2 phased-array RX chip is fabricated in a standard 65-nm bulk CMOS process. The chip measures 4.04 × 3.03 mm². A die micrograph is shown in Fig. 4. Each RX unit occupies an area of 0.765 mm² and consumes 117 mW. Two array configurations are implemented: (1) a 16-unit array using one RX chip, and (2) a 32-unit array using two RX chips. Both prototypes are tested wirelessly (over-the-air). As illustrated in Fig. 5, the radiative test link is established using external frequency multipliers, a signal source, and standard-gain horn antennas. All measurements are conducted at room temperature (290K).

Regarding the array's EICG, the tests verified the coherent combining capability of the array. As shown in Fig. 6(a), with only a single RX unit enabled at f_{LO}= 105 GHz and f_{RF}= 312.6 GHz, the measured peak EICG—after de-embedding the on-chip combiner and normalizing to a 0-dBi

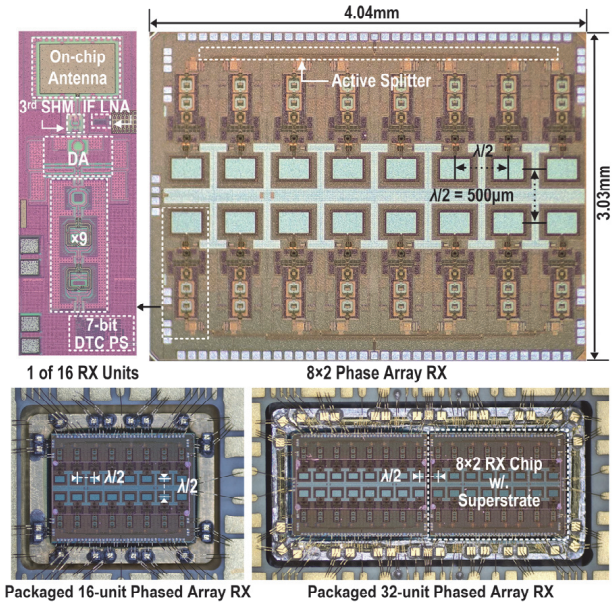
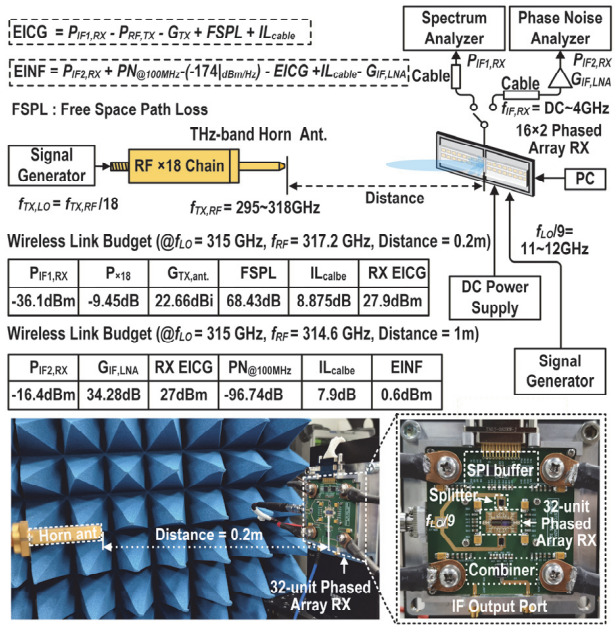


Fig. 4. Die photo, packaged 32-unit and 16-unit phased array RX



$P_{IF1,RX}$	$P_{×18}$	$G_{TX,ant.}$	FSPL	IL_{calbe}	RX EICG
-36.1dBm	-9.45dB	22.66dBi	68.43dB	8.875dB	27.9dBm

$P_{IF2,RX}$	$G_{IF,LNA}$	RX EICG	$PN_{@100MHz}$	IL_{calbe}	EINF
-16.4dBm	34.28dB	27dBm	-96.74dB	7.9dB	0.6dBm

Fig. 5. Mesurement setup for RF performance characterization

isotropic antenna—is 14.1 dB. Subsequently, when the 16-unit receiving array is enabled and phase-calibrated, as depicted in Fig. 6(b) (f_{LO}= 105 GHz, f_{RF}= 315.2 GHz), the peak EICG increased to 24.3 dB. The deviation from the theoretical value is primarily attributed to amplitude/phase errors. Fig. 6(c) presents a frequency sweep of the 16-unit array with a fixed IF of 0.2 GHz and an RF step of 0.5 GHz. A peak EICG of 23.6 dB is measured at f_{LO}= 104.93 GHz and f_{RF}= 315 GHz, with an operational bandwidth spanning 295 to 318 GHz. Finally, with all 32 RX units operating concurrently and phase-calibrated, the system achieved a peak EICG of 28 dB at f_{LO}= 105 GHz and f_{RF}= 317.2 GHz, as shown in Fig. 6(d). The IF 3-dB bandwidth for both the upper and lower sidebands is 4 GHz. The array demonstrates excellent noise performance. As shown in Fig. 7(a) and (b), the EINF is measured. In the 16-unit mode, a

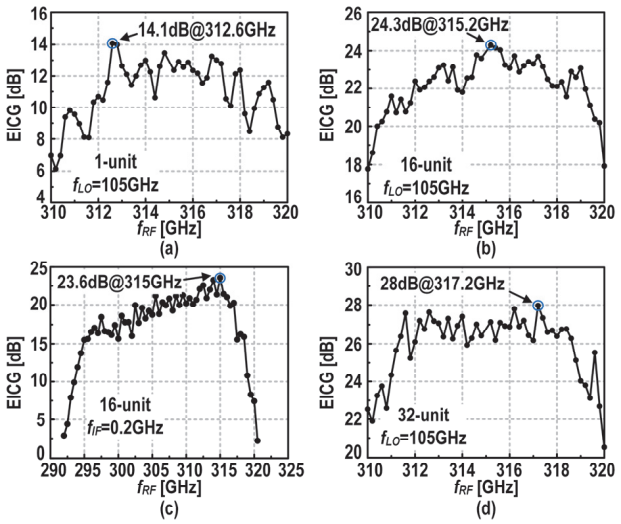


Fig. 6. Measured EICG: (a) 1-unit RX and (b) 16-unit RX @ f_{LO}=105GHz, (c) 16-unit RX @ f_{IF}=0.2GHz, and (d) 32-unit RX @ f_{LO}=105GHz.

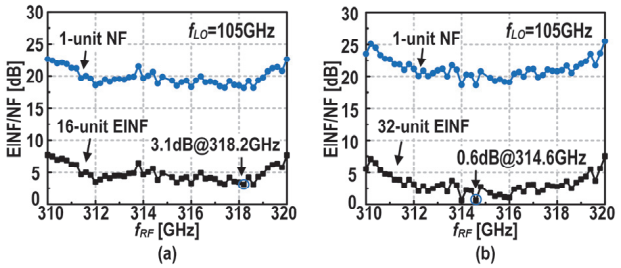


Fig. 7. Measured EINF and NF: (a) 16-unit RX and (b) 32-unit RX.

minimum EINF of 3.1 dB is obtained. The corresponding 1-unit RX NF, after de-embedding the unit combining gain and on-chip antenna gain, is 18.1 dB. When all 32 units operated coherently at the optimal beam steering angle, the system achieved a remarkable minimum EINF of 0.6 dB. This superior performance benefits from the effective suppression of noise via spatial power combining in the array. The corresponding de-embedded 1-unit RX NF for the 32-unit RX is 18.6 dB. The radiation patterns are measured using an antenna turntable. The H-plane and E-plane patterns for a 1-unit RX are shown in Fig. 8(a) and (b), respectively, agreeing well with theoretical expectations. The measured patterns for the 16-unit and 32-unit RX arrays are presented in Fig. 8(c) and (d). Both the 16-unit and the 32-unit RX array achieved a beam scanning range exceeding ±55° in the H-plane (azimuth plane). The main lobe beamwidth is 11° for the 16-unit RX array and 5° for the 32-unit RX array.

Finally, the system's practical performance is evaluated through wireless communication experiments based on QPSK and 16QAM modulations. Four high-data-rate wireless links employing QPSK and 16-QAM schemes are measured; the corresponding constellation diagrams are shown in Fig. 9. With an f_{LO} of 105 GHz, a carrier center frequency of 317 GHz, and a communication distance of 10 cm, the transmitted QPSK signal at 6 Gbps achieved a received signal-to-noise ratio (SNR) of 12.7 dB with an EVM of 23%. The 16-QAM transmission at 8 Gbps exhibited an SNR of 14.8 dB and an EVM of 14%.

TABLE I. COMPARISON WITH THE STATE -OF-THE-ARTS

	This Work		ISSCC2026 [1]	JSSC2022 [2]	SSCL2025 [3]	JSSC2023 [4]	JSSC2022 [5]	RFIC2024 [6]	JSSC2016 [7]	RFIC2015 [8]
Freq. Band [GHz]	295~318		436~472	242~280	262~275	110~170	139~155	132~142	320	312
Array Size	16 (8×2)	32 (16×2)	4 (4×1)	4 (4×1)	4 (2×2)	4 (4×1)	8 (4×2)	128 (2×8×8)	8	4 (2×2)
RX Architecture	Phased Array		Phased Array	Phased Array	Phased Array	Phased Array	Phased Array	Phased Array	RX Array	RX Array
Ant. Spacing [λ]	0.5×0.5		0.63	0.5	0.54×0.54	0.5	0.5×0.5	0.57×0.57	N/A	N/A
Antenna Type	On-chip Patch Ant. +Superstrate		On-chip Patch Ant. +Superstrate	Off-chip AiP	Off-chip AiP	On-chip Patch Ant.	On-chip patch Ant. +Superstrate	Off-chip Aip	On-chip Patch Ant.	On-chip Loop Ant.
EICG [dB]	24.3	28	-8.1†	-14†	20	32.8†	27.5	N/A	29.8	-19
EINF [dB]	3.1	0.6	12	N/A	18	N/A	N/A	N/A	30~40†	N/A
NF [dB]	18.1	18.6	27.5	20††	N/A	10.08††	6.4	7††	N/A	N/A
1st Stage Detector	3rd SHM		2nd SHM	2nd SHM	Mixer	LNA	LNA	LNA	2nd SHM	3rd SHM
H&V Beam Steering	±55° / N/A		±35° / N/A	±18° / N/A	±20°/ ±30°	±45° / N/A	±35° / N/A	±45° / ±45°	N/A / N/A	N/A / N/A
Beamforming Arch.	LO DTC		IF PS	LO Varactor	LO&IF PS	RF TTD	IF VM	RF VM	N/A	N/A
Phase Shifter Res. [bit]	7		6	N/A	N/A	4	5	4	N/A	N/A
IF 3dB Bandwidth [GHz]	DC~4		2~8†	3~22†	43.5~56.5	DC~27	9.5~12.5	9~14	N/A	1.1~2.3
Wireless Data Rate[Gbps]	8		N/A	36	36	200	10	2×42	N/A	N/A
P_{DC} / Unit [mW]	117		211	750	700	488	145	97	14.64	27.5
Chip Area / Unit [mm²]	0.765		1.92	4.17	7.37	5.65	3.17	0.73	0.38	0.43
Technology	65nm CMOS		65nm CMOS	65nm CMOS	40nm CMOS	130nm SiGe	45nm CMOS-SOI	45nm RFSOI	130nm SiGe	65nm CMOS

† Estimated from figure. †† Simulation results without antenna loss

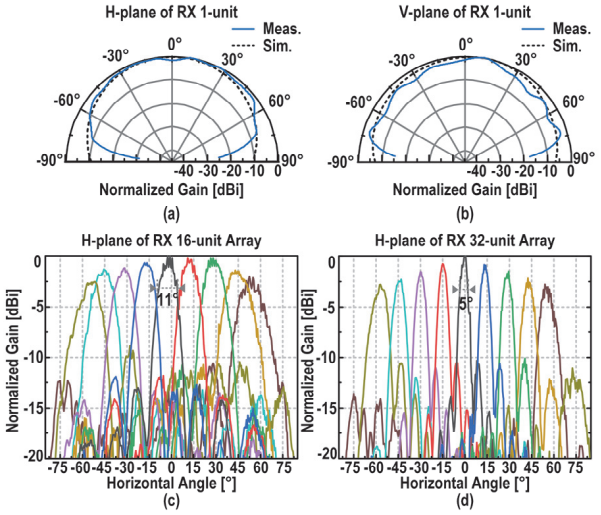


Fig. 8. Measured antenna pattern at f_{RF}=315 GHz: (a) H-plane and (b) V-plane of 1-unit RX, H-plane of (c) 16-unit RX and (d) 32-unit RX.

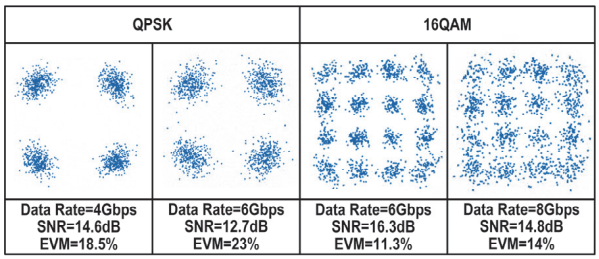


Fig. 9. Measured constellation and EVM of wireless link.

IV. CONCLUSION

This work presents a silicon phased array RX chip using 65nm CMOS. The core RX link utilizes a 3rd SHM to down-convert a 295~318GHz RF signal to an IF. The LO chain generates a 98.3~106GHz LO from an 10.9~11.8GHz reference through a 7-bit DTC and a ×9 frequency multiplier. The design achieves compact broadband combining through 16-to-1 IF current combiner. Table I compares this work with other state-of-the-art designs. Test results show the 32-unit array has an EICG of 28dB, an EINF of 0.6dB, and a beam scanning range exceeding ±55°. In wireless communication experiments, data transmission rates of 6Gbps (QPSK) and 8Gbps (16-QAM) are achieved. Among reported phased arrays above 300 GHz, this work achieves the largest scale, featuring a half-wavelength spacing configuration and a highly competitive noise figure.

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