A 25.4-to-29.7GHz Dual-Path-Synchronized Quad-Core Class-F^{-1} VCO with Q-Enhanced 1st and 2nd Harmonic Resonance Achieving 194.5dBc/Hz FoM at 1MHz Offset in 55nm FDSOI

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***Abstract*—This paper presents a low phase noise (PN) quad-core inverse class-F (class-F^{-1}) voltage-controlled oscillator (VCO) with dual-path-synchronized and Q-enhanced first and second harmonic resonance. By establishing direct interconnections between non-adjacent cores and maintaining coupling between adjacent cores, PN degradation caused by frequency mismatch is eliminated, while high-Q transformers suppress PN. In addition, constructive coupling is obtained in both differential-mode (DM) and common-mode (CM) operation, leading to simultaneous DM and CM impedance enhancement and further PN suppression. Fabricated in a 55nm FDSOI, the proposed oscillator achieves -121.1 dBc/Hz PN at 1 MHz offset from a carrier of 25.8 GHz, corresponding to a state-of-the-art peak FoM of 194.5 dBc/Hz. It consumes 28.4 to 33.6 mW from a 0.6 V supply, and occupies a core area of 0.07 mm^2.**

Keywords—phase noise, inverse class-F oscillator, voltage-controlled oscillator, dual-path synchronization, DM and CM impedance enhancement.

I. Introduction

The high-order modulation schemes employed in millimeter-wave (mm-wave) wireless communication networks, such as 5G-Advanced and future 6G, imposes strict phase noise (PN) requirements on oscillators. Harmonic shaping [1-11] and multi-core coupling [12-13] are effective technique for reducing PN at mm-wave frequencies. [2] proposed a class-F$_{23}$ voltage-controlled oscillator (VCO), which achieves low phase noise (PN) by combining harmonic shaping and multi-core coupling techniques. However, the head transformer for achieve high common-mode (CM) impedance results in increased area, and the lack of synchronization among non-adjacent oscillator cores leads to PN penalty caused by frequency mismatch. The scalable inter-core-shaping multi-core VCO can effectively enhance CM impedance without increasing area [3], which improves the Q of the CM inductor by nulling CM mutual coupling and further boosts the CM impedance by eliminating single-ended capacitors. Moreover, a PN reduction of 13 dB is achieved by coupling 20 oscillators together. Nevertheless, the frequency mismatch among the oscillator cores hinders the improvement of PN performance. [4] presents an inverse class-F (class-F^{-1}) VCO that achieves outstanding PN without third-harmonic shaping, where a circular pentafilar transformer-based tank combined with segmented high-impedance tuning serves to reduce PN while strengthening synchronization among non-adjacent cores. However, the destructive coupling in differential mode (DM) inevitably lowers the fundamental impedance, thereby deteriorating PN performance.

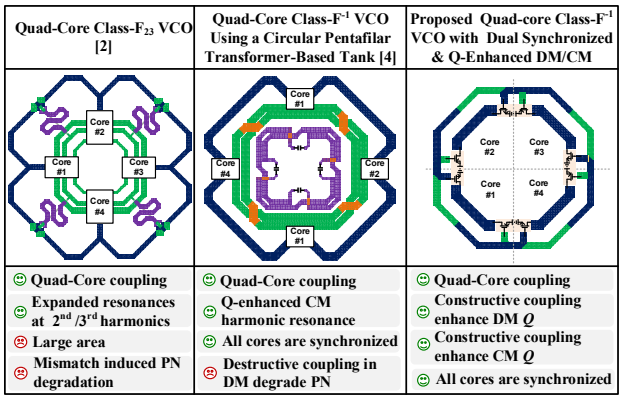


Fig. 1. The comparison of the prior-art and proposed VCO.

To mitigate the above-mentioned issues, this paper proposes a quad-core class-F^{-1} VCO, which incorporates the dual-path synchronization with both DM and CM quality-factor enhancement to achieve superior PN and FoM performance. Implemented in a 55nm FDSOI technology, the proposed VCO achieves -121.1 dBc/Hz at 1 MHz offset from 25.8 GHz, corresponding to a FoM of 194.5 dBc/Hz that compares competitively with prior art. Thanks to the proposed dual-path synchronization technique, the measured FoM across ten prototype samples exhibits a variation of less than 0.3 dB.

II. Proposed Class-F^{-1} VCO

A. Dual Path Synchronization

Fig. 2 shows the schematic of the proposed dual-path-synchronized quad-core class-F^{-1} VCO, in which non-adjacent class-F^{-1} VCO cores are directly interconnected through gate inductors, while adjacent class-F^{-1} VCO cores are coupled together through gate-to-drain inductors. For non-adjacent VCO cores, direct parallel connection

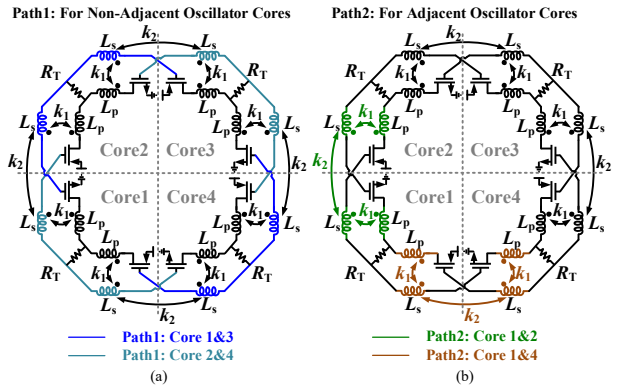


Fig. 2. The schematic of the proposed dual-path-synchronized quad-core class-F^{-1} oscillator. (a) Direct connection. (b) Coupling.

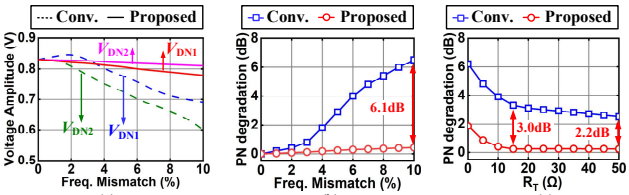


Fig. 3. Voltage and PN variation with frequency mismatch.

significantly suppresses mismatch-induced frequency deviations as shown in Fig. 2(a). Furthermore, by increasing the resistor (R_T) of the inductor center-tap, the current flow into the tap is effectively blocked, ensuring identical oscillation amplitude across the non-adjacent cores. For adjacent oscillator cores, employing magnetic coupling between L_p and L_s within an additional synchronization path as depicted in Fig. 2(b), leading to further suppression of mismatch-induced impairments. The simulation results demonstrate that under frequency mismatch, the oscillation amplitude difference between Core 1 (Core 3) and Core 2 (Core 4) is merely 0.03 mV, corresponding to a PN degradation of only 0.43 dB, as shown in Fig. 3(a) and (b). Under a frequency mismatch setting of 10%, the PN degradation of the VCO across R_T variations from 0 to 50 Ω is illustrated in Fig. 3(c). The results show that when R_T is greater than 15 Ω, the degradation of PN is constant. In this design, a 15 Ω R_T is chosen to balance mismatch and PN.

B. DM and CM Impedance Enhancement

Fig. 4 illustrates the circuit implementation and floorplan of the proposed quad-core class-F^{-1} VCO operating in DM and CM excitations. PMOS and NMOS are both placed inside the inductor while maintaining a distance greater than 30 μm from the inductors to minimize the influence on Q. The center tap of the inductors is interconnected through high-resistance metal line, simultaneously enabling self-biasing, mitigation of mode ambiguity, and suppression of mismatch-induced impairments. The inductor at the gate of each VCO core is coupled to both the drain and gate inductors of its adjacent VCO core, with coupling coefficients k_1 and k_2, respectively.

In DM, the currents flowing through all inductors share the same direction, as shown in Fig. 4(a). As a result,

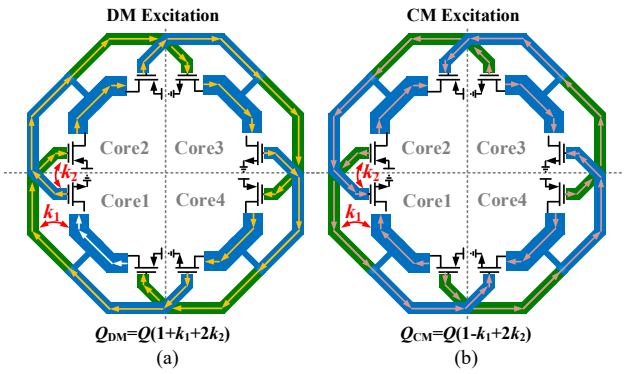
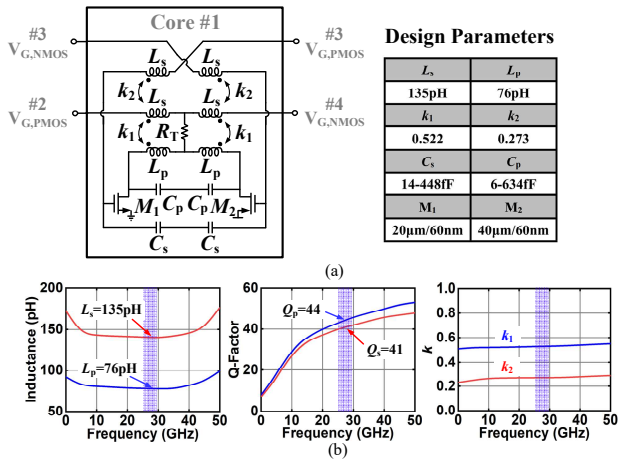


Fig. 4. The floorplan of the proposed oscillator operating in (a) DM and (b) CM excitations.



L_s	L_p
135pH	76pH
k_1	k_2
0.522	0.273
C_s	C_p
14-448fF	6-634fF
M_1	M_2
20μm/60nm	40μm/60nm

Fig. 5. (a) The schematic of the proposed VCO core. (b) simulated parameter of the transformer.

constructive mutual coupling enhances the Q in DM by a factor of $1+k_1+2k_2$. In CM, the currents in all gate inductors flow in the same direction, while those in all drain inductors also share a common direction, with the current directions between gate and drain inductors being opposite. Under this configuration, the destructive coupling k_1 between gate and drain inductors, combined with the constructive coupling k_2 among adjacent gate inductors, collectively alters the Q in CM by $1-k_1+2k_2$ times. When k_2 is sufficiently large, it can counteract the detrimental effect of k_1 on the Q in CM, as depicted in Fig. 4(b). Compared to implicit CM techniques that exhibit destructive coupling in CM operation [4], the proposed topology eliminates the destructive coupling, thereby maintaining a high Q in CM. In addition to inductor Q enhancement, the proposed VCO employs differential capacitors in both DM and CM states, thereby improving the capacitor Q. As a result, the enhancement of both inductor and capacitor Q under DM and CM effectively increases the first and second harmonic impedances, thereby strengthening the harmonic-shaping effect.

C. Circuit Implementation

The schematic of the VCO core is detailed in Fig. 5(a), where stacked PMOS and NMOS ensure differential output,

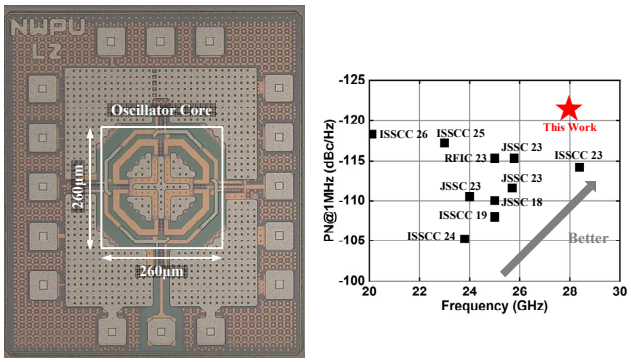


Fig. 6. Die micrograph and benchmarks with the relevant prior-art VCOs.

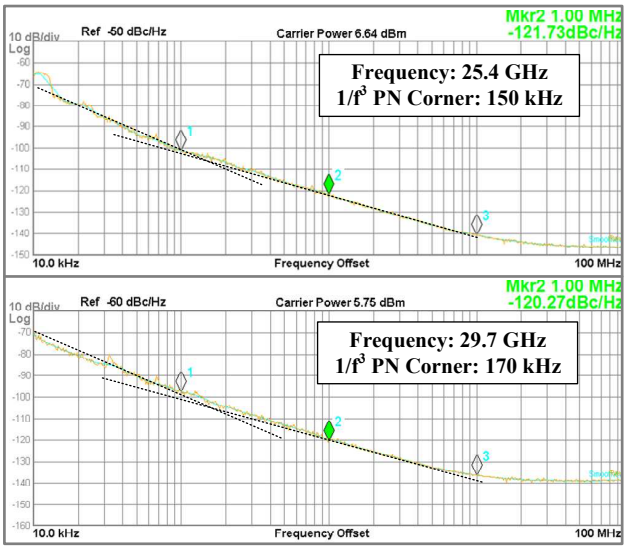


Fig. 7. Measured PN.

with the size of 40 µm/60 nm and 20 µm/60 nm, respectively. C_P and C_S employ 6-bit switched capacitor array alongside an additional varactor, dedicated to frequency tuning and second harmonic alignment, respectively. The transformer in the layout of Fig. 4 employs the top thick layer and thick AP to maximize the Q. Electromagnetic (EM) simulation results indicate that the inductances of L_p and L_s are 76 pH and 135 pH, respectively, with quality factors reaching 44 and 41 at 28 GHz, as shown in Fig. 5(b). At 28 GHz, the coupling coefficient k_1 between L_p and L_s is 0.522, while the coupling coefficient k_2 between the adjacent L_s is 0.273. Owing to the complementary topology of the Class-F^{-1}, the close proximity between VDD and GND facilitates a minimized CM current return path through decoupling and parasitic capacitors, which further reduces the flicker noise.

III. Measurement Results

The proposed dual-path-synchronized quad-core class-F^{-1} oscillator is designed and fabricated in a 55nm FDSOI and occupies a core area of 0.07 mm^2 excluding the output buffer and pads as shown in Fig. 6. The oscillator dissipates 28.4 to 33.6 mW from a 0.6 V supply. Fig. 7 displays the PN measurement results, showing that at 25.4 GHz, the measured PN and the corresponding FoM are -100.0/-121.7/-141.7 dBc/Hz and 192.8/194.3/194.8 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz offsets, respectively, with a 1/f^3 flicker corner of approximately 150 kHz. At 29.7 GHz, the measured PN and the corresponding FoM are -99.8/-120.1/-139.6 dBc/Hz and 191.9/194.2/194.4 dBc/Hz at 100 kHz, 1 MHz, and 10 MHz offsets, respectively, with a 1/f^3 flicker corner of approximately 170 kHz. Since the PN approaches the noise floor of instrument after 10 MHz offset, the measured results consequently appear as flat lines. Fig. 8 depicts the measured PN, the corresponding FoM, and the 1/f^3 flicker corner across frequency tuning range. The PN at 1 MHz offset ranges from -120.1 to -121.7 dBc/Hz, with the corresponding FoM varying between 193.5 and 194.5 dBc/Hz, while the 1/f^3 flicker corner remains below 170 kHz throughout the entire frequency tuning range. Fig. 8(d) shows the measured frequency pushing is merely 14 MHz/V at 29.7 GHz, whereas it increases to 30 MHz/V at 25.4 GHz.

Table 1 summarizes the measured results and shows the comparison between the relevant prior-art VCOs. Compared with other quad-core VCOs, the proposed VCO achieves the lowest PN and best FoM at 100 kHz and 1 MHz offsets, owing to the dual-path synchronized class-F^{-1} topology that reduces the PN degradation induced by mismatch while enhancing the Q-factor at the 1st and 2nd harmonic resonances. Benchmarking against the oscillators in Fig. 6, this work demonstrates the best PN performance at 1 MHz offset around 28 GHz.

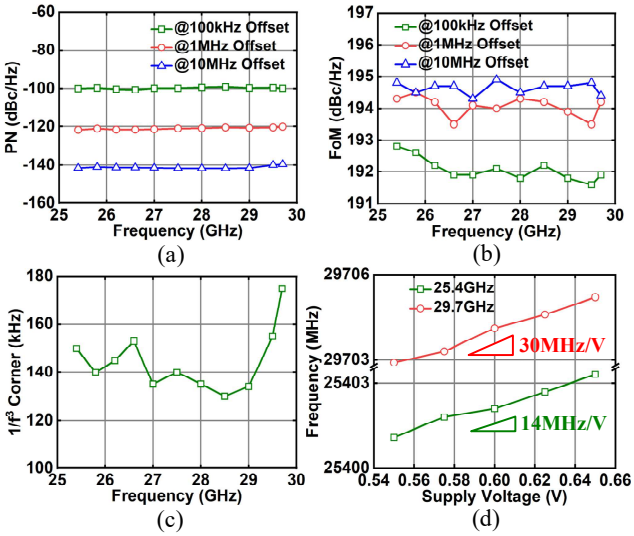


Fig. 8. Measured (a) PN, (b) FoM, (c) flicker corner across the tuning range and (d) frequency pushing at 25.4GHz and 29.7GHz.

IV. Conclusion

This paper reports a quad-core class-F^{-1} VCO that employs dual-path synchronization along with Q-enhanced first and second harmonic resonance for PN reduction. Implemented in 55 nm FD SOI process, the proposed VCO achieves a low PN of -121.5 dBc/Hz and a state-of-the-art FoM of 194.5 dBc/Hz at 1 MHz offset in 25.8 GHz.

TABLE I. SUMMARIZES AND COMPARISON WITH THE RELEVANT PRIOR-ART LOW PN VCOS.

		This Work	ISSCC'26 [4]	ISSCC'25 [2]	ISSCC'23 [9]	ISSCC'23 [3]	JSSC'23 [10]
Technology		55nm FDSOI	65nm CMOS	65nm CMOS	65nm CMOS	40nm CMOS	65nm CMOS
Topology		Circular xfmr + Dual Sync. Path	Circular xfmr + Trip. Sync. Path	Circular xfmr	Circular xfmr + Dual Sync. Path	Circular xfmr	Circular xfmr
Supply (V)		0.60	NA	0.50	0.50	NA	0.55
Power (mW)		28.4 to 33.6	18.5 to 24.0	17.3 to 21.0	17.6 to 25.0	11.0 to 12.0	22.5 to 23.6
Tuning Range (GHz)		25.4 to 29.7 (15.6%)	17.9 to 22.4 (22.3%)	18.5 to 23.6 (24.3%)	22.4 to 26.8 (18.2%)	25.4 to 30.3 (17.6%)	52.4 to 60.4 (14.2%)
PN (dBc/Hz)	100kHz	-99.1 to -100.6	NA	-92.1 to -95.4	-88.1	NA	-71.2 to -75.2
	1MHz	-120.1 to -121.7	-116.9 to -121.1	-116.8 to -118.3	-115.3	-113.1 to -115.6	-101.4 to -104.7
	10MHz	-139.6 to -141.9	-141.0 to -145.6	-138.0 to -139.3	-138.0	-133.8 to -136.4	-127.7
*PN referred to 28GHz (dBc/Hz)	100kHz	-99.4	-88.3	-91.7	-87.4	NA	-79.9
	1MHz	-120.9	-117.2	-115.5	-114.6	-114.3	-107.5
	10MHz	-141.9	-141.7	-136.5	-137.3	NA	-133.2
**FoM (dBc/Hz)	100kHz	191.6 to 192.8	NA	185.4 to 188.3	183.4	NA	172.1 to 176.9
	1MHz	193.5 to 194.5	190.4 to 192.5	189.4 to 192.6	190.6	191.8 to 193.3	182.2 to 186.5
	10MHz	194.3 to 194.8	194.3 to 196.9	190.1 to 193.0	193.3	192.6 to 194.0	188.5
$1/f^3$ PN corner (kHz)		130 to 170	110 to 430	140 to 250	780	250 to 350	800
Core Area (mm^2)		0.07	0.15	0.28	0.16	0.06	0.03

*PN referred to 28GHz=PN+$20\log_{10}(28GHz/f_{OSC})$
**FoM=$|PN(\Delta f)|+20\log_{10}(f_{OSC}/\Delta f)-10\log_{10}(P_{DC}/1mW)$

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