A 2-Cell Battery-Input Pseudo-T_{ON} Overlapping Controlled Symmetric Cross-Coupled Capacitor Converter with 97.1% Peak Efficiency and 0-1 VCR

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***Abstract*—This paper presents a two-phase symmetric cross-coupled capacitor (SCC) buck converter for 6–8 V battery-input applications. The proposed SCC power stage inherently achieves a continuous 0-to-1 voltage-conversion ratio (VCR) in a single operating mode, self-balances both inductor currents and flying-capacitor voltages without auxiliary circuits, and reduces inductor-current stress to lower conduction loss. A phase-allocation-based pseudo-T_{ON} overlapping control (POC) is employed to enable adaptive phase overlap during load transients, further improving the current slew rate. Fabricated in a 0.18-µm BCD process, the prototype occupies 2 × 3 mm² and delivers a 0.8-7 V output from a 6-8 V input at 0.8 MHz with a maximum load current of 4 A. Measurement results show a peak efficiency of 97.1%, while the overall efficiency remains above 85% for load currents exceeding 0.5 A. In addition, the converter achieves fast transient response, with an output undershoot/overshoot of 84/116 mV under a 0 to 4 A load step.**

Keywords*—Hybrid DC–DC converter, multilevel and multiphase buck converter, constant on-time control, phase overlapping, self-balancing.

I. Introduction

Battery-powered applications such as portable electronics and cordless tools increasingly rely on two-cell Li-ion batteries, which typically provide a 6-8 V input range. These systems demand step-down converters that simultaneously offer high efficiency, wide output-voltage range, and fast transient response under rapidly changing loads.

Hybrid buck converters have been widely investigated to improve efficiency. Three-level converters reduce the AC component of inductor current by using flying capacitors (C_{FS}), while multiphase converters reduce the DC conduction loss by distributing the load current across multiple inductors. However, conventional three-level converters employ only a single inductor and therefore suffer from significant DC conduction loss at heavy loads, whereas conventional multiphase converters typically require additional current-balancing circuits.

As shown in Fig. 1, the dual step-down (DSD) converter [1] combines a flying capacitor with two inductors, thereby reducing both AC and DC inductor-current losses while naturally balancing the phase currents. However, its VCR is limited to 0-0.25 and its current slew rate is relatively low during load transients. The cross-connected converter (CCC) [2] improves the transient response by introducing a D>0.5 operating condition, but its VCR is still limited to 0-0.25 in normal operation, as in [3] and [4], and an additional control

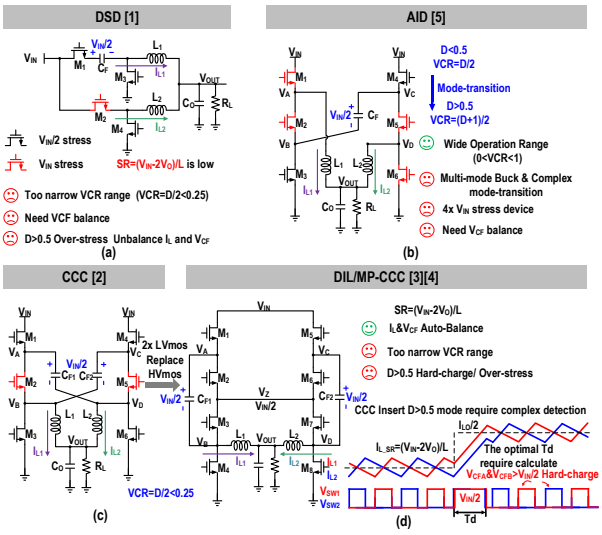


Fig. 1. (a) DSD (b) CCC (c) DIL/MP-CCC (d) AID.

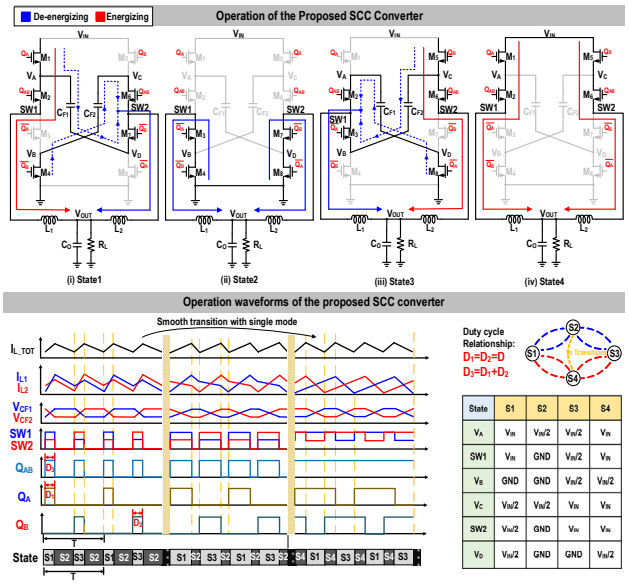
circuit is required during mode insertion. The asymmetrically implemented dual-phase (AID) converter [5] achieves a full 0-1 VCR, but it relies on complex mode transitions and employs more high-voltage devices, which increase implementation complexity and switching loss.

To address these limitations, this paper proposes a symmetric cross-coupled capacitor (SCC) two-phase buck converter. The proposed SCC converter achieves a continuous 0-1 VCR in a single operating mode, inherently balances both inductor currents and flying-capacitor voltages, and provides a higher effective current slew rate during load transients. These features make it well-suited for compact, high-efficiency battery-input power management systems.

II. The Proposed SCC Converter

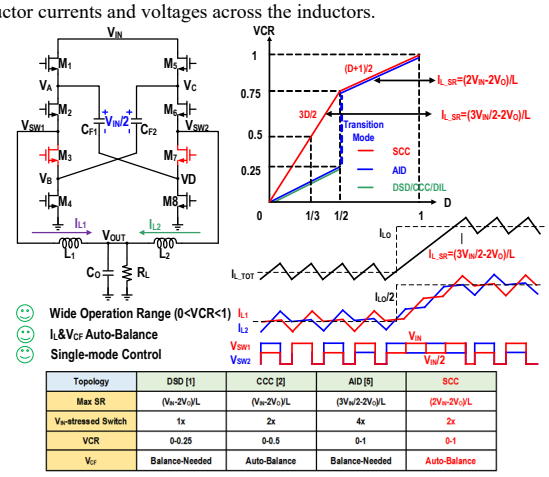
A. Converter Topology and Operating Principle

Fig. 2 illustrates the operation of the SCC converter over the full range of duty cycle D. The converter employs two 180° phase-shifted switching signals (Q_A, Q_B) to control eight switches, defining four states (S1, S2, S3, S4), where $Q_{AB} = Q_A + Q_B$. In state S1, C_{F1} is charged and C_{F2} is discharged by I_{L2}, resulting in switch-node voltages of V_{IN} and $V_{IN}/2$, respectively. Conversely, in state S3, I_{L1} discharges C_{F1} and charges C_{F2}, setting the switch-node voltages to $V_{IN}/2$ and V_{IN}. In state S2, both I_{L1} and I_{L2} are de-energized, whereas in state S4, both are energized. The SCC converter operates by



State	S1	S2	S3	S4
V_A	V_{IN}	$V_{IN}/2$	$V_{IN}/2$	V_{IN}
SW1	V_{IN}	GND	$V_{IN}/2$	V_{IN}
V_B	GND	GND	$V_{IN}/2$	$V_{IN}/2$
V_C	$V_{IN}/2$	$V_{IN}/2$	V_{IN}	V_{IN}
SW2	$V_{IN}/2$	GND	V_{IN}	V_{IN}
V_D	$V_{IN}/2$	GND	GND	$V_{IN}/2$

Fig. 2. Operation state and principle of the proposed SCC converter with inductor currents and voltages across the inductors.



Topology	DSD [1]	CCC [2]	AID [5]	SCC
Max SR	$(V_{IN}-2V_O)/L$	$(V_{IN}-2V_O)/L$	$(3V_{IN}/2-2V_O)/L$	$(2V_{IN}-2V_O)/L$
V_{IN}-stressed Switch	1x	2x	4x	2x
VCR	0-0.25	0-0.5	0-1	0-1
V_{CF}	Balance-Needed	Auto-Balance	Balance-Needed	Auto-Balance

Fig. 3. Comparison of the proposed SCC converter with previous converters.

combining subsets of the four states, enabling smooth transitions among operating regions as D increases and thereby achieving a continuous 0-to-1 VCR. Consequently, V_{CF} settles at $V_{IN}/2$ in all states, driving I_L and V_{CF} toward equilibrium (ΔI_L, $\Delta V_{CF} \rightarrow 0$). These mechanisms reduce conduction losses arising from both the AC and DC components of I_L across the full VCR range, as each inductor provides half of the load current (I_O), and the C_Fs reduce ΔI_L.

B. Current Slew Rate Enhancement of the SCC Converter

Fig. 3 compares the proposed SCC converter with prior hybrid DC-DC converters. The DSD converter [1] achieves a VCR of only 0-0.25. The CCC [2] extends the VCR to 0-0.5 by introducing a D > 0.5 operating condition. However, this mode must be forcibly inserted during load transients, which requires complex detection circuits, risks low-side switch overvoltage, and necessitates extra V_{CF} rebalancing afterward. The AID converter [5] achieves a full 0-1 VCR but relies on multi-mode operation with complex mode transitions and more high-voltage devices.

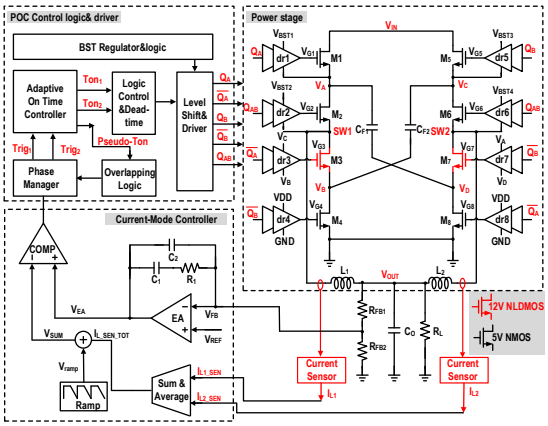


Fig. 4. SCC buck converter with pseudo-T_{ON} overlapping COT control.

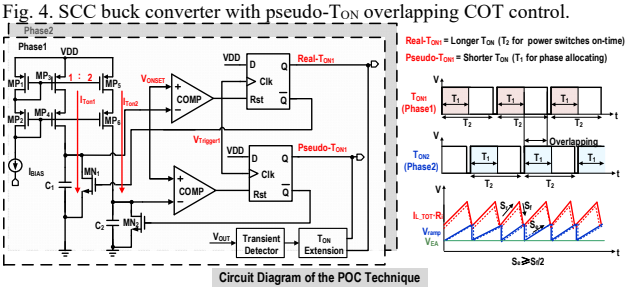


Fig. 5. Pseudo-T_{ON} phase overlapping technique: implementation circuit and operation waveforms.

In contrast, the SCC converter inherently features the S4 phase with two V_{IN} paths directly energizing the inductors, while the C_Fs remain floating, preserving their voltage balance. This eliminates the need for complex mode insertion required in the CCC. For VCR < 0.75, SR=$(3V_{IN}/2-2V_O)/L$, VCR = 3D/2, and for VCR > 0.75, VCR = (1 + D)/2, SR=$(2V_{IN}-2V_O)/L$. Owing to its symmetric cross-coupled architecture, the SCC achieves the highest current slew rate (SR) among the compared topologies, while only two switches sustain the full V_{IN} stress.

C. Pseudo-T_{ON} Phase-Overlapping Technique

Fig. 4 shows the overall architecture of the proposed SCC converter, including the SCC power stage and the current-mode constant-on-time (COT) controller. The power stage consists of eight power switches (M_1 to M_8, all N-type), two flying capacitors (C_{F1}, C_{F2}), and two inductors (L_1, L_2). M_3 and M_7 are implemented as 12 V HV MOSFETs, while the remaining switches are 5 V devices. On-chip bootstrap circuits drive M_1, M_2, M_5 and M_6. M_3 is powered by node V_C, M_7 is powered by node V_A, and the remaining low-side switches are driven by VDD (5 V). The converter employs a current-mode constant-on-time (COT) scheme with pseudo-T_{ON} overlapping and slope compensation. The error-amplifier output (V_{EA}) is compared with the ramp signal, and the gate-drive signals are generated by logic and driver circuits.

The proposed pseudo-T_{ON} overlapping control (POC) generates two on-time intervals from a single comparator trigger: a shorter interval T_1 fed to the phase allocator, and a longer interval $T_2 = 2T_1$ driving the power switches. Because the allocator releases control at T_1 while the power stage remains active until T_2, the subsequent phase is triggered

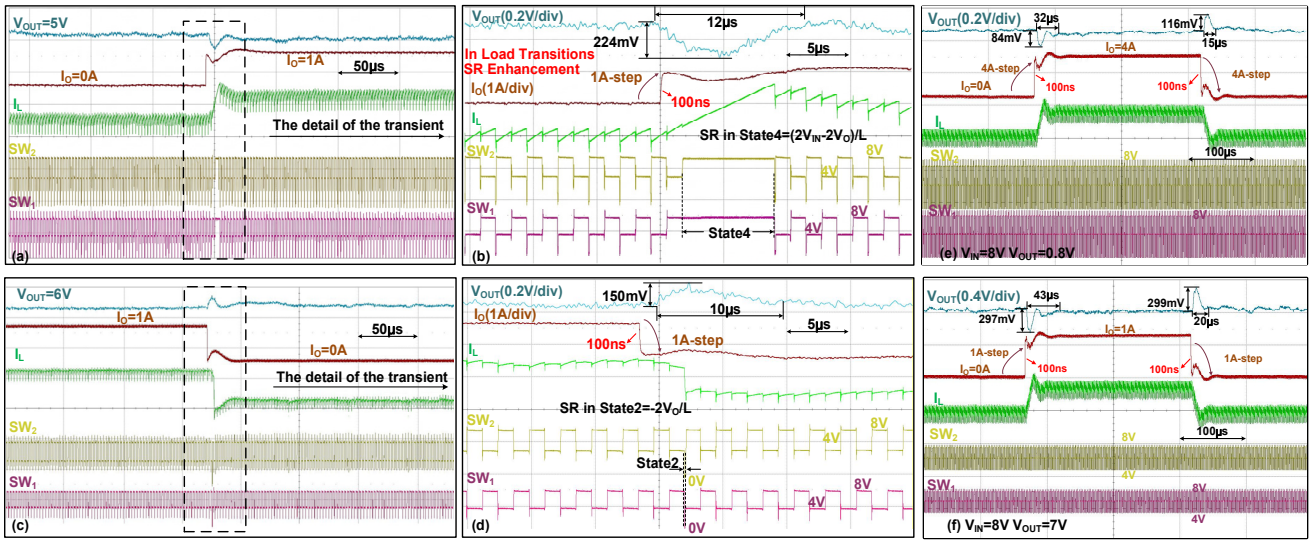


Fig. 6. Measured load transient responses with V_{IN}=8V. (a) I_O=0A↔1A, V_{OUT}=5V, (b) V_{OUT}=5V (zoom-in), (c) I_O=0A↔1A, V_{OUT}=6V, (d) V_{OUT}=6V (zoom-in), (e) I_O=0A↔4A, V_{OUT}=0.8V and (f) I_O=0A↔1A, V_{OUT}=7V.

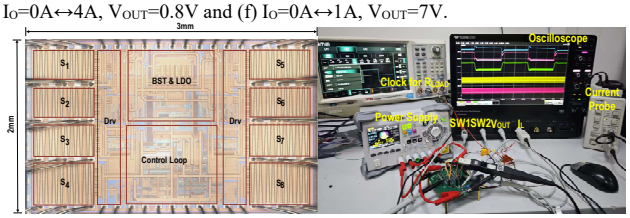


Fig. 7. Die micrograph and measurement setup.

before the current phase turns off, achieving seamless phase overlapping. During load transients, a dedicated detection circuit extends T_2 to prolong the overlapping interval, thereby enhancing the total inductor-current slew rate. To ensure stability in the overlapping region, adjustable ramp compensation with a slope satisfying $S_e \geq S_f/2$ is incorporated, which is consistent with the critical stability condition derived from discrete-time Nyquist analysis [6], [7]. The proposed POC allows the next phase to be activated before the current phase finishes conducting, thereby effectively enabling phase overlapping and extending the duty cycle.

III. Measurement Results

The proposed SCC converter was fabricated in a 0.18-μm BCD process. The die micrograph and the measurement setup are shown in Fig. 7. The chip occupies a 6 mm^2 silicon area. The prototype employs two 1 μH inductors with a 9-mΩ DCR, two 4.7-μF flying capacitors and a 10-μF output capacitor. The converter was measured under an input voltage of 6-8 V, a total switching frequency of 0.8 MHz, and an output voltage of 0.8-7 V. Fig. 6 presents the measured transient response under a load step. Fig. 6(a) shows the load transition waveform when V_{OUT} = 5 V under a 0-to-1 A load step, with Fig. 6(b) providing zoom-in views. As observed at the load step, the pseudo-T_{ON} phase-overlapping technique enables the converter to naturally enter the D>0.5 mode, bypassing state S2 and thereby improving the current slew rate for a fast transient response. The converter achieves a undershoot of 224 mV (4.5%) and a recovery time of 12 μs. Fig. 6(c) depicts the transient response at V_{OUT} = 6 V, with Fig. 6(d) presenting zoom-in views. During the heavy-to-light load transition, the converter re-enters state S2 to de-energize the inductors rapidly, resulting in an overshoot of 150 mV (2.5%) and a recovery time of 10 μs. Fig. 6(e) shows the transient response under the full 0-to-4 A load step at V_{OUT} = 0.8 V. The converter achieves an undershoot of 84 mV and an overshoot of 116 mV, with recovery times of 32 μs and 15 μs, respectively, demonstrating the effectiveness of the POC technique under demanding load conditions. Fig. 6(f) presents the transient at V_{OUT} = 7 V under a 0-to-1 A load step, where the undershoot and overshoot are 297 mV and 299 mV, respectively. The steady-state waveforms are presented in Figs. 8(a)-(e), including V_{OUT}, inductor currents (I_{L1}, I_{L2}, I_{L_TOT}), and the switch-node voltages of both phases (SW1 and SW2) under different voltage conversion ratios. Fig. 8(f) illustrates the start-up waveform showing that V_{OUT} reaches steady state within 1.5 ms.

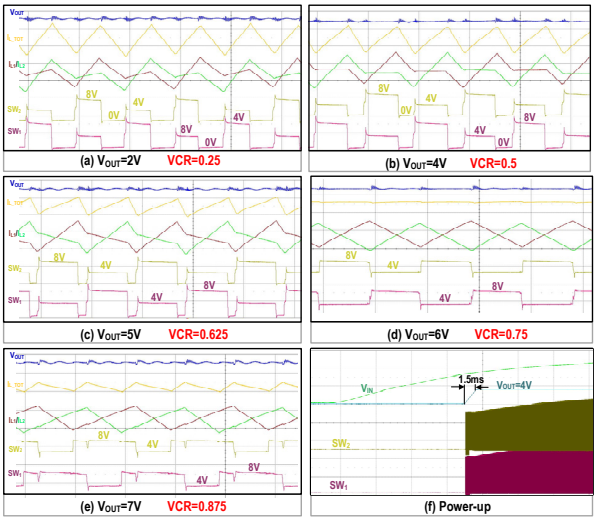


Fig. 8. Measured steady-state waveforms: (a) V_{OUT} = 2 V, (b) V_{OUT} = 4 V, (c) V_{OUT} = 5 V, (d) V_{OUT} = 6 V, (e) V_{OUT} = 7 V, and (f) start-up transient.

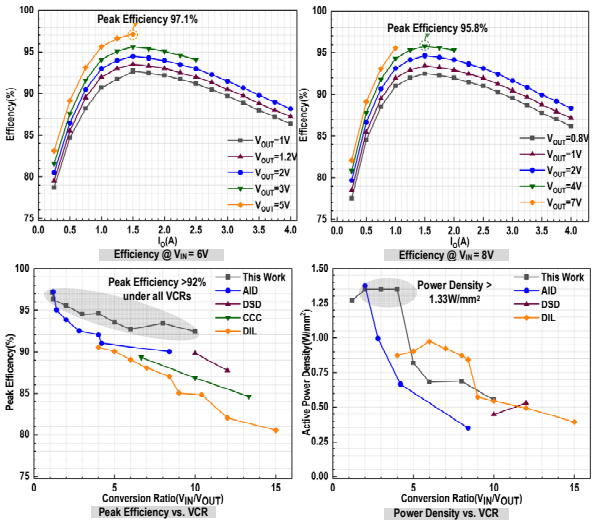


Fig. 9. Measured efficiency of the proposed converter and performance comparison with the prior works.

TABLE I. PERFORMANCE COMPARISON

Publication	TPE'21 [9]	ISSCC'23 [10]	JSSC'22 [1]	JSSC'23 [2]	ISSCC'24 [5]	This Work
Process	0.13μm	0.18μm	0.18μm	0.18μm	0.13μm	0.18μm
Topology	Three level	ReSC PL	DSD	CCC	AID	SCC
Die area	16.65mm²	8.88 mm²	9.6 mm²	2.8 mm²	2.318 mm²	6 mm²
Control	PWM	COT	PWM	SH	PWM	COT
V_{IN}	8V	12V	12-24V	12V	3.3-5V	6-8V
V_{OUT}	1.8-3.3V	0.6-1.2V	1-1.2V	0.9-1.8V	0.3-4.7V	0.8-7V
Max load current	N/A	5A	3A	4A	1.5A	4A
Frequency	0.8-1 MHz	0.8 MHz	1 MHz	2 MHz	2.5 MHz	0.8 MHz
C_{FLY}	4.7μF*2	20μF*2+10μF*2	4.7μF	2.2μF*2	10μF	4.7μF*2
C_{OUT}	N/A	100μF	12μF	10.6μF	10μF	10μF
Inductor	10μH	1μH	1.0μH*2	0.56μH*2	0.47μH*2	1μH*2
Undershoot/ Overshoot	N/A	152mV/180mV @4A step	165mV/N/A @3A step	190mV/210mV @4A step	118mV/125mV @1A step	84mV/116mV @4A step
Peak efficiency @VCR	88.60%@0.41	91.80%@0. 83	88.30%@0.1	86.8%@0.1	97.18%@0.857	97.10%@0.833 92.5%@0.1
Operation VCR Range	0-0.5	0-0.5	0-0.25	0-0.5	0-1	0-1

Fig. 9 shows the measured efficiency of the proposed converter and performance comparisons with the prior works. As summarized in Table I, the proposed SCC converter achieves a continuous 0-1 VCR within a single operating mode, thereby expanding the usable output-voltage range. Benefiting from the intrinsic self-balancing of inductor currents and flying-capacitor voltages, reduced I_{L_AC} and I_{L_DC} (lowering DCR losses), and the limited number of high-voltage devices, the proposed converter achieves high efficiency over a wide operating range. The prototype achieves peak efficiencies of 97.1% and 92.5% at VCR = 0.833 and 0.1, respectively, with overall efficiency exceeding 85% for load currents >0.5A. Under the control of the pseudo-T_{ON} phase-overlapping technique, minimum undershoot and overshoot of 84 mV and 116 mV, respectively, are achieved at V_{OUT}=0.8 V. The layout area is 6 mm², representing a 37.5% and 63.9% reduction compared with [1] and [9], respectively, which enables high power density (>1.25 W/mm²) across a wide operating range.

IV. CONCLUSION

This paper presents an SCC two-phase buck converter verified in a 0.18-μm BCD process. The proposed symmetric cross-coupled topology achieves a continuous 0-1 VCR within a single operating mode while inherently balancing both inductor currents and flying-capacitor voltages. The pseudo-T_{ON} phase-overlapping control enables loop-adaptive phase overlap, thereby improving the effective current slew rate and achieving fast transient response. Moreover, the reduced AC and DC components of inductor current minimize DCR losses, leading to a peak conversion efficiency of 97.1%. For load currents above 0.5 A, the overall efficiency remains above 85%. With an active die area of only 6 mm², the converter supports up to 4-A load current and achieves a power density exceeding 1.25 W/mm².

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China under Grant 62222406, Shaanxi Provincial Key Research and Development Program 2025CY-YBXM-051, the Fundamental Research Funds for the Central Universities and the Innovation Fund of Xidian University.

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