An Area-Efficient Reconfigurable Analog Baseband for 2x2 WLAN/Bluetooth SoCs

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***Abstract*— This paper presents a compact reconfigurable analog baseband (ABB) filter for 2x2 WLAN and Bluetooth (BT) transceivers fabricated in a 28-nm CMOS process. To minimize the silicon area typically dominated by passive components, a symmetric capacitor-sharing scheme is proposed, reusing the Rx ABB filter capacitors during both Tx normal and calibration operation. This technique reduces the Tx ABB area by 15% for WLAN and 80% for BT. Furthermore, an analog interpolating current-steering DAC is integrated to relax the Tx ABB filter order from 3rd to 1st. Specifically, the interpolating DAC achieves an initial 50% area reduction, and by applying the capacitor-sharing technique to the remaining footprint, a total area saving of 90% is ultimately realized for BT Tx ABB. The DAC also enhances image suppression by 14 dB. In the Rx path, a cross-coupled neutralizing capacitor technique extends the gain-bandwidth product, yielding a 5 dB IM3 improvement in the BT Rx filter. Measurement results confirm that the proposed ABB maintains strict error vector magnitude requirements, fully supporting 1024-QAM for WLAN and up to 8-DPSK for BT basic rate and enhanced data rate Class 1 applications.**

Keywords*— *Analog baseband filter, Capacitor sharing, Interpolating digital to analog converter, Neutralizing capacitor compensation, Reconfigurable RFIC, WLAN and Bluetooth transceivers

I. Introduction

Modern RFICs for wireless local area network (WLAN), Bluetooth (BT), and cellular applications face stringent power, performance, and area (PPA) constraints [1]-[5]. Within these transceivers, the analog baseband (ABB) filter is a critical bottleneck. Previously, several architectures such as digital transmitters, harmonic rejection mixers, and direct RF DACs have been proposed to alleviate the burden on the ABB filter. However, while these approaches succeed in reducing the ABB complexity, they inevitably shift the design and power burden onto other building blocks, failing to provide a fundamentally efficient area reduction for the ABB itself. Breaking this inherent limitation demands an innovative architecture.

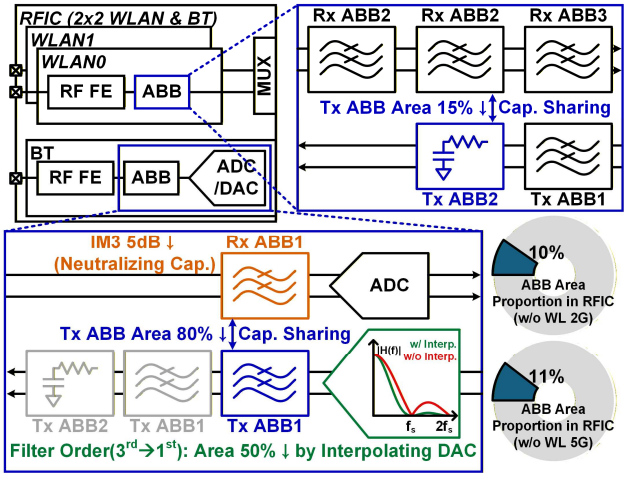

Fig. 1. Proposed architecture in RFIC.

To address this, we present a compact 28-nm CMOS ABB filter integrating three key optimizations, as illustrated in the overall block diagram in Fig. 1. First, time division duplex (TDD)-aware capacitor sharing reuses bulky capacitors between transmitter (Tx) and receiver (Rx) paths, drastically reducing passive area. Second, an analog interpolating current-steering DAC suppresses image signals, relaxing the Tx filter order and cutting area and bias current. Third, neutralizing capacitors explicitly cancel input parasitic capacitances, pushing the pole higher to maximize the gain-bandwidth product (GBW) and stability. By co-integrating these strategies, the proposed design achieves remarkable area reduction while fully supporting high-order modulations and maintaining an excellent error vector magnitude (EVM) performance.

The remainder of this paper is organized as follows: Section II details the proposed circuit techniques, Section III presents the measurement results of the fabricated prototype, and Section IV concludes the paper.

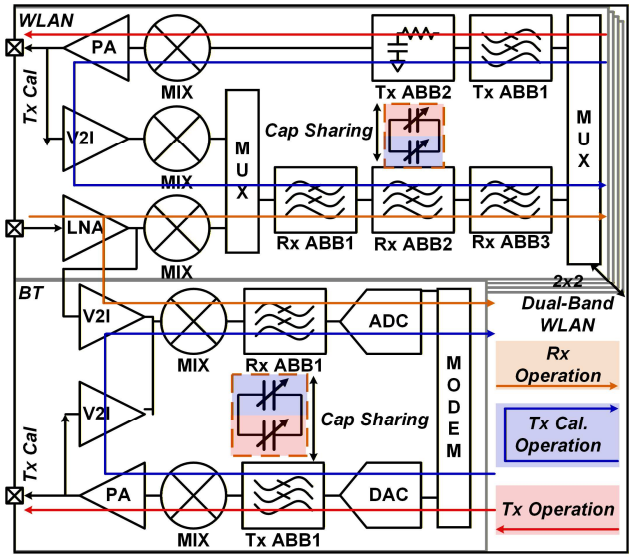

Fig. 2. RFIC top block diagram with operation mode.

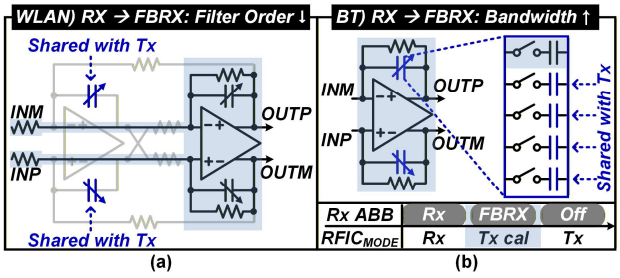

Fig. 3. Reconfiguration of the Rx ABB for Tx calibration: (a) WLAN Rx ABB2/3, (b) BT Rx ABB1.

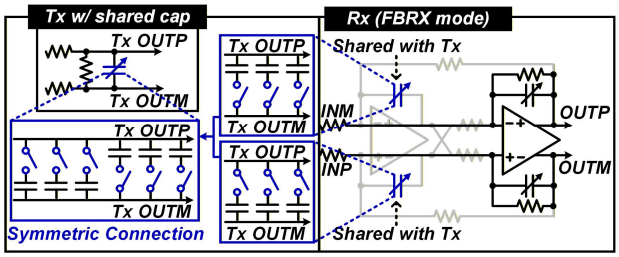

Fig. 4. Proposed symmetrical capacitor sharing connection.

II. Area-Efficient ABB Architecture

A. TDD-Aware Capacitor Sharing for Area Reduction

Since WLAN and BT operate in TDD mode as shown in Fig. 2, Tx and Rx paths are never active simultaneously. While reusing the Rx ABB as a feedback receiver (FBRX) for Tx calibration is common [6], full active-path sharing often necessitates complex, programmable OTAs to meet diverse bandwidth and linearity requirements. To minimize design

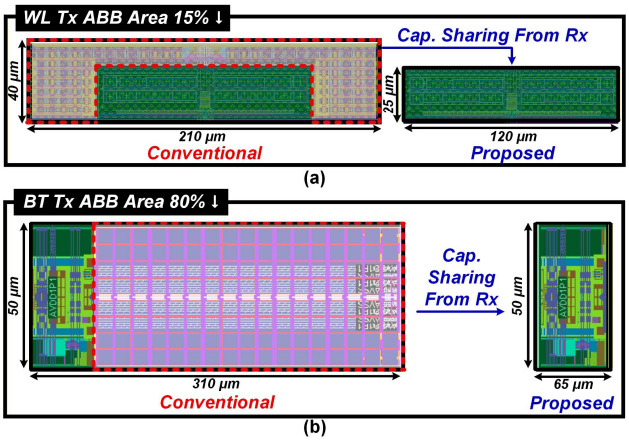

Fig. 5. Comparison of layout before and after applying capacitor sharing: (a) WL Tx ABB2, (b) BT Tx ABB.

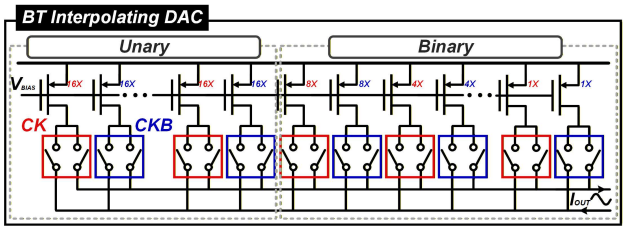

Fig. 6. Detailed schematic of the proposed BT interpolating DAC architecture.

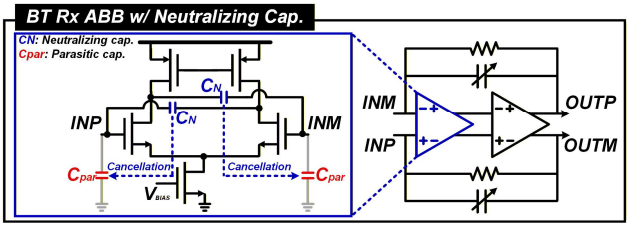

Fig. 7. BT Rx ABB block diagram with neutralizing capacitor.

complexity and power overhead, this work limits sharing to the passive capacitors.

In WLAN mode, the FBRX requires a lower filter order than the main Rx. As shown in Fig. 3(a), unused Rx capacitors are reallocated to the Tx path. Similarly, in BT mode, the bandwidth disparity between FBRX and Rx ABB enables significant capacitance reuse, as illustrated in Fig. 3(b). Fig. 4 illustrates the proposed symmetric sharing network, which ensures identical switching behavior across differential nodes, preserving signal balance and minimizing distortion. As shown in Fig. 5, layout-level validation confirms that this scheme reduces the Tx ABB area by 15% in WLAN and 80% in BT. Furthermore, to ensure isolation during Tx calibration, shared capacitors are cross-connected between WLAN0 and WLAN1 paths. This strategy suppresses direct Tx-Rx coupling without passive overhead, achieving a robust, compact ABB design.

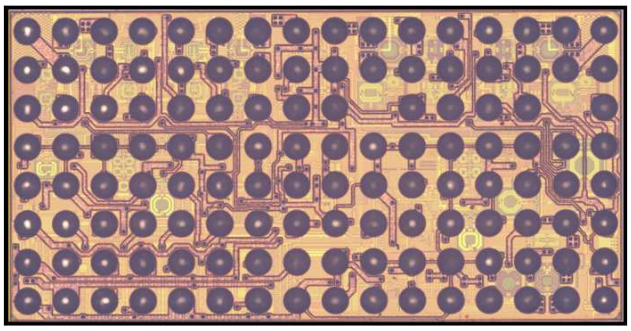

Fig. 8. Chip microphotograph.

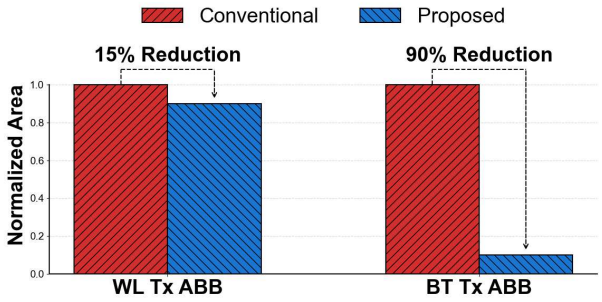

Fig. 9. Normalized silicon area comparison of the Tx ABB between the conventional and proposed architecture.

B. *Filter Order Reduction Using Interpolating DAC*

To satisfy BT enhanced data rate (EDR) Class1 adjacent channel power (ACP) and Federal Communications Commission (FCC) requirements without the area/power of high-order filters, an analog interpolating current-steering DAC is employed with duty-cycle correction (DCC) [7], [8]. As shown in Fig. 6, by utilizing both clock edges, the DAC inherently provides additional high-frequency attenuation near the sampling frequency. This inherent suppression significantly relaxes the required Tx ABB filter order from 3rd to 1st. Consequently, this approach achieves a 50% reduction in the active filter area along with decreased bias current, making it highly suitable for power-constrained connectivity RFICs.

C. *Neutralizing Capacitor for Performance Improvement*

While conventional Miller compensation ensures stability in ABB amplifiers by shifting the dominant pole, it reduces loop gain near the filter bandwidth, degrading linearity and usable bandwidth. To overcome this, a cross-coupled neutralizing capacitor is introduced between the first-stage input and output nodes of the two-stage trans-impedance amplifier (TIA), as illustrated in Fig. 7. This technique neutralizes parasitic capacitances, effectively pushing the problematic third pole to a higher frequency. Notably, this approach eliminates the inherent trade-off between stability, loop gain, GBW, and linearity that limits conventional designs. Unlike Miller compensation, it significantly improves phase margin, loop gain, GBW, and linearity simultaneously without any additional power consumption.

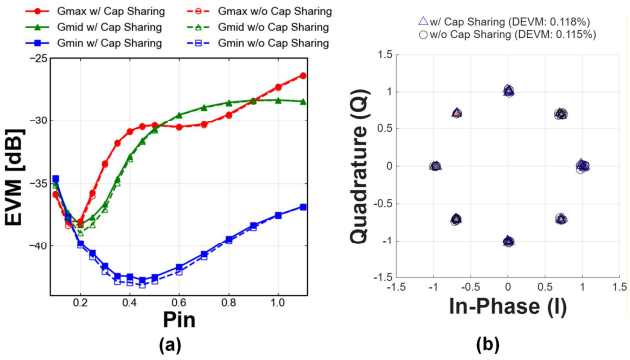

Fig. 10. Measured Tx EVM result with capacitor sharing enable and disable.

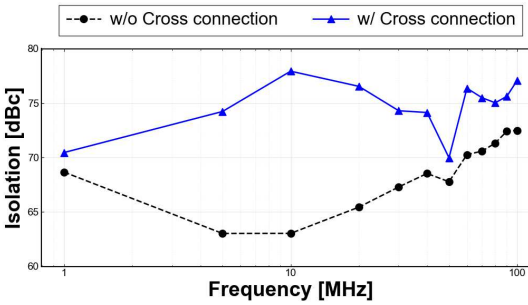

Fig. 11. Measured WL Tx-Rx isolation result with cross connection.

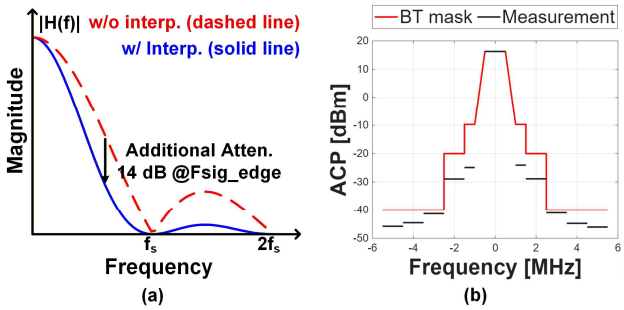

Fig. 12. Measured BT DAC results: (a) attenuation with interpolating enable and disable, (b) Tx ACP.

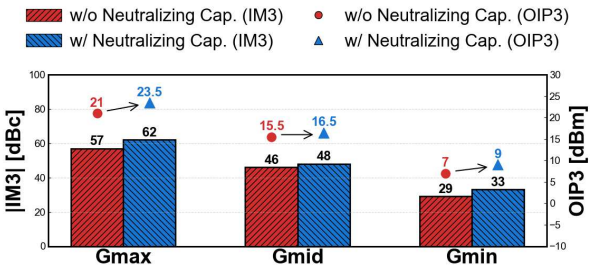

Fig. 13. Measured BT Rx ABB IM3 and OIP3 result with neutralizing enable and disable.

TABLE I. COMPARISON WITH STATE-OF-THE-ART WORKS

Specifications	**This work**	[1] ISSCC 2024	[2] ISSCC 2024	[3] ISSCC 2021	[4] VLSI 2020	[5] ISSCC 2019
Technology	**28nm**	14nm	14nm	14nm	14nm	14nm
Supporting mode	**WLAN 6E, BT 6.0**	WLAN 7, BT 6.0	2G, 3G, 4G,LTE-A, SA/NSA FR1 NR	2G, 3G, 4G, LTE-A, SA/NSA FR1 NR	2G, 3G, 4G, LTE-A, SA/NSA FR1 NR	2G, 3G, 4G, LTE-A, SA/NSA FR1 NR
RF Bandwidth (Hz)	**160M**	320M	100M	100M	100M	100M
Internal PA/LNA	**Yes**	No	No	No	No	No
Sensitivity (dBm)/NF (dB)	**-/4.3 (5G)**	-/4.3 (5G)	-101 (n28, 10M)/-	-100.8 (B20, 10M)/-	-101/-	-99.8 (B7, 10M)/-
Rx EVM (dB)	**-44.3***	-47.4*	-42 (n77,100M)	-37 (80M)	-31.7 (80M)	-33.6 (20M)
Tx EVM (dB)	**-44* @Pout=12dBm**	-46.3* @Pout=5dBm	-42 (n77,100M) @Pout=3.5dBm	-38 (n78) @Pout=7.2dBm	-34 (n77)	-34.24 (n77) @Pout=5dBm
Tx ABB Norm. Area**	**0.04**	0.19	0.13	0.53	0.97	0.80
BT Tx ABB Norm. Area***	**0.02**	0.28	N/A	N/A	N/A	N/A

* = MCS11(160M)
** Normalized area is calculated as Area / (Technology)^2 / (Filter Order) and includes both I and Q channels.
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III. Measurement Results

As illustrated in Fig. 8, the proposed reconfigurable baseband was fabricated in 28-nm CMOS. Measurements for both WLAN and BT operations were performed on packaged samples. As shown in Fig. 9, the combined techniques achieve significant Tx ABB area reductions of 15% in WLAN and 90% in BT (combining an initial 50% reduction from the interpolating DAC with an 80% reduction on the remaining footprint via the capacitor-sharing scheme). To evaluate the impact of this sharing, Tx EVM was measured under identical conditions. As depicted in Fig. 10, EVM is strictly maintained across both standards, confirming negligible performance degradation. Moreover, Fig. 11 demonstrates that the cross-allocation effectively mitigates Tx-Rx coupling.

Furthermore, the measured results in Fig. 12(a) confirm that the interpolating DAC suppresses image components by 14 dB. This reduces the required filter order from 3 to 1, cutting the active filter area by 50% while still complying with spectral masks, as verified in Fig. 12(b).

In the BT Rx path, as plotted in Fig. 13, neutralizing capacitors improve BT IM3 by 5 dB, mitigating distortion with zero power consumption. As summarized in Table I, the proposed Tx ABB itself achieves a remarkably compact size.

IV. Conclusion

This paper presented a compact reconfigurable ABB for WLAN and BT RFICs utilizing capacitor sharing, an interpolating DAC, and a neutralizing capacitor technique. 28-nm CMOS measurements confirm that these techniques synergistically improve area efficiency without performance penalty. Specifically, symmetric capacitor sharing reduces passive area while preserving Tx EVM and Tx-Rx isolation, yielding a 15% Tx ABB area reduction for WLAN. For BT, the interpolating DAC enables 90% area savings, while the neutralizing capacitor improves Rx IM3 by 5 dB without overhead power. As shown in Table I, this work achieves superior normalized Tx ABB area compared to state-of-the-art designs. Although internal PAs/LNAs limit the overall RFIC footprint reduction to 2%, the proposed architecture would deliver effective area savings in systems with external front-end modules. Future implementation of fully extended cross-connection schemes can maximize this area savings.

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