A D-Band Zero-IF 16nm FinFET Receiver with Embedded I/Q Mismatch Calibrations for 64-QAM Wireless Links

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***Abstract* — This paper presents a D-band zero-IF receiver (RX) using 16nm FinFET technology, leveraging its high RF performance. A FinFET wireless link is formed with the proposed RX and a customized transmitter (TX), which achieves 64-QAM with a maximum data rate of 36 Gb/s and an EVM of -22.7 dB. The RX consists of a carrier generation block with a frequency octupler, a RF block with a low-noise amplifier (LNA) and two passive mixers, and a baseband amplifier block. Meanwhile, a current-steering variable gain amplifier (VGA) and a digitally controlled artificial dielectric (DiCAD) transmission line are implemented on each of the I/Q paths to achieve on-chip amplitude and phase calibration for I/Q mismatches. The RX achieves a conversion gain (CG) of 33.5 dB, a 3-dB RF bandwidth of 126-143 GHz, a noise figure (NF) of 8.2 dB, and a total DC power consumption of 265 mW. The FinFET wireless link achieves an excellent efficiency of 59.9 pJ/bit/m.**

***Keywords* — FinFET, D-band, zero-IF, direct-conversion, 64-QAM, 16-QAM, receiver, RX, chip set, mm-Wave circuits.**

I. Introduction

The D-band frequencies are gaining increased attention for their potential wide bandwidth for beyond-5G communication. Also, recent advances in RF p-FinFETs have enabled their application in the D-band, thanks to their high f_{max} [1].

Reducing I/Q mismatch is essential for maintaining low error vector magnitude (EVM) in mm-Wave receivers (RXs). Recent works have demonstrated D-band RXs or full wireless links with high modulation indices [2]–[8]. However, they often rely on off-chip equalization or digital pre-distorsion, which increases system complexity. To address these issues, the proposed RX incorporates on-chip amplitude and phase calibration circuits that directly compensate for I/Q imbalance. This architecture allows precise mismatch calibration, ensuring robust operation for high-order modulation schemes.

The block diagram of the proposed zero-IF RX is shown in Fig. 1. The D-band carrier is generated on-chip by a frequency octupler. A differential coupler then produces the I/Q signals, which are routed to the calibration stage. Specifically, a current-steering variable gain amplifier (VGA) provides adjustable amplitude control, while a digitally controlled artificial dielectric (DiCAD) transmission line enables fine phase tuning. The input RF signal is amplified by a low-noise amplifier (LNA) and down-converted by two passive mixers. The baseband signal passes through a continuous-time linear equalizer (CTLE), followed by a buffer and an output driver.

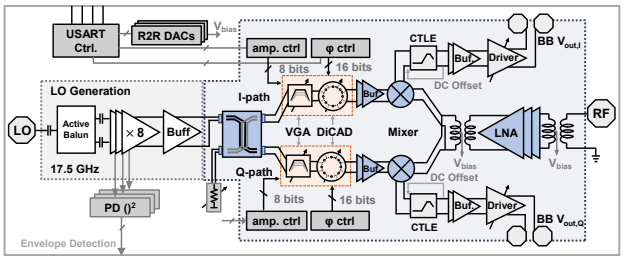


Fig. 1. Block diagram of the proposed D-band zero-IF RX.

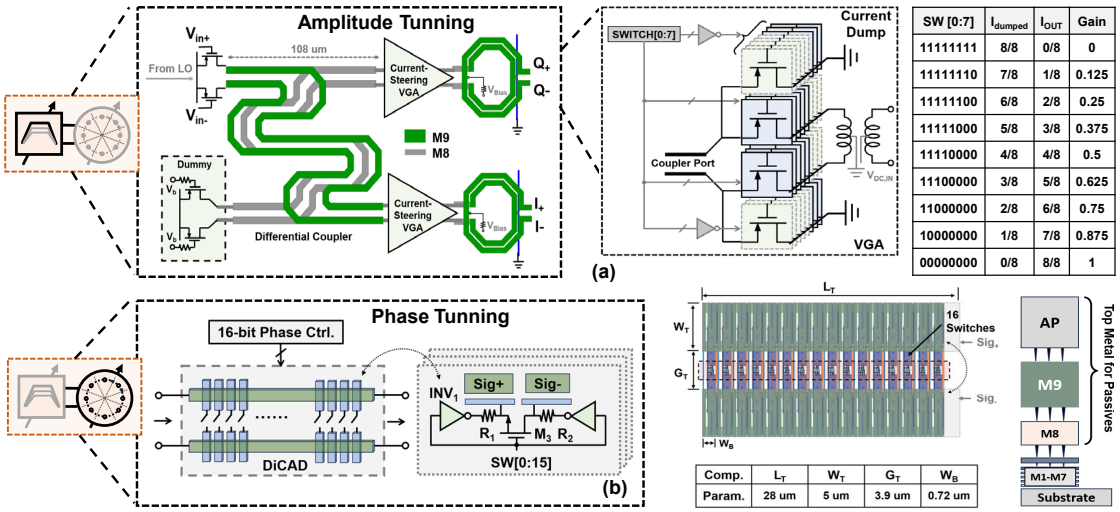
II. Receiver Circuit Design

A. LO Generation Block

The LO generation block employs an active balun to generate the differential signal and a frequency octupler to multiply the input Ku-band signal to the D-band [9]. The frequency octupler consists of three cascaded frequency doublers followed by a broadband LO buffer. Each doubler adopts a push–push topology with stacked p-FET devices to form a double-clipped current waveform, thereby improving the harmonic-generation efficiency. An output matching network with common-mode (CM) suppression is integrated at the balun center tap to minimize undesired CM coupling between stages. The final LO buffer delivers a differential 140 GHz signal with a harmonic rejection ratio exceeding 35 dBc, ensuring sufficient spectral purity and voltage swing for the following quadrature generation and mixer stages.

B. I/Q Mismatch Calibration Blocks

A current-steering VGA is implemented on each I/Q path to provide on-chip amplitude and gain control. The VGA consists of a differential coupled-line coupler followed by a cascode amplifier, where a current-steering transistor array controls the output amplitude by dynamically switching unit devices between the signal and ground paths, as shown in Fig. 2 (a) [9]. An 8-bit thermal code determines the number of active branches, enabling fine gain adjustment while maintaining an approximately constant Z_{load}. The structure minimizes parasitic capacitance and preserves bandwidth, achieving >17 GHz bandwidth. It allows independent amplitude tuning of the I and Q channels to suppress magnitude imbalance without requiring external equalization.



SW [0:7]	I_{dumped}	I_{OUT}	Gain
11111111	8/8	0/8	0
11111110	7/8	1/8	0.125
11111100	6/8	2/8	0.25
11111000	5/8	3/8	0.375
11110000	4/8	4/8	0.5
11100000	3/8	5/8	0.625
11000000	2/8	6/8	0.75
10000000	1/8	7/8	0.875
00000000	0/8	8/8	1

Comp.	L_T	W_T	G_T	W_B
Param.	28 um	5 um	3.9 um	0.72 um

Fig. 2. (a) Block diagram of amplitude tuning parts realized as current-steering VGAs, and the current gain under different control codes. (b) Block diagram of phase tuning parts realized as DiCAD and its HFSS model with medal stacks.

Phase mismatch between the I and Q channels is corrected by a DiCAD transmission line that provides tunable phase delay (Fig. 2 (b)). The DiCAD employs a differential transmission line with integrated switchable metal–oxide–metal (MoM) capacitors controlled by a 16-bit digital word [9]. Turning on additional capacitors increases the propagation delay ($\Delta\phi$), allowing a total tuning range of approximately 17° with approximately 1° phase resolution at 140 GHz. The DiCAD is implemented using top-metal layers, achieving less than 2 dB insertion loss across the D-band. Combined with the VGA, the DiCAD enables precise I/Q phase calibration, improving the overall EVM.

C. LNA, Mixer and Baseband Amplifiers

The RF front end consists of a three-stage LNA followed by two passive single-balanced mixers. Each LNA stage adopts a common-source topology with capacitive neutralization (Fig. 3 (a)-(b)). Interstage coupling is realized through low-coupling transformers, which extend the bandwidth. The amplified RF signal is then split and fed into two single-balanced passive mixers that directly convert the D-band input to baseband (Fig. 3 (c)). The overall LNA and mixer achieve a gain of 17.2 dB and a 3-dB bandwidth of 17 GHz, as plotted in Fig. 4 (a).

The baseband signal is amplified by a three-stage DC-coupled amplifier chain prior to the output, as shown in Fig. 3 (c)-(e). The first stage is a CTLE implemented as a common-gate amplifier with a tunable current source. A shunt capacitor provides high-pass filtering, with a current-absorbing transistor (M_1) placed in parallel with each load resistor to adjust the drain current and cancel DC offset, preventing error propagation to subsequent stages. This CTLE stage compensates for channel loss and extends the baseband bandwidth to support high symbol rates. The second stage is a three-stage self-biased transimpedance amplifier (TIA) acting as a buffer, providing approximately 26 dB gain to restore signal amplitude before the driver. The final driver stage employs a differential common-source topology with a tunable bias current and source degeneration resistor (R_{tune}), which improves linearity at the expense of gain. Integrated 50-Ω load resistors ensure broadband output matching. The simulated gain responses of each stage are shown in Fig. 4 (b), demonstrating a combined 3-dB IF bandwidth of 17.2 GHz.

III. Measurement Results

The D-band RX is fabricated using 16nm FinFET technology. The microphotograph and dimensions of the chip are shown in Fig. 5. Its total size is 1.4 × 0.78 mm (1.1 mm^2).

The RX measurement setup is shown in Fig. 6. For the continuous wave (CW) measurement, the RF input signal is generated by a commercial D-band frequency multiplier with 0 dBm Pout, followed by an attenuator for input power control (Fig. 6 (b)). The baseband outputs are connected to the spectrum analyzer or oscilloscope for frequency/time domain measurements. The CW simulation and measurement results are plotted in Fig. 7, where the RF bandwidth is measured under 1 GHz IF frequency, and the IF bandwidth is measured with 138 GHz RF frequency. The RX has a RF bandwidth of 17 GHz (126 GHz to 143 GHz) and a peak conversion gain (CG) of 33.5 dB (I path). The measured 3-dB IF bandwidth is 7.5 GHz, which is slightly lower than the simulation, due to the parasitics from the PCB traces and cables. The RX doubler-sideband (DSB) noise figure (NF) is measured based on the noise floor on the spectrum analyzer (FSA):

$$NF_{\mathrm{DSB}} \approx F_{\mathrm{SA}} - G_{\mathrm{RX}} - 10\log(kTB) - 3\,\mathrm{dB}, \qquad (1)$$

where G_RX is the measured CG of the RX and B is the resolution bandwidth of the spectrum analyzer (1 kHz). The simulated and measured DSB NF versus RF and IF frequency is plotted in Fig. 7 (c)-(d), where the lowest measured value

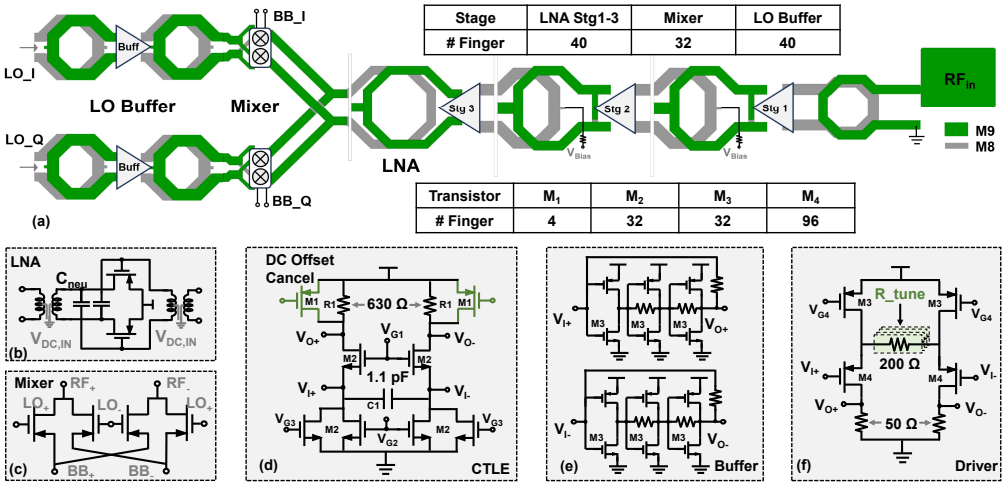


Fig. 3. (a) Layout of passive components of the RF blocks. Schematic of (b) LNA, (c) mixer, (d) CTLE, (e) baseband buffer, and (f) output driver.

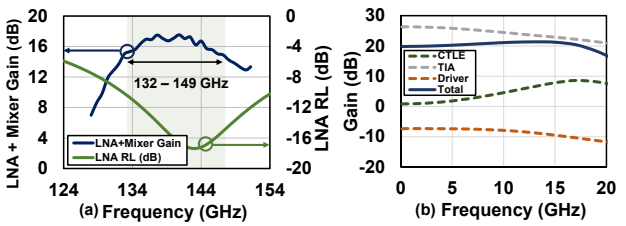


Fig. 4. (a) Simulated LNA and mixer gain and LNA's RL versus frequency. (b) Simulated baseband gain and its combined value versus frequency.

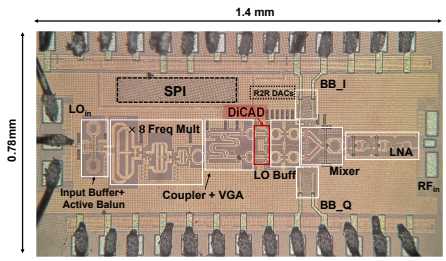


Fig. 5. D-band RX's chip photo with labeled components and dimensions.

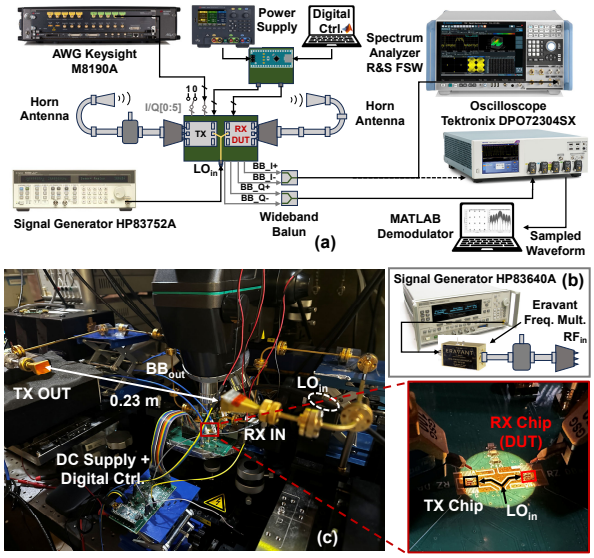
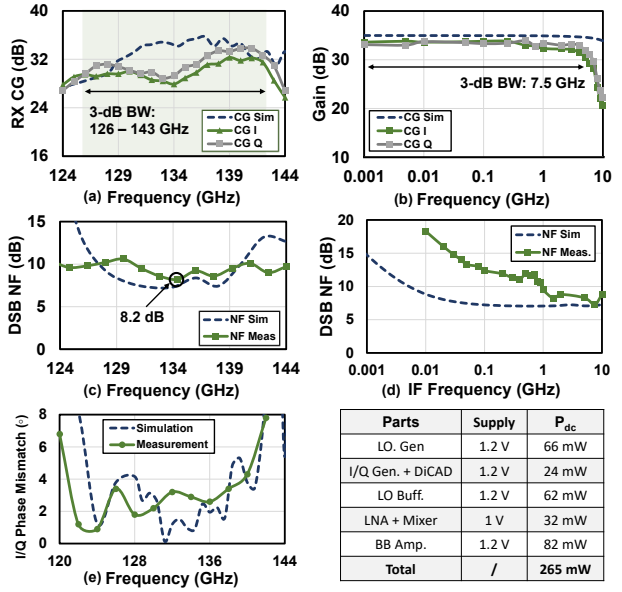


Fig. 6. (a) D-band wireless link OTA measurement setup. (b) D-band RX CW measurement and RF signal generation. (c) Photo of the OTA measurement.

at 1.5 GHz IF is 8.2 dB. The I/Q phase mismatch with the default setting is shown in Fig. 7 (e), and is below 5° from 124 GHz to 140 GHz. Then, the calibration is carried out using the on-chip VGA and DiCAD to reduce the I/Q mismatch to below 0.5 dB/ 1°. After the CW characterization, the over-the-air (OTA) data modulation measurement is performed by building a wireless link using a pair of synchronized transmitter (TX) and RX (Fig. 6 (a)). The customized FinFET TX delivers 12 dBm Psat and 235 mW DC power consumption, shares the same LO multiplication ratio [9]. Sharing the same LO source, the TX and RX form a coherent link, enabling phase noise cancellation, and the transmitted RF signal is directly down-converted to zero-IF. The TX output and the RX RF input are both probed and connected to a waveguide horn antenna at a 23-cm distance. A carrier frequency of 138 GHz is chosen for the optimum TRX performance. The TX's input bits are generated using an AWG, and the RX I/Q baseband outputs are sampled by an oscilloscope and processed using a MATLAB demodulation program that performs deeper equalization, plots the constellations, and calculates the EVM.

The data modulation test started with a symbol rate of 2 GS/s. The measured constellations for 16-QAM and 64-QAM are plotted in Fig. 8, where the EVMs are -26.7 dB and -23.5 dB, respectively. A root raised cosine filter is applied with α=0.5. The symbol rate is then raised to 6 GS/s, and the EVMs of 16-QAM and 64-QAM are -26.1 dB and -22.7 dB, respectively. The EVMs are limited by the signal-to-noise ratio (SNR) of the wireless link, and the data rate is limited by the



Parts	Supply	P_{dc}
LO. Gen	1.2 V	66 mW
I/Q Gen. + DiCAD	1.2 V	24 mW
LO Buff.	1.2 V	62 mW
LNA + Mixer	1 V	32 mW
BB Amp.	1.2 V	82 mW
Total	**/**	**265 mW**

Fig. 7. Simulated and measured RX CG for both I/Q paths versus (a) RF and (b) IF frequency. Simulated and measured DSB NF paths versus (c) RF and (d) IF frequency. (e) Simulated and measured I/Q phase mismatch and RX DC power breakdown.

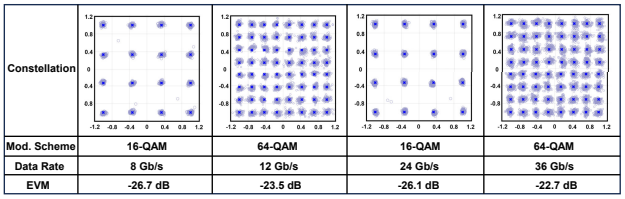


Fig. 8. Data modulation results with constellations and EVMs of the wireless link over a 23-cm OTA measurement.

overlapped bandwidth of the TX and RX.

The performance for D-band RX and wireless link is shown in Tables I and II, respectively. Compared to state-of-the-art CMOS D-band RXs, this work exhibits excellent NF and CG. The FinFET wireless link achieves a competitive data rate (36 Gb/s) and EVM (-22.7 dB) under 64-QAM, which leads to the highest link efficiency of 59.9 pJ/bit/m.

IV. Conclusion

This work presents a D-band zero-IF RX in 16nm FinFET technology. To mitigate I/Q imbalance, a current-steering VGA and a DiCAD transmission line are used for precise on-chip amplitude and phase tuning. The RX achieves a CG of 33.5 dB, 3-dB bandwidth of 126–143 GHz, and a DSB NF of 8.2 dB, while consuming 265 mW of DC power. A 23-cm FinFET wireless link formed with the paired TX demonstrates 64-QAM modulation with a data rate of 36 Gb/s and an EVM of –22.7 dB, achieving the highest efficiency of 59.9 pJ/bit/m. This work also demonstrates the feasibility of FinFET technology for next-generation mm-Wave/sub-THz wireless communication systems.

Table I. Performance Comparison between CMOS D-Band Receivers

References	Technology	CG (dB)	NF (dB)	RF BW (GHz)	Arch.	IP1dB (dBm)	P_{DC} (mW)	On-Chip I/Q Cal?	Aera (mm^2)
This work	**16nm FinFET**	**33.5**	**8.2**	**126-143**	**Zero-IF**	**-35***	**265**	**Yes**	**1.1/0.6****
ISSCC 2023 [2]	22nm FinFET	17	12.4*	119-141	Zero-IF	-15	166	No	4/0.7**
RFIC 2022 [3]	45nm SOI	15	10	140-158	IF@ 56-61	/	420	No	5.1
JSSC 2024 [4]	28nm CMOS	25	6	123-140	Direct Digital	/	175	No	3.6
CICC 2020 [5]	28nm CMOS	44*	8*	113	Zero-IF	/	500	No	4.7^
JSSC 2024 [6]	28nm CMOS	43.6	9.3	132-150	Zero-IF	-37	485	No	5.8^
JSSC 2025 [7]	65nm CMOS	20	9	114-170	IF@4-60	/	700	No	4.3
ESSCIRC 2022 [8]	28nm CMOS	58	7.8	127-145	Zero-IF	/	98	No	1.2**

*: Simulated value; **:Core area; #: Low bias; ^: Includes multiple elements.

Table II. Performance Comparison between CMOS D-Band Wireless Links

References	Tech.	OTA Distance	Link Interface	P_{DC} TX / RX (mW)	Modu. Scheme	DR (Gb/s)	EVM (dB)	Link Effi. (pJ/bit/m)
This work	**16nm FinFET**	**23 cm**	**Off-Chip Antenna**	**235 / 265**	**64-QAM**	**36**	**--22.7**	**59.9**
RFIC 2022 [3]	45nm SOI	3 cm	Off-Chip Antenna	600 / 420	64-QAM	48	-20	708.3
JSSC 2024 [4]	28nm CMOS	2 cm	Off-Chip Antenna	130 / 157	16-QAM	36	-18.4	365
CICC 2020 [5]	28nm CMOS	10 cm	Off-Chip Antenna	470 / 500	16-QAM	80	-15	121
JSSC 2024 [6]	28nm CMOS	30 cm	Off-Chip Antenna	521 / 485	16-QAM	48	-15.5	70
JSSC 2025 [7]	65nm CMOS	32 cm	Off-Chip Antenna	1468 / 700	128-QAM	56	-25.5	120.9

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