300~325GHz, 32-unit Dual-beam Phased Array TX with 24.3dBm EIRP and 7-bit DTC Beamformer

Zhiang Wang[1*], Yan Li[1*], Yinian Feng[1], Dixian Zhao[4,5], Zhi Chen[3], Bo Zhang[2], Cheng Wang[1]
1. School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu, China
2. Shenzhen Institute for Advanced Study, University of Electronic Science and Technology of China, Shenzhen, China.
3. National Key Laboratory of Wireless Communications, University of Electronic Science and Technology of China, Chengdu, China.
4. National Mobile Communications Research Laboratory, Southeast University, Nanjing, China.
5. Peng Cheng Laboratory, Shenzhen, China
Equally Credited Authors, Email: wangch87@uestc.edu.cn

***Abstract*—Massive swarms of UAVs or drones need accurate 3D environment sensing for navigation and collision avoidance. This work presents a 300~325 GHz, 32-unit, λ/2-spaced planar phased array transmitter (TX), supporting dual-beam scanning. Firstly, since higher effective isotropic radiated power (EIRP) is desired, an on-chip patch antenna, boosted by 100μm-thick quartz superstrate, improves the radiation efficiency to 50%. In addition, the RF power of two 300~325GHz frequency triplers are combined. An impedance equalizer (IEQ) is proposed to eliminate the amplitude & phase unbalance of the feeding network of two triplers. Secondly, the high precision beamforming is achieved through a 7-bit digital-to-time converter (DTC), consisting of a 5-bit floating-source coarse DTC and a 7-bit integration-mode phase interpolator (IMPI). The 7-bit DTC with a delay range of 0~3.17ps drives a ×9 multiplier chain for the 360° phase shifting at 315 GHz. Thirdly, two 16-unit (8×2) phased array TXs are stitched to be a 32-unit TX, supporting dual-beam scanning. Fabricated using 65 nm CMOS process and measured at 315GHz, the 32-unit TX achieves a EIRP of 24.3 dBm, a H-plane scanning angle of ±60°, and a 3-dB main-lobe of 5°. The dual-beam antenna pattern and the 300~320 GHz chirp are also validated.**

Keywords*—300GHz, phased-array, CMOS, on-chip antenna. frequency tripler with power combining ,7-bit DTC.

I. INTRODUCTION

The terahertz frequency band can provide high resolution for drone radar, making it a key technology for achieving fine target detection and recognition [1]. Phased array technology is the key to compensating for severe path loss in this frequency band [2-5] and maintaining an effective detection range for drones. But constructing a large-scale, λ/2-spaced phased array for drone platforms above 300 GHz faces multiple challenges. Under standard CMOS processes, the performance of high-efficiency radiating antennas and high-power frequency multiplier chains is limited, making it difficult to support the high-power transmission requirements needed for airborne radar detection [4]. Furthermore, the available chip area per array unit decreases sharply with λ^2, making it hard for traditional beamforming networks to balance low loss and compactness, and difficult to meet the stringent constraints on drone payload size, weight, and power consumption [2,3,5]. Although beam-steerable coupled oscillator arrays can achieve high EIRP [8], they suffer from limited frequency chirping speed, making them unsuitable for FMCW radar [6-9].

To address these issues, this work presents a 300~325 GHz, 32-unit, λ/2-spaced phased array TX fabricated in a 65 nm bulk CMOS process. As shown in Fig. 1, it consists of two 8×2 TX chips and supports dual-mode operation. In single-beam mode, the array can synthesize a high-gain beam, effectively compensating for path loss and supporting high-precision detection of a single long-distance target by the drone. In dual-beam mode, the system can simultaneously generate two independent beams, enabling parallel detection or rapid scanning of multiple short-distance targets. The Schematic of the 16-unit phased array TX chip is shown in Fig. 2. Each TX unit integrates a 7-bit DTC, S2D, two-stage ×3, DA, tripler with power combining and on-chip patch antenna with quartz substrate.

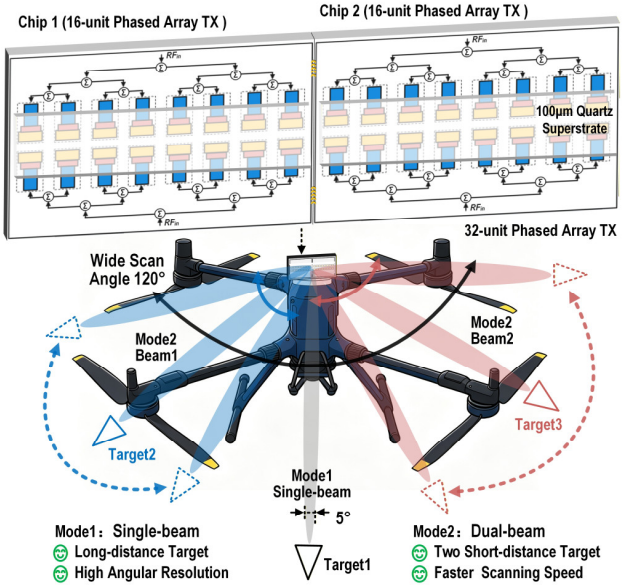

Fig. 1. 32-unit phased array TX for UAV-mounted radar.

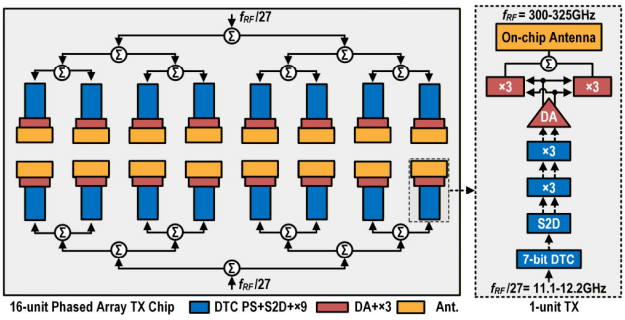

Fig. 2. Schematic of the 16-unit phased array TX chip.

II. PHASED ARRAY TRANSMITTER CIRCUITS

A. On-chip Patch Antenna with Quartz Superstrate

As shown in Fig. 3, this design proposes an on-chip patch antenna structure operating in the 315 GHz band, aiming to meet the requirements of high integration and efficient radiation performance for terahertz on-chip systems. The

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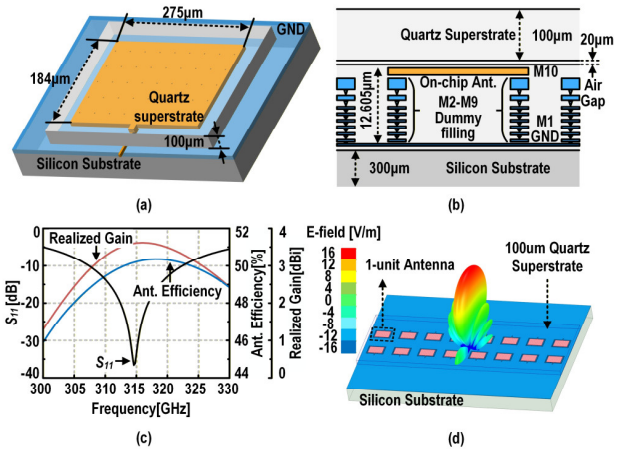


Fig. 3. On-chip patch antenna with quartz superstrate: (a)1-unit. (b). Cross section view. (c)Antanna simulation. (d) 16-unit.

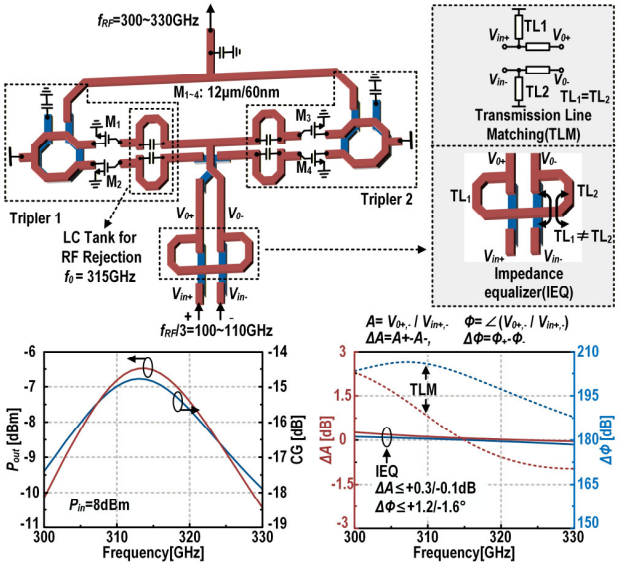


Fig. 4. Schematic of 300-325 GHz fequency tripler with power combining.

antenna uses the top aluminum metal layer (AP) in a 65 nm CMOS process as the radiating patch, with physical dimensions of 184 μm × 275 μm. To enhance radiation efficiency and suppress surface wave losses, a 100 μm thick quartz (SiO_2) superstrate without pattern is placed above the antenna structure. This dielectric layer offers low loss and high dielectric stability, making it suitable for high-frequency millimeter-wave and terahertz applications. After optimizing the structure with metal dummy filling technology, simulation results show that the antenna achieves a peak gain of 3 dBi at the target frequency, a peak radiation efficiency of 50%, and a bandwidth of 15 GHz for S_{11} below -10 dB.

B. 300~330GHz Frequency Tripler with Power Combining

This work designs a 300–330 GHz frequency tripler with power combining, whose circuit structure is shown in Fig. 4. It achieves high RF power output by combining two frequency triplers; however, the feeding network of the two triplers introduces amplitude and phase unbalances. Traditional transmission line matching (TLM) methods struggle to eliminate such unbalances and may even exacerbate them. To address this, this study compensates for

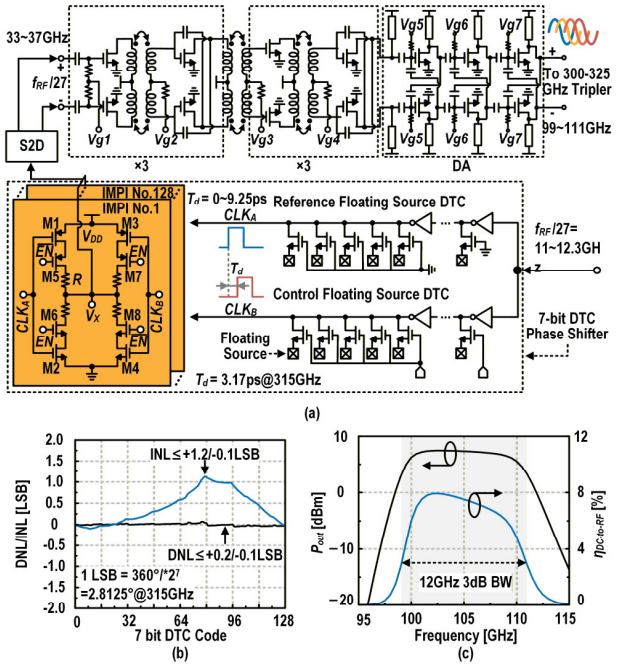


Fig. 5. Schematic of 7-bit DTC and ×9 multiplier chain.

the unbalance by designing an Impedance Equalizer (IEQ). The compensation mechanism lies in the actual position of the virtual ground established by the IEQ, which is determined by the degree of circuit unbalance and naturally produces a compensating effect at that location.. Additionally, an LC high-impedance resonant cavity centered at 315 GHz is integrated at the gate input of each frequency multiplier core transistor. This structure exhibits high impedance at the target frequency, significantly blocking the reflected power of the 315 GHz signal, thereby improving power transmission efficiency. Simulation results show that at P_{in}= 8dBm, the peak Pout can reach approximately -6.5 dBm, with a CG less than -18.5dB. The amplitude error is < +0.3/–0.1 dB, and the phase error is < +1.2°/–1.6°.

C. 7-bit DTC Phase Shifter and ×9 Multiplier Chain.

Based on VM-based high-frequency RF phase shifters suffer from issues of high loss and low precision [10]. Another approach involves cascading a low-frequency local oscillator phase shifter with an ×M frequency multiplier, but this imposes higher requirements on the phase shifter's phase-shifting accuracy [11]. To address this issue, as shown in Fig 5(a), this work designs an architecture that cascades a low-frequency, high-precision phase shifter with ×9 multiplier chain. Specifically, a 7-bit DTC phase shifter operates in the frequency range of $f_{RF}/27$ = 11~12.3 GHz, adopting a combined structure of a 5-bit coarse-tuning stage and a 7-bit fine-tuning stage. It uses a floating-source DTC to generate a clock signal with tunable delay (T_d) and employs a 128-unit integration-mode phase interpolator (IMPI) to achieve high-precision fine phase tuning [12]. The signal output from the DTC phase shifter is processed by Single-to-Differential (S2D) and then undergoes frequency multiplier chain through two-stage ×3 frequency multiplier, followed by power amplification through three-stage DA. To achieve 360° 7-bit resolution at 315GHz (1LSB=360°/2^7=2.8125°), the 5-bit coarse-tuning stage is adjusted such that T_d=3.17ps, resulting in a 7-bit DTC delay step of approximately 25 fs. The simulated integral nonlinearity (INL) and differential nonlinearity (DNL) are better than +1.2/-0.1 LSB and +0.2/-

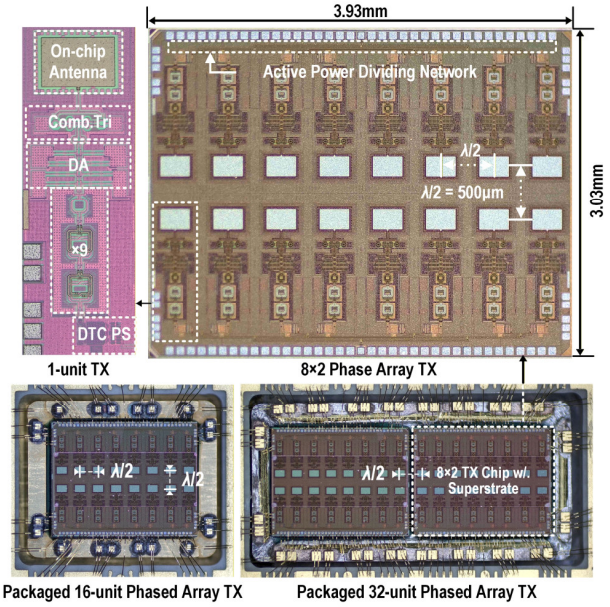
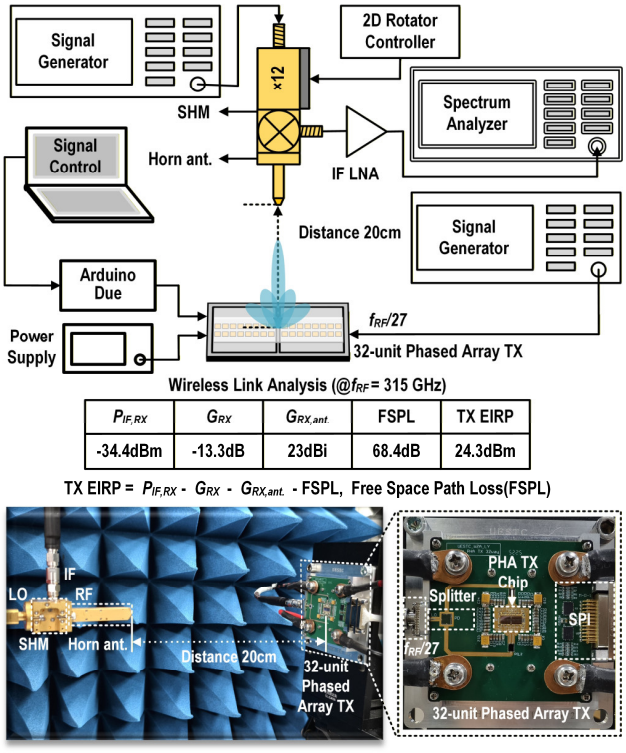


Fig. 6. Die micrograph, packaged 16-unit and 32-unit PHA.



Wireless Link Analysis (@f_{RF} = 315 GHz)

$P_{IF,RX}$	G_{RX}	$G_{RX,ant.}$	FSPL	TX EIRP
-34.4dBm	-13.3dB	23dBi	68.4dB	24.3dBm

TX EIRP = $P_{IF,RX}$ - G_{RX} - $G_{RX,ant.}$ - FSPL, Free Space Path Loss(FSPL)

Fig. 7. Setup for the RF performance characterization.

0.1 LSB, respectively. The output RF power of this ×9 multiplier chain can reach 7.5 dBm, with a 3 dB bandwidth of 12 GHz. The DC-to-RF conversion efficiency is up to 8%.

III. Measurement Results

This 8×2 transmit phased array chip is fabricated using a 65 nm bulk silicon CMOS process, with a chip area of 3.93 × 3.03 mm². The chip micrograph is shown in Fig. 5. Each transmit unit occupies 0.744 mm² and dissipates 158 mW of power. The packaged 16-unit and 32-unit phased array TX are also illustrated in Fig. 6, and Fig.7 presents the test setup for the RF performance characterization.

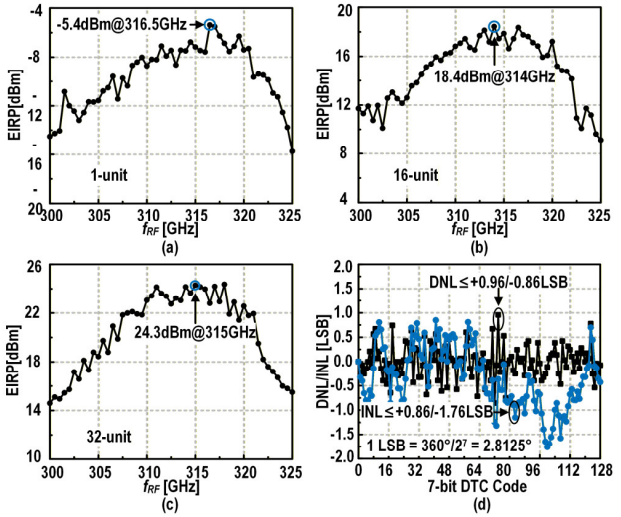


Fig. 8. Measured EIRP: (a) 1-unit TX, (b) 16-unit TX, (c) 32-unit TX, and (d) Linearity of 7-bit DTC phase shifter.

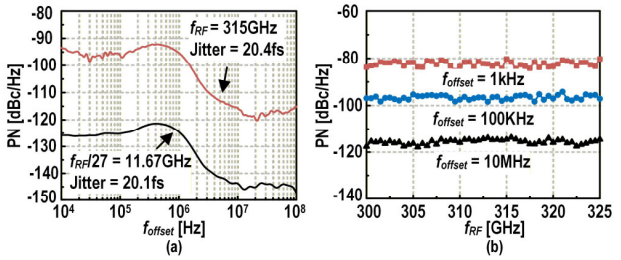


Fig. 9. Measurement results: (a) Jitter of f_{RF} = 315 GHz, (b) Phase noise.

Firstly, as shown in Fig. 8, The equivalent isotropic radiated power （EIRP） measured at f_{RF} = 300~325 GHz. The measured EIRP of 1-unit of the phased array TX is –16 dBm to –5.4 dBm, with a peak EIRP of –5.4 dBm at 316.5 GHz. For the 16-unit array, the EIRP ranges from 8 dBm to 18.4 dBm, with a peak EIRP of 18.4 dBm at 314 GHz; for the 32-unit array, the EIRP ranges from 14 dBm to 24.3 dBm, with a peak EIRP of 24.3 dBm at 315 GHz. Secondly, for a 7-bit resolution at 315GHz (1LSB=360°/2^7=2.8125°), the measured integral nonlinearity (INL) of the digital-time-converter (DTC) phase shifter is ≤+1.6/–1.0 LSB, and the differential nonlinearity (DNL) is ≤+0.5/–0.7 LSB.

Moreover, as shown in Fig. 9(a), the integrated clock jitter of this 16-unit TX array at f_{RF} = 315 GHz is 20.4 fs, and Fig. 9(b) presents the measured phase-noise (PN) curve. In addition, as shown in Fig. 10, the antenna patterns are measured at f_{RF} = 315 GHz. The H-plane and V-plane patterns of 1-unit of the phased array are shown in Fig. 10(a) and (b), respectively. The 16-unit phased array transmit achieves a scanning range of ±55° in the H-plane with a 3-dB main-lobe of 11° are shown in Fig. 10(c). While the 32-unit TX phased array realizes a scanning range of ±60° in H-plane with a 3-dB main-lobe of 5° are shown in Fig. 10(d). The normalized gain of the sidelobes is below -9 dB at all angles. It demonstrates excellent sidelobe suppression and beam control capabilities. Furthermore, Fig.11(a) is the antenna pattern at f_{RF}=315 GHz when the transmitter operates in dual-beam scanning mode and Fig. 11(b) displays the spectrum of 300~320GHz chirp signal.

TABLE I. PERFORMANCE COMPARISON WITH STATE-OF-THE-ARTS

	This Work		JSSC2026 [2]	RFIC2024 [3]	TMTT2016 [4]	T-TST2015 [5]	ESSERC2025 [6]	JSSC2022 [7]	JSSC2024 [8]	JSSC2015 [9]
Frequency [GHz]	300~325		236~266	263~279	374~407	310~320	366~386.4	412~419	643~689	320
TX Architecture	Phased Array Tripler-last		Phased Array Amplifier-last	Phased Array Mixer-last	Phased Array Tripler-last	Phased Array Mixer-last	Beam-steerable COA	Beam-steerable COA	Beam-steerable COA	Coupled Osc. Array(COA)
Array Size	16 (8×2)	32 (16×2)	4 (4×1)	4 (2×2)	8 (8×1)	4 (4×1)	16 (4×4)	16 (4×4)	144 (12×12)	16 (4×4)
Antenna Type	On-chip Patch Ant. + Superstrate		On-chip Vivaldi Ant.	Off-chip AiP	On-chip Patch Ant. + Superstrate	On-chip Slot Ring + Superstrate	On-chip Loop Ant.	On-chip Patch Ant.	On-chip Patch Ant.	On-chip Folded Slot Ant.
Ant. Spacing [λ]	0.5×0.5		0.59	0.54×0.54	0.5	0.9	0.35×0.35	0.5×0.5	0.5×0.5	0.5×0.5
EIRP [dBm]	18.4	24.3	16.2	-6.9	8	10.6	12.2	14	30.8	22.5†
Rad. RF Power [dBm]	3.4	6.3	N/A	N/A	-7	-2.4	0.45	-3	9.1	5.2†
H&V Beam Steering	±55° / N/A	±60° / N/A	±28°/ ±24°	±30°/ ±30°	±35°~40°/ N/A	±12° / N/A	-28°~+15°/-7°~+9°	±30° / ±30°	±45°/ N/A	N/A
Beamforming Arch.	LO DTC		LO STPS	LO&IF PS	LO VM	LO RTPS	N/A	N/A	N/A	N/A
PS Res. [bit]	7		N/A	N/A	3	N/A	N/A	N/A	N/A	N/A
P_{DC} / Unit [mW]	158		222	925	188	250	47	91	23.1	38.1
Area / Unit [mm²]	0.744		2.47	7.37	1.31	8.6	0.1	0.256	0.024	0.13
Technology	65nm CMOS		65nm CMOS	40nm CMOS	45-nm SOI CMOS	0.13-μm SiGe BiCMOS	40nm CMOS	65nm CMOS	65nm CMOS	0.13-μm SiGe BiCMOS

† Measured With A hemispherical silicon lens.

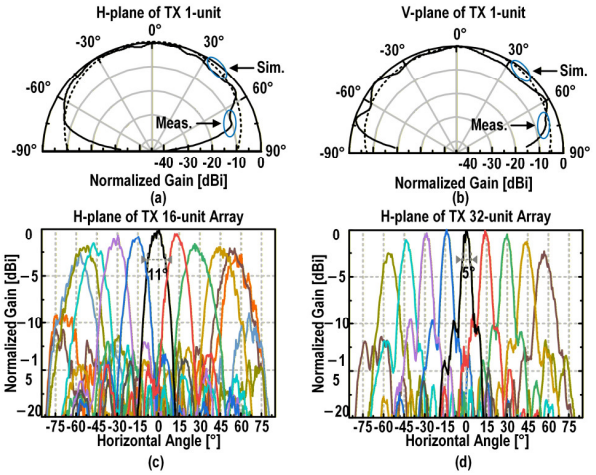


Fig. 10. Measured antenna pattern at 315 GHz: (a) H-plane of 1-unit. (b) V-plane of 1-unit. (c) H-plane of 16-unit. (d) H-plane of 32-unit.

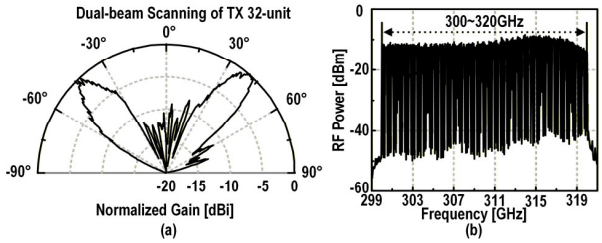


Fig. 11. Measurement results: (a) Dual-beam antenna pattern at 315 GHz. (b) Spectrum of 300~320GHz chirp signal.

IV. CONCLUSION

This work presents a 300~325 GHz, 32-unit, λ/2-spaced planar phased array transmitter (TX), supporting both single/dual-beam operation modes. Beamforming is achieved using a 7-bit DTC phase shifter that exhibits integral nonlinearity (INL) and differential nonlinearity (DNL) better than +0.86/−1.76 LSB and +0.96/−0.86 LSB, respectively. The packaged 32-unit phased array achieves a peak EIRP of 24.3 dBm. It provides a beam-steering range of ±60° in the H-plane. Table I compares this work with other state-of-the-art designs. Compared to phased arrays, this work demonstrates the strongest scale, EIRP, and radiation RF power. In comparison with coupled oscillator arrays, its EIRP is also highly competitive, and it enables rapid chirp while achieving a larger beam-steering angle.

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