A 67 dBc SFDR Baseband Digital Waveform Generator Employing Stochastic Calibration for Multi-Qubit Control

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***Abstract*— This paper presents a baseband digital waveform generator comprising a direct digital frequency synthesizer (DDFS) and a current-steering (CS) digital-to-analog converter (DAC). Stochastic calibration scheme is proposed to address both static and dynamic nonlinearities in multi-qubit control applications. The proposed architecture utilizes only a single DDFS with pulse-accumulating memory, enabling compact multi-tone frequency generation and 40 % reduction in area compared to conventional designs. Fabricated in 65 nm CMOS, the prototype confirms the multi-qubit operation and the effectiveness of the proposed calibration method, achieving a spurious-free dynamic range (SFDR) up to 66.88 dBc at 90 K. The power consumption with single channel is 2.68 mW per qubit for the analog part and 57.31 mW in total for the digital part, measured at room temperature.**

Keywords*— *Digital-to-analog converter (DAC), direct digital frequency synthesizer (DDFS), stochastic calibration, spurious-free dynamic range (SFDR), multi-tone generation, qubit controller.

I. Introduction

Quantum computing has attracted significant attention due to its potential advantages over classical computers [1]. A digital arbitrary waveform generator (AWG) is employed to generate desired baseband waveforms for qubit control. As the scaling of quantum computing systems has become crucial for realizing practical applications, frequency-division multiplexing (FDM) is considered a promising solution for maximizing the number of controllable qubits [2]. However, employing FDM poses several challenges, including increased bandwidth requirements and strict spurious-free dynamic range (SFDR) specifications. To address these challenges, the AWG must be capable of generating multiple frequency tones, either individually or simultaneously. Prior works have often configured multiple channels in parallel, at the cost of area [2], [3], [4]. Furthermore, the nonlinearity of these controllers is critical, as it deteriorates interference between frequency channels, which worsens with increasing frequency. Therefore, calibration of the current-steering (CS) digital-to-analog converter (DAC) is essential, as mismatches between unit current sources are the primary contributors to DAC nonlinearity [5], [6].

In this work, a baseband digital qubit control signal generator and DAC with stochastic calibration scheme are proposed to support a scalable (multi) qubit control system. As shown in Fig. 1, the baseband qubit controller is composed of a direct digital frequency synthesizer (DDFS), a 12-bit CS DAC, and calibration logic. Instead of employing multiple DDFS modules, only a single DDFS core with a pulse-accumulating memory is used. To further compensate the nonlinearity of the DAC, a sinc^{-1} filter is applied to equalize the DAC output signals over the entire system bandwidth. A stochastic calibration technique is implemented to monitor and adjust current sources in the DAC, comprising a calibration path that includes an additional low-pass filter (LPF) and a comparator. The rest of this paper is organized as follows: Section II describes the architecture and operations of the proposed controller, Section III presents the measurement results, and Section IV concludes the paper.

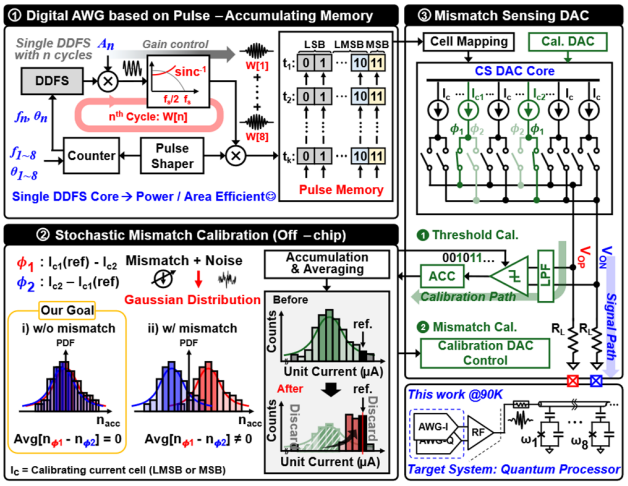

Fig. 1. Overall architecture of pulse-accumulating memory-based DDFS and stochastic calibration DAC for qubit control.

II. Baseband Qubit Controller

A. DDFS using Pulse-Accumulating Memory

To generate multiple frequency tones targeting FDM of qubits, a typical approach, shown in Fig. 2 (a), is to allocate parallel core DDFS modules for each qubit frequency. Since the pulse-shaping is applied to the waveform output, the final output (D_{OUT}) is a composition of pulse-shaped frequency tones. The resulting number of DDFSs is proportional to the number of target qubits, which significantly increases both area and power consumption accordingly.

The proposed architecture with a single DDFS is illustrated in Fig. 2 (b). Instead of using multiple DDFS modules, a shift register that stores temporal waveform data is implemented as a pulse-accumulating memory to improve power, performance, and area (PPA) efficiency. Given the information of frequency, phase, and amplitude required for

This work was supported in part by the National Research Foundation of Korea (NRF) grant (RS-2025-02217987, RS-2025-00516839, and RS-2025-24533292, RS-2025-16063688).

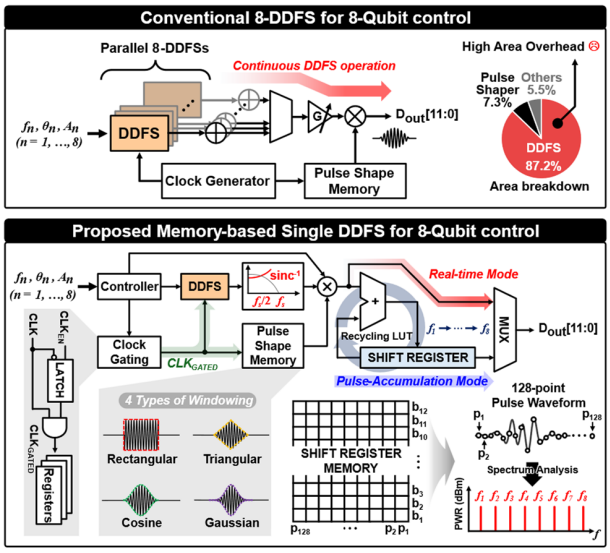

Fig. 2. Architectures of the conventional (top) and proposed pulse accumulation memory-based DDFS (bottom).

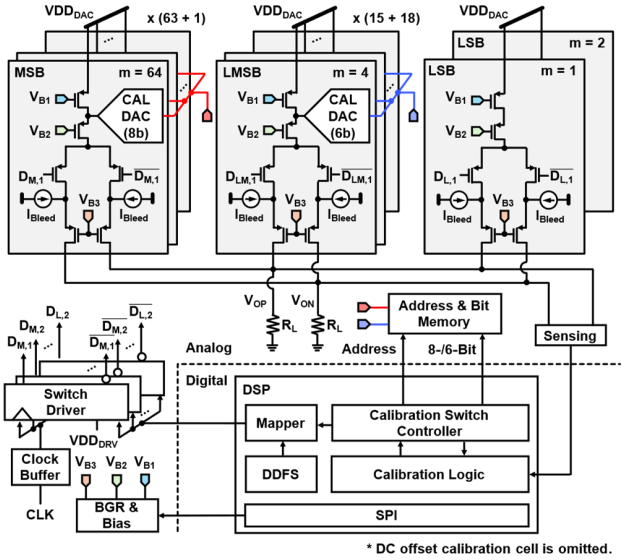

Fig. 3. Current cell structure of the CS DAC with auxiliary calibration cells.

each qubit, the DDFS sequentially generates corresponding signals in each operating cycle. The pulse-shaping module is applied in each cycle, where one of four types in rectangular, triangular, Gaussian, and cosine shapes is multiplied by the original output from DDFS. After the prior waveform is generated and stored in the shift register memory, an accumulator updates the waveform data, which is the sum of the prior and current waveform points. By the end of eight iterations at maximum, the final output points stored in memory represents signal containing multiple frequency components up to eight. Compared with parallel implementation, the total core area is reduced by 40 %, eliminating redundant hardware resources. A 12-bit resolution, a total of 128 data points can be stored in the accumulating memory. The clock-gating module deactivates the DDFS core after waveform generation, and the shift register drives the next stage DAC. Additionally, a pre-distortion based on the sinc^{-1} function compensates for the DAC frequency roll-off to balance signal power over the Nyquist frequency range.

B. DAC Structure

Fig. 3 presents the architecture of the CS DAC used in the proposed controller. The 12-bit DAC comprises segmented unary MSB (6-bit), LMSB (4-bit), and binary LSB (2-bit) arrays, with additional current-source banks for calibration. The MSB array consists of 64 current cells, with one reserved for calibration, and the LMSB array consists of 33 current cells, with 18 reserved for calibration. A current-cell mapper determines which cells are used for the main operation and which are used for calibration. During calibration, the target current cell is replaced by one of the spare current cells, without interrupting the main operation of the DAC. Each current cell is driven by a switch driver within the cell. The unit currents of the two LSB arrays are set to one-quarter and one-half of the LMSB unit current to obtain additional resolution, while enabling a smaller device size. Each unit cell incorporates bleeding current sources to improve linearity, along with 8-bit and 6-bit CAL DACs for the MSB and LMSB arrays, respectively, at the expense of higher current consumption. During DAC operation, dummy current cells not used in either operation or calibration are switched in a complementary manner to mitigate switching noise and DC offset. A memory storing cell addresses and calibration bits, and the digital logic required for output sensing and calibration, are also implemented to control the CAL DAC. On-chip functionality is configured and controlled via a serial peripheral interface (SPI).

C. Calibration Algorithm

As discussed in Section I, a mismatch between current cells is the fundamental performance-limiting factor in CS DAC, leading to degradation in SFDR, integral nonlinearity (INL), and differential nonlinearity (DNL). Previous works proposed for calibration of mismatch in CS DACs [7],[8] have often introduced an additional switch path that detaches each current cell from an output node, where each cell is compared with a dedicated reference current source. However, an inherent limitation of these calibration methods is the discrepancy between the calibration phase and the actual operating environment, which compromises detection accuracy.

The proposed stochastic calibration flow applied in this work is illustrated in Fig. 4. Compared with prior works, no additional switching path to disconnects the target cell from the main signal path is required. Instead of adjusting the unit current compared to the fixed reference current source, the reference cell is selected among the current cell banks in each array of the DAC. The calibration process is as follows. Two unit cells are first arbitrarily selected and connected differentially to the input of the comparator. The calibration switches and the dynamic comparator are clocked at an operating frequency 32 times slower than the DAC operating speed. Although an absolute comparison of the two current cells is deterministic, a DC offset between differential output nodes (V_{OP} and V_{ON}) may cause a false detection of the comparator. To avoid this, the comparator threshold is adjusted during the first calibration state (S_1). The comparator output is determined by the difference between the output voltages of the two current cells, of which the interpolation resistors and LPF filters the high-frequency components, which are further cancelled by averaging at the off-chip post-processing step.

During each phase (ϕ_1 or ϕ_2), the two current cells are compared N times, and an on-chip counter accumulates the

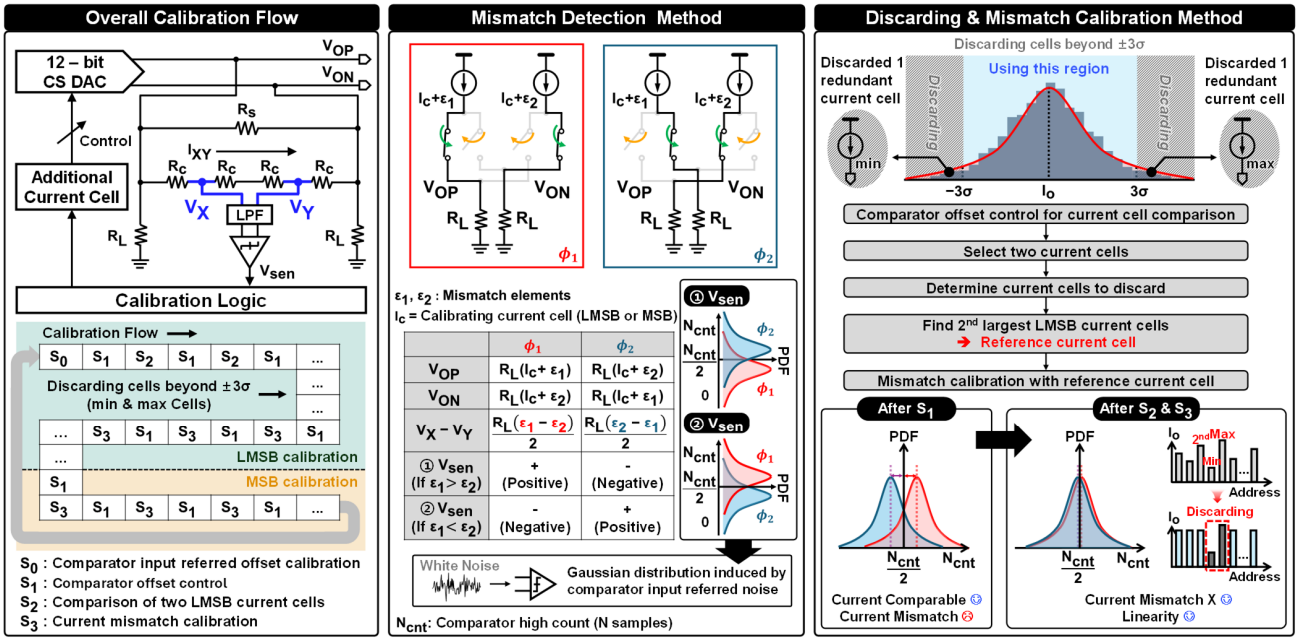

Fig. 4. Proposed stochastic mismatch calibration algorithm: (left) overall flow of the calibration process, (middle) mismatch detection method, and (right) discarding-based mismatch calibration procedure.

number of logic-highs in each phase. Without the noise from the comparator, the sum of counter outputs would always be higher in the phase in which the larger current is connected to V_{OP}. However, if the mismatch between the two current cells is hardly distinguishable, as the difference is not sufficiently large compared with the input-referenced noise, the comparison result may be inaccurate due to the presence of white noise. To mitigate the effects of circuit noise, comparisons are iterated N times per comparison cycle, repeated, and averaged M times externally at each phase. Consequently, the possible range of the counter value in each phase is from 0 to N, and the number of data points is M, which is averaged for the final decision.

Similarly, in S_1 and S_2, the two cells are compared at each phase to evaluate the relative magnitude of the unit current. The target reference cell is chosen to be the second-largest current cell, which is determined during S_1. This limits the required calibration range for the CAL DAC and additional current banks by excluding the largest and smallest from the main operation. Once the reference cell is fixed, the remaining current cells are compared, and the CAL DAC compensates for current mismatch based on the comparator output results during S_2. In practical implementation, the tunable range and calibration accuracy are limited when the reference current cell has a large value, which is often insufficient to be compensated by existing calibration cells.

III. Measurement Results

The proposed signal generator was fabricated using a 65 nm CMOS process, and Fig. 5 shows the die micrograph. The total area, including the IQ channels and the RF block, was 4.28 mm², and the DAC core area, including the memory required for CAL DAC operation, was 0.0672 mm² per channel. Due to constraints in the measurement setup, the cryogenic environment was limited to 90 K, and only one of the IQ channels was utilized for characterization. The measured total power consumption of a single channel is 78.73 mW at 90 K under a sampling rate of 0.4 GS/s and a supply voltage of 1.2 V. Fig. 6 shows the cryogenic experimental setup and measured eight-tone output spectrum using cosine pulse-shaping, with and without sinc^{-1} compensation.

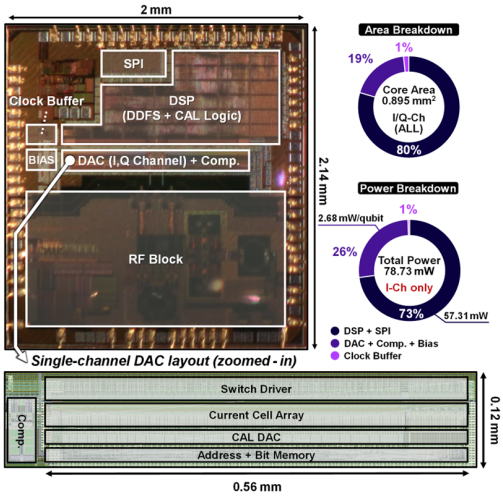

Fig. 5. Chip photograph with area and power breakdowns.

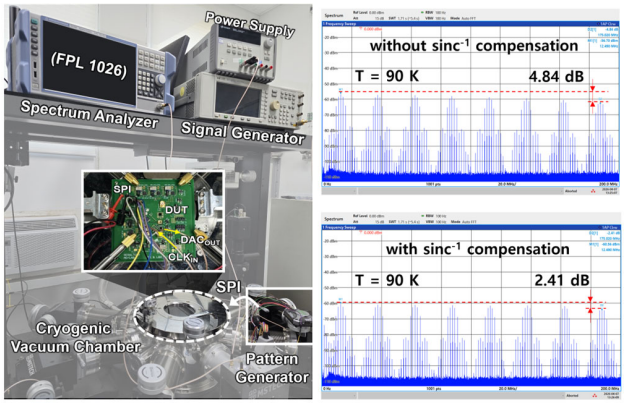

Fig. 6. Cryogenic measurement setup and 8-tone output spectrum using cosine pulse shaping, shown with/without sinc^{-1} compensation.

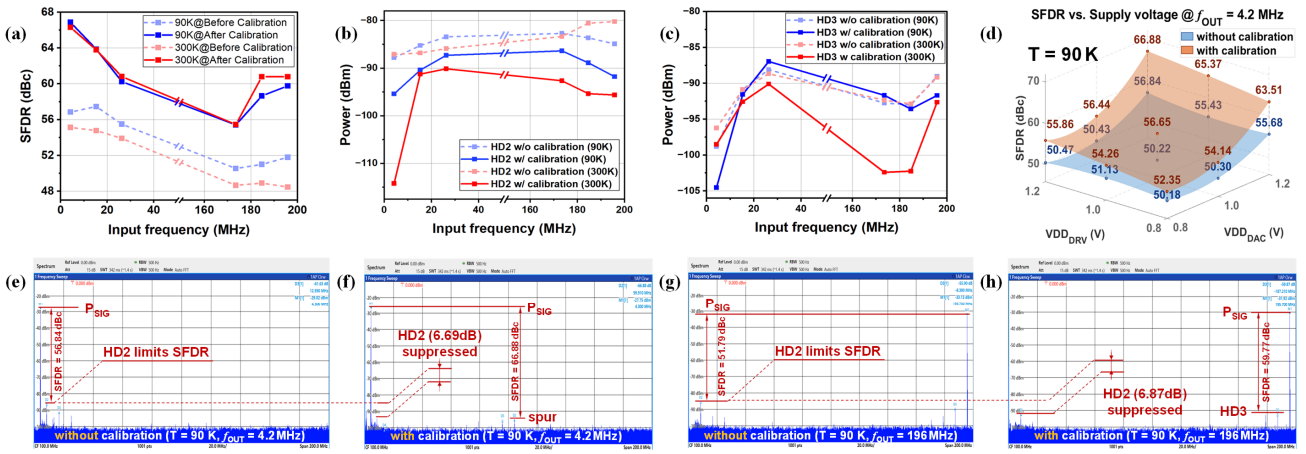

Fig. 7. Measurement results: (a) comparison SFDR at 300 K and 90 K, (b) and (c) HD2 and HD3 power with/without calibration (d) SFDR on DAC, switch driver supply voltage, (e) and (f) frequency spectrums with/without calibration (f_{OUT} = 4.2 MHz, f_S = 400MHz), (g) and (h) frequency spectrum with/without calibration (f_{OUT} = 196 MHz, f_S = 400 MHz).

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

		[2]	[9]	[10][a]	This work[b]
Process Technology		22 nm FinFET	40 nm CMOS	110 nm CMOS	65 nm CMOS
Operating Temperature (K)		3	77	4	90
Qubit Multiplexing		32	1	N/A	8
On-chip DDFS Architecture		LUT	LUT	N/A	Recycling LUT (for Pulse ACC)
Waveform points		upto 40960	Pre-defined	N/A	128
DAC Architecture (Segmentation)		CS (5b+5b)	Nonlinear CS (4b+4b+int.)	CS (5b+3b+4b)	CS (6b+4b+2b)
Resolution (bits)		10	9	12	12
Sampling Rate (GS/s)		1	≈ 2	0.2	0.4
$SFDR_{Peak}$[c] (dBc)		> 45[d]	N/A	57.9 @4.7 MHz	66.88[e] @4.2 MHz
Power (mW)	**Analog**	1.7/qubit	2.9/qubit	< 22	2.68[f]/qubit
	Digital	330	2.6/qubit		57.31
Area (mm^2)		4	0.39	< 0.21	4.28

[a] DAC only [b] DDSF and DAC only. Only a single-channel is measured.
[c] Single-tone SFDR [d] measured at RF output (note that [2] includes whole TX chain.)
[e] With calibration (Without calibration: 56.84 dBc) [f] Single channel

Fig. 7 presents the measured results of the proposed circuit. Fig. 7(a) shows the SFDR characteristics with and without stochastic calibration, measured at 300 K and 90 K. The peak SFDR is significantly improved up to 66.88 dBc at 4.2 MHz. The suppressed HD2 and HD3 are respectively reported in Fig. 7(b)–(c), where they are reduced by up to 27.1 dB and 9.38 dB, respectively. Single-tone output spectrums at both low frequency and near-Nyquist frequency are also presented. The SFDR dependence on the supply voltages of the DAC driver (VDD_{DRV}) and current cells (VDD_{DAC}) is shown in Fig. 7(d). Fig. 7(e)–(h) show the single-tone spectrums at low and near-Nyquist frequencies (with and without calibration), measured at 90 K. Table I provides a performance summary of the proposed qubit controller compared with prior works, including cryogenic DACs. The proposed controller utilizes a DDFS architecture that recycles LUTs to reduce the area required for multiple signal generation. Employing the CS DAC structure with 6b+4b+2b segmentation, this work achieves the peak SFDR of 66.88 dBc after applying the proposed calibration. The analog power consumption including the DAC drivers and current cells is 2.68 mW per qubit, and the digital controller consumes 57.31 mW in total.

IV. CONCLUSION

This work presents a baseband waveform generator with stochastic calibration targeting multi-qubit control for quantum computing. The pulse-accumulating memory-based DDFS enables compact multi-tone frequency generation for up to eight qubits, achieving a 40 % area reduction over conventional designs. The measurement results at 90 K show a peak SFDR of 66.88 dBc, validating the proposed calibration method of indirect sensing of current mismatch in cryogenic environments.

ACKNOWLEDGMENT

The chip fabrication and EDA tool were supported by the IC Design Education Center (IDEC), Korea.

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