A Programmable Cryo-CMOS Dynamic Comparator Using Forward Body Biasing

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***Abstract*—This work presents a dynamic comparator in a 65-nm bulk CMOS technology that works at both room temperature (RT) and cryogenic temperature (4 K). To mitigate the increase in threshold-voltage (V_{TH}) at 4 K, Forward Body Biasing (FBB) is applied via off-chip bulk control. A programmable reservoir-capacitor scheme reduces the effective supply voltage during the decision phase, enabling lower-energy operation. Measurements at 4 K show that combining bulk-bias control with switched-supply programmability enables input-referred noise (IRN) tuning from 19.8 μV to 117.4 μV. The proposed comparator achieves a FoM of 0.2–0.8 at RT and 0.01–1.1 at 4 K.**

***Index Terms*—Cryo-CMOS, dynamic comparator, forward body biasing, input-referred noise, energy efficiency.**

I. Introduction

Large scale quantum computers, with over 1000 qubits, will require Cryogenic (Cryo) CMOS controllers capable of integrating multiple qubit readout channels with the lowest possible power dissipation. Successive-Approximation-Register (SAR) Analog to Digital Converters (ADC) capable of operating at 4 K with low power dissipation have been extensively reported [1], [2]. However, most of these designs should still scale their power dissipation by about 10x. Comparators are known to be the most power consuming analog block in the SAR ADC, and its noise and power dissipation study at cryogenic temperatures is a must to build efficient converters. Earlier works have presented the modeling and characterization of a few cryogenic comparators. In [3], a calibrated PDK model is used to design a strong-arm comparator, which was characterized at 4 K as both standalone and as part of a SAR ADC. Later in [4], a modified BSIM model is used to emulate the shift in sub-threshold slopes (SS) and threshold voltage (V_{TH}) from RT and 4 K, with these models a benchamark between the typical comparator architectures such as strong-arm, dual tail, triple latch feedforward and their proposed one was presented. More recently in [5], the authors also used a custom modified PDK for cryo and presented a benchmark between the principal comparator architectures based on silicon experimental data. Since V_{TH} shift is one of the main limitations at 4 K, FBB has recently been shown to compensate for this effect in a floating-inverter amplifier (FIA) and in digital blocks [1]. In this work, FBB is applied to compensate for the cryogenic V_{TH} shift in a dynamic comparator. Moreover, to meet the stringent cryogenic power and noise requirements, the programmable switch-supply dynamic comparator of [6] is adopted, which is well suited for low-noise and low-power operation. The rest of the paper is organized as follows: Section II describes the proposed comparator, while Section III deals with the measurement results. Section IV draws some conclusions.

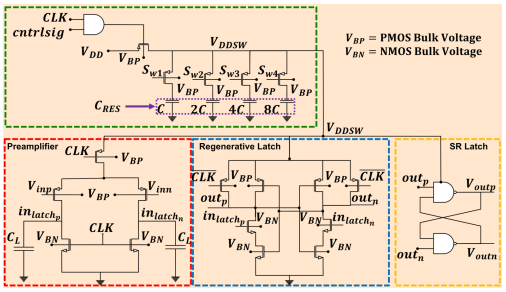

Fig. 1. Proposed Programmable Cryo-CMOS Comparator Using FBB.

II. Proposed Cryogenic Dynamic Comparator

Fig. 1 shows the proposed programmable Cryo-CMOS dynamic comparator. The architecture is derived from the programmable switched-supply comparator in [6]. Because the V_{TH} increases significantly at deep-cryogenic temperatures [7], this work employs off-chip bulk control to externally bias the NMOS and PMOS bulks (V_{BN}/V_{BP}), enabling FBB to partially recover the nominal V_{TH} at 4 K. Moreover, in agreement with the state-of-the-art for conventional non-cryogenic dynamic comparators, body-bias control has been shown to reduce comparator delay by lowering the effective V_{TH} and increasing device transconductance [8]. Therefore, in the proposed cryogenic implementation, bulk biasing is used not only to compensate for the V_{TH} shift induced by low-temperature operation, but also to improve the transient response of the comparator. A programmable reservoir-capacitor array, with binary-weighted control signals (S_{w1}, S_{w2}, S_{w3}, S_{w4}), reduces the effective supply voltage during evaluation, enabling lower-energy operation. To further mitigate the increase in low-temperature V_{TH}, the design uses low-threshold-voltage (LVT) devices and minimum channel length (60 nm) to maximize regeneration strength. A PMOS input differential pair is adopted to reduce sensitivity to low-frequency noise mechanisms that can become more pronounced at cryogenic temperatures [9]. To enable FBB, both NMOS and PMOS transistors use a deep-N-well in the layout [1]. Fig. 4(a) shows the layout of the proposed dynamic comparator, occupying an area of 118.5 μm $\times$ 46.78 μm.

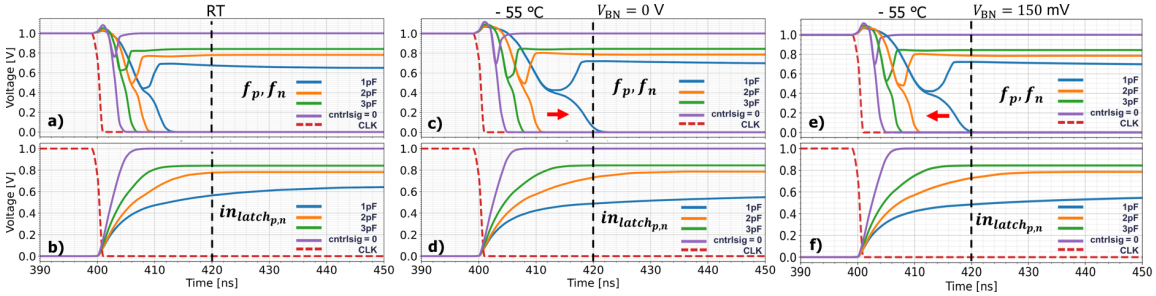

Fig. 2. Simulated timing waveforms for (a-b) RT operation, (c-d) -55 °C operation with $V_{BN} = 0$ V, and (e-f) -55 °C operation with $V_{BN} = 150$ mV.

To illustrate the operation of the FBB scheme and programmable switched-supply technique, transistor-level simulations were carried out at RT and at -55 °C, the edge of the validity of the foundry supplied model. Simulations were performed using V_{DD} = 1 V, clock frequency CLK = 5 MHz, 200 μV input differential voltage, V_{CM} = 350 mV. Fig. 2 shows the time-domain waveforms of the CLK, preamplifier outputs ($in_{latchp,n}$), and latch outputs ($f_{n,p}$). Compared to RT waveforms shown in Fig. 2(a) and (b), the -55 °C waveforms in Fig. 2(c) and (d), show slower transitions due to the increase in V_{TH}, which reduces overdrive and slows both pre-amplification and regeneration. By applying a bulk voltage of $V_{BN} = 150$ mV, Fig. 2(e) and (f) show that the latch signals tend to recover the delay observed at RT, shifting to the left for each reservoir capacitance (C_{RES}) configuration. Several studies have reported increased delay at cryogenic temperatures [5], which is one of the main reasons for degraded performance under cryogenic operation. The energy behavior as a function of C_{RES} is consistent with [6]; as C_{RES} decreases, the energy consumption is reduced. To emulate the main cryogenic effects without a dedicated cryogenic PDK, DC gate-bias sources in series are applied in simulation to the devices of the dynamic comparator, reproducing the effective V_{TH} increase by reducing overdrive. The results show that the IRN is much more sensitive to V_{bTHN} than to V_{bTHP}, indicating that the latch NMOS devices are the most noise-critical elements under cryogenic-induced V_{TH} shifts. (Figures omitted due to space limitations).

III. Measurements

The comparator was implemented in 65 nm CMOS technology. The chip micrograph is shown in Fig. 4(b), where the location of the proposed dynamic comparator is highlighted. Measurements were made using a PCB for cryo-testing as showed in [10]. The chip was mounted on a copper bridge and silver paint was applied to improve thermal contact as showed in Fig. 4 (c). Measurements were made in a Bluefors LD-4K cryostat. Since the long cryostat cabling can introduce additional perturbations, the input stimulus lines were low-pass filtered to attenuate out-of-band noise and reduce measurement artifacts. A power supply HMP4040 provided V_{DD}, a Keysight 33500A waveform generator generated the clock, and a Stanford Research Systems SR1 generated the

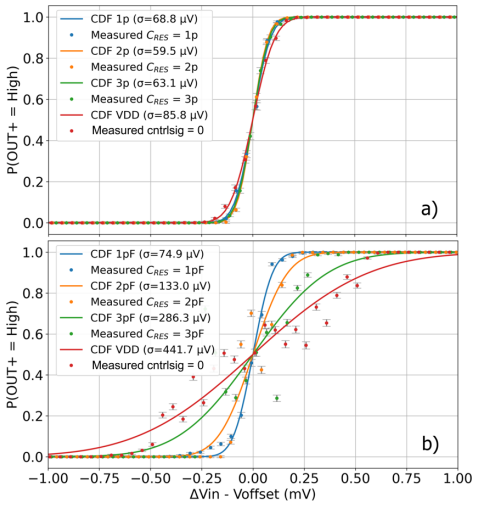

Fig. 3. Measurements of IRN without FBB at (a) RT and (b) 4 K.

differential input excitation. Measurements were performed at T = 300 K and 4 K with V_{DD} = 1.0 V and CLK = 5 MHz. For all measurements IRN was extracted by sweeping ΔV_{in} from -1 mV to 1 mV around $V_{CM} = 350$ mV in 50 μV steps. For each input value, 5000 output comparisons were collected at 40 different time instants and fitting the switching probability with a normal cumulative distribution function (CDF).

A. Without FBB at RT and 4 K

During this test, the NMOS and PMOS bulks were tied to GND and V_{DD}, respectively. Figs. 3(a) and (b) show the measured noise and fitted CDFs of the proposed comparator at RT and 4 K, respectively, for three C_{RES} settings (1, 2, and 3 pF). At RT, all switched-supply configurations achieve lower IRN than the direct supply connection to V_{DD} ($cntrlsig$ = 0), consistent with [6]. At 4 K, however, the measured data exhibit a wider spread, resulting in a poorer CDF fit and higher IRN. This behavior is attributed to the significant V_{TH} increase at cryo temperature, which makes the internal nodes more sensitive to overdrive and timing constraints.

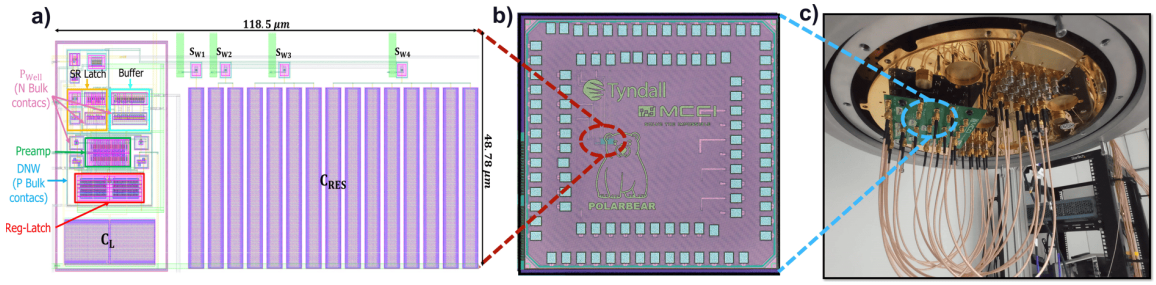

Fig. 4. (a) Comparator layout overview, (b) test-chip micrograph with the comparator location highlighted, and (c) internal cryostat interconnects and PCB.

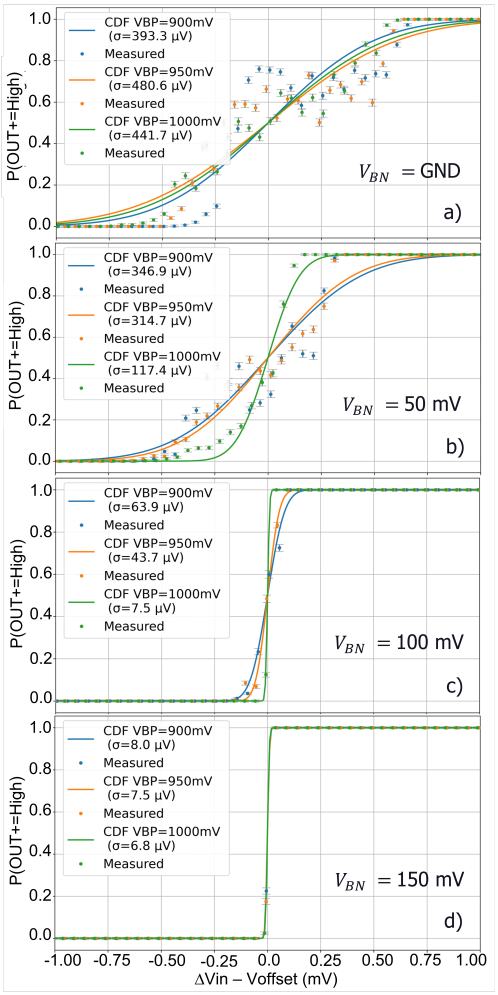

Fig. 5. Measurements of IRN with cntrlsig = 0, sweeping V_{BP} and V_{BN}.

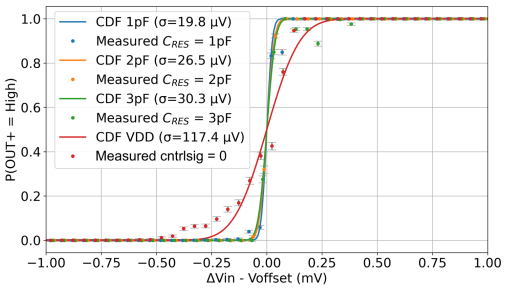

Fig. 6. Measured IRN at 4 K for fixed FBB (V_{BN} = 50 mV,V_{BP} = 1 V) and different C_{RES} settings.

B. With FBB at 4 K

To facilitate the visualization of the FBB biasing effect, the comparator was characterized with $cntrlsig$ = 0. Keeping the comparator in this state, the bulk voltages of the PMOS and NMOS were swept to try to recover the comparator's IRN characteristics. Three DC values for the PMOS bulk biasing were used: V_{BP} = 1 V, 950 mV and 900 mV. Fig. 5(a) shows the measured results for V_{BN} = GND and the three different V_{BP} voltages, where irrespective of the V_{BP} value, the comparator exhibits significantly degraded IRN. Fig. 5(b) illustrates the results with V_{BN} = 50 mV, where for V_{BP} = 1 V the IRN seems to be closer to the RT result (Fig. 3(a) curve for $cntrlsig$ = 0) but for lower values of V_{BP} the IRN degrades. Fig. 5(c) depicts the results for V_{BN} = 100 mV, where the CDFs have significantly straightened and the data points are more consistent and with a smaller number of outliers, meaning that the IRN performance has significantly improved. Nevertheless, the trend is that the IRN degrades with lower values of V_{BP}. Finally, Fig. 5(d) shows the results for V_{BN} = 150 mV, where the CDFs have further straightened and the IRN is dramatically reduced for any value of V_{BP}. The caveat here is that the used measurement equipment is limited to 50 μV of differential voltage resolution and therefore any measured comparator's IRN under this value cannot be a true measurement of the intrinsic noise behaviour. In general, all these results show that NMOS body-biasing is the main parameter for restoring and improving the comparator's IRN performance at 4 K.

C. FBB and Switched Supply at 4 K

To verify the robustness of the FBB technique, the next step is to enable the switched supply feature of the comparator. Since lower C_{RES} values led to lower IRN at RT, see Fig. 3(a), V_{BP} and V_{BN} at 4 K should be chosen in such a way there is enough margin to capture lower IRN when activating the switched supply feature. Therefore, Fig. 6 shows the IRN

TABLE I
STATE-OF-THE-ART COMPARISON OF CRYOGENIC DYNAMIC COMPARATORS

Parameter	This work		[11]		[3]		SA [5]		DT [5]		TT [5]		TTCO [5]	
	RT	4K	RT	6K	RT	4K	RT	6K	RT	6K	RT	6K	RT	6K
Architecture	Programmable switch-supply		TTCO		StrongARM		SA		DT		TT		TTCO	
Area [μm^2]	5543.43		105.6		—		41.0	41.0	63.7	63.7	88.6	88.6	105	105
Technology [nm]	65		40		40		40		40		40		40	
V_{DD} **[V]**	1.0		0.9		—		0.7–0.9	0.7–0.9	0.7–0.9	0.7–0.9	0.7–0.9	0.7–0.9	0.7–0.9	0.7–0.9
V_{CM} **[V]**	0.35		0.3		0.65		0.2–0.5	0.1–0.4	0.2–0.5	0.1–0.4	0.2–0.5	0.1–0.4	0.2–0.5	0.1–0.4
f_{clk} **[MHz]**	5		0.1–50		1000		—		—		—		—	
Noise [μV]	63.9–100.3	19.8–117.4	—	237	—	—	955	314	858	390	685	362	678	274
Energy [fJ]	553–812	421–839	—	158	—	—	36.0	25.6	55.4	38.5	88.7	101	129	123
FoM* **[nJ·μV^2]**	0.2–0.8	0.01–1.1	—	8.9	—	—	3.2	0.2	4.0	0.5	4.1	1.3	5.9	0.9

** FoM definition as reported by each reference. The FoM value for [5] was estimated*

at 4 K with V_{BP} = 1 V and V_{BN} = 50 mV for C_{RES} = 1, 2, and 3 pF and $cntrlsig$ = 0 operation. It can be observed that all switched supply modes clearly outperform $cntrlsig$ = 0, with a similar trend to that at RT in Fig. 3(a). This demonstrates that the comparator performance has not only been recovered for a specific configuration, but also across the other evaluated configurations. Notably, for lower C_{RES}, there is a lower effective supply voltage for the comparator, the fact that it continues to operate under lower supply voltages also proves the robustness of the FBB technique in the comparator. Fig. 7 illustrates the measured energy consumption of the programmable comparator at both RT and 4 K. The comparator achieves lower power consumption, as well as lower IRN (see Fig. 6), for lower values of C_{RES} for both cases. Notably, the energy per conversion at 4 K outperforms the RT measurements, further proving the positive effect of FBB in recovering the comparators operating conditions. Table I shows a comparison of the proposed comparator with the state of the art, highlighting it as one with the lowest reported IRN, which is programmable in the range from 19.8 to 117.4 µV. However, the lower IRN comes at the expense of reduced energy efficiency, which is also programmable from 421 to 839 fJ at 4 K. Since the test setup did not include delay measurements, like these performed in [5], the reported FoM only considers the operation frequency, the power and the IRN.

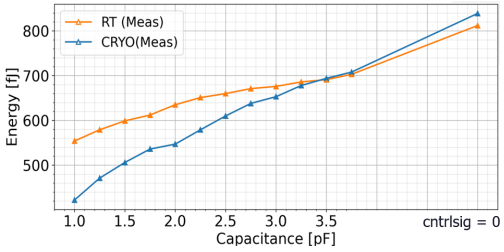

Fig. 7. Measured energy for different values of C_{RES} at 4 K

IV. CONCLUSION

This work reports the measured noise and energy consumption of a programmable dynamic comparator using FBB at both RT and 4 K. Measurements at 4 K show that the comparator mitigates the cryogenic V_{TH} shift through FBB, as confirmed by the improved noise performance obtained by adjusting the bulk voltage, particularly for the NMOS devices. The measurements show substantial IRN tuning at 4 K, from 19.8 μV to 117.4 μV. The proposed comparator achieves a FoM of 0.2–0.8 at RT and 0.01–1.1 at 4 K. Overall, these results support the use of combined supply programmability and FBB as an effective strategy for energy-efficient, low-noise Cryo-CMOS mixed-signal interfaces.

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