

VENUE

AUDITORIUM PALMA DE MALLORCA

Av. Gabriel Roca, 18
07014 Palma - Illes Balears (SPAIN)
www.auditoriumpalma.com/en/

The Auditorium de Palma enjoys a privileged location in the heart of Palma Bay, surrounded by some of the finest hotels in Mallorca.

Situated along Palma's seafront promenade, at the very center of the city and just 10 minutes from Palma de Mallorca Airport, it offers both local and international audiences convenient access to the island's premier performances and events.

CONTACT

ORGANIZING SECRETARIAT

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Advancing Chips, Advancing Europe
ESSERC2026

7-10 September 2026
PALMA DE MALLORCA (Spain)

WWW.ESSERC2026.ORG

WHY PALMA DE MALLORCA?

Palma, the capital of island of Mallorca, is a historic city that has looked to the sea since its Roman origins. Its medieval old town offers a wealth of cultural landmarks within walking distance: the iconic Cathedral (begun in the 13th century), the Royal Palace of the Almudaina, the Arab Baths, the Museum of Contemporary Art, and numerous churches in Gothic, Renaissance, and Baroque styles, many housing valuable artworks. The seafront remains partially enclosed by medieval walls.

Bellver Castle, located on a wooded hill just 3 km from the city center, offers one of the finest views of the Bay of Palma.

The narrow, shaded streets reveal noble palaces with Gothic and Renaissance courtyards, staircases, and grand windows. The city also features lively areas with bars, bakeries, markets, and restaurants offering local and international cuisine. Traditional Mallorcan dishes are best enjoyed in cellars, old wine cellars now serving regional recipes, and century-old bakeries still offer delicious pastries.

Just outside Palma, you'll find some of the Mediterranean's most beautiful beaches and a scenic mountain range dotted with picturesque villages once home to famous artists and writers.

Palma is well connected, especially in summer (May to October), with many daily direct flights from major European cities. The map below shows a selection of routes and flight times.



●● GENERAL PURPOSE OF THE CONFERENCE

The aim of **ESSERC** (European Solid-State Electronics Research Conference) is to provide an annual European forum for the presentation and discussion of recent advances in solid-state devices and circuits. It is a continuation of the former **ESSDERC-ESSCIRC** conference series. The level of integration for system-on-chip design is rapidly increasing. This is enabled by advances in semiconductor technology. Therefore, more than ever before, a deeper interaction among technologists, device experts, IC designers and system designers is necessary. **ESSERC** is governed by a Steering Committee and consists of Plenary Keynote Presentations, invited papers and research papers on technology, circuits and topics bridging both device and circuit communities.

●● CONFERENCE TRACKS

Although not limited, papers are solicited for the following main topics:

Advanced Technology, Process and Materials

Process and material developments for logic, memory, and non-CMOS, including electrical and physico-chemical characterization, process integration and manufacturing: 2D TMDs and related insulators (e.g., hBN), graphene and graphene-related materials, TFTs, gate oxide, gate material, silicide, MOL and BEOL materials, 3D monolithic as well as conventional and novel memory cells including charge-based memories, ReRAM, MRAM, PCRAM, ferroelectrics, crosspoint and selectors, organic memory.

Analog, Power and RF Devices

From material growth to device, components, and systems (process, design, devices fabrication, applications). Device design and electrical/ physical/electro-thermal/reliability characterization of devices based on Si RF CMOS, RF SOI, SiGe HBTs, SiC, InP/InGaAs/ GaAs, AlGaN/InGaN/ GaN, CNT, diamond, and related material systems. Power systems integration issues including thermal management, packaging technologies, system-level electro thermal characterization, product quality and system reliability aspects. Device production processes and design for manufacturability.

Modelling and Simulation of Electron Devices

Modelling and simulation of electronic devices, including, Logic, Analog/RF, Power, Optical, Sensors, MEMS and Memory applications. Methodologies include TCAD (process and device simulation), Design-Technology Co-Optimization (DTCO), physics-based compact modelling,

numerical, statistical, and ML/AI-based methods. Model parameter extraction techniques. Key topics of interest are Emerging Devices including 1D/2D and organic materials, non-classical transport, and new memory concepts, Neuromorphic Computing, Cryogenic Electronics and Quantum Computing, Variability and Reliability modelling including radiation effects, Device-Circuit Co-Design, and 3D-Integration including Thermal modelling. Multi-scale modeling that includes one or more of the following levels: atomistic, mesoscopic, single-device, cell, circuit, block, and system level simulations, multiscale modelling chains and interactions between TCAD and compact modelling as well as multi-scale modelling for 3D/heterogeneous integration, is of particular interest. Model validation with experimental data is highly encouraged.

Analog Circuits

Building blocks, systems, and techniques operating in the analog or mixed-signal domain, such as amplifiers, drivers, comparators, filters, references, analog systems, analog interfaces, and analog techniques.

Data Converters

Nyquist-rate and oversampling A/D and D/A converters. Capacitance-to-digital, time-to-digital, frequency-to digital converters. Embedded and application-specific A/D and D/A converters. Analog to information conversion. A/D and D/A converter building blocks (sample-and-hold circuits, calibration circuits). Enabling new techniques, architectures, or technologies.

RF & mm-Wave Circuits

Building blocks and front-ends operating at RF, mm-Wave and THz frequencies for wireless communication, radar, sensing, and imaging.

Frequency Generation Circuits

Oscillators and controlled oscillators, PLL, DLL, injection locked oscillators, frequency dividers, any kind of frequency generation or time base circuits and systems.

Digital Circuits & Systems

Digital circuits and memory subsystems for microprocessors, micro-controllers, application processors, graphics processors; digital systems for communications, video, multimedia, security, and cryptography applications. Digital design techniques for power reduction, intra-chip communication, clock distribution, soft-error and variation-tolerant design, system-level integration. Devices and circuits for IoT and loE security (e.g., PUFs, TRNGs).

Power Management

Power management and control circuits. Regulators. Switched-mode power converter ICs using inductive,

capacitive, and hybrid techniques. Energy harvesting circuits and systems. Wide-bandgap topologies and gate-drivers. Power and signal isolators; robust power management circuits for automotive and other harsh environments. Circuits for lighting, wireless power and envelope modulators. Design for manufacturability.

Wireless Systems

Wireless systems: radio transceivers, highly integrated front-ends, SoCs and SiPs, incl. heterogeneous packaging solutions, at RF, mmWave or THz frequencies, for established or future standards, as well as novel applications such as radar, sensing, and imaging.

Wireline and Optical Circuits and Systems

2.5/3D interconnect, copper-cable links, and equalizing on-chip links, exploratory I/O circuits for advancing data rates, chip to chip system communications, high speed serial interfaces, optical interfaces, laser drivers, optical receivers, clock and data recovery.

Emerging Computing Devices and Circuits

Novel devices and circuits to improve existing and enable new computing paradigms. In-memory computing and logic-in-memory using emerging devices. Qubit devices and cryogenic circuits for quantum computing. Non-charge-based logic devices and circuits (magnetic logic, spintronics and plasmonics), beyond CMOS transistors (tunnel FETs, Dirac-source FETs). Devices and circuits based on low-dimensional systems (2D materials, nanowires etc.), topological insulators, and phase transitions.

Architectures and Circuits for AI and ML

Silicon implementations of AI, ML, neuromorphic accelerators and processors, together with their applications. Edge and cloud AI computing platforms. In- and near-memory computing at the array/processor-level using commercially available technologies.

Devices & Circuits for Sensors, Imagers and Displays

Devices and circuits based on MEMS and bioelectronics devices for biomedical and imaging applications. Image sensors and related circuits and systems, SoCs. Automotive, LIDAR, and ultrasonic sensors for ADAS, autonomous driving, smart mobility. MEMS sensor systems. Thin Film Transistors. Electrochemical Transistors. Flexible, wearable, printable, organic and ingestible electronics, biomedical SoCs, neural interfaces and closed-loop systems. Biosensors, microarrays, and lab-on-a-chip. Display and large area electronics, displays with sensing functionality. Devices, circuits, and systems for AR/VR and related sensing/actuation. Product quality and reliability aspects. Device and circuits production processes and design for manufacturability.

●● CONFERENCE HIGHLIGHTS

- Tutorials and Workshops
- Keynote Presentations covering circuit and design aspects, semiconductor technologies, and integrated technologies and devices
- Selection of Research Papers in the fields of IC design and semiconductor device development
- **ESSERC 2025** Best Paper Awards
- Networking Opportunities during the Welcome Cocktail and Gala Dinner

●● PAPER SUBMISSION

Papers submitted for review must clearly state:

- The purpose of the work
- How and to what extent it advances the state-of-the art
- Specific results and their impact.

Only work that has not been previously published or submitted elsewhere will be considered. Submission of a paper for review and subsequent acceptance is considered as a commitment that the work will not be publicly available prior to the conference. Measurement results or calibration against measured data is required to support the claims of the submitted paper.

After selection of papers, the authors will be informed about the decision of the Technical Program Committee by e-mail by **May 27, 2026**.

At the same time, the complete program will be published on the conference website. An oral presentation will be given at the Conference for each accepted paper. No-shows will result in the exclusion of the papers from any conference related publication. The submitted final PDF files must be IEEE Xplore compliant.

For each paper independently, at least one (co-)author is required to register for the conference (one registration one paper policy).

Registration fees and deadlines will be available on the conference website.

PAPERS SUBMISSION DEADLINE: APRIL 3, 2026

●● BEST PAPER AWARD

Papers presented at the conference will be considered for the “Best Paper Award” and “Best Young Scientist Paper Award”. The selection will be based on the results of the paper selection process and the judgment of the conference participants. The award delivery will take place during **ESSERC 2027**.