Depletion-layer-modulated analog memory behavior in ferroelectric-GeSn capacitors

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***Abstract*— This work presents a capacitive memory device with a ferroelectric HfO_2–ZrO_2 superlattice (HZO-SL) on a p-type polycrystalline (poly-) GeSn semiconductor layer fabricated within a low thermal budget of 450 °C. Although the high hole concentration of poly-GeSn (4.0×10^{18} cm^{-3}) restricts the maximum depletion-layer width, the remanent polarization of HZO-SL generates sufficient bound charges at the interface to drive meaningful depletion-layer-width modulation. This device concept demonstrates multilevel nonvolatile capacitance states, as well as pulse-programmable synaptic potentiation and depression. These results highlight the viability of the HZO-SL/poly-GeSn capacitor as a low-thermal-budget analog neuromorphic memory element that can be integrated into CMOS back-end-of-line processes, display backplanes, and flexible electronics.**

Keywords*— *depletion layer, ferroelectric, HfO_2–ZrO_2 superlattice, polycrystalline GeSn, low-temperature process

I. Introduction

The rapid growth of data-intensive artificial intelligence (AI) workloads has exposed fundamental limitations of conventional von Neumann architectures, where repeated data transfer between physically separated processing and memory units incurs significant energy and latency penalties. Neuromorphic computing addresses this bottleneck by embedding computation directly within memory, inspired by

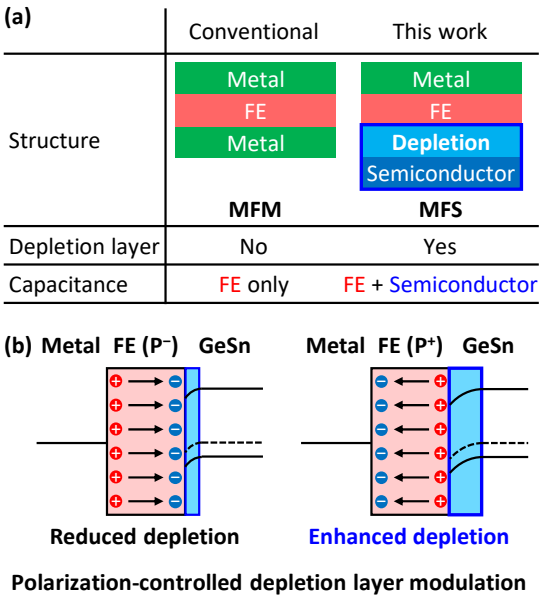

Fig. 1 Concept of ferroelectric depletion-layer modulation. (a) Structural comparison between a conventional MFM and the present MFS capacitors. (b) Schematic band diagrams of the MFS structure illustrating depletion-width modulation induced by ferroelectric (FE) polarization reversal, assuming a p-type semiconductor under depletion conditions. The remanent polarization determines the sign and magnitude of the bound interface charge, which in turn controls the depletion-layer width d and, hence, the depletion-layer capacitance $C_{dep} = \varepsilon_s/d$, thereby enabling analog capacitance tuning through polarization-state control.

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biological synapses. Capacitive memory devices are promising candidates as artificial synapses because, unlike resistive memory, they inherently suppress sneak-path currents while permitting multiple programmable states [1], [2], [3].

Metal–ferroelectric–semiconductor (MFS) capacitors offer distinct advantages over conventional metal–ferroelectric–metal (MFM) devices (Fig. 1(a)) [4], [5]. In the MFS structure, the bottom metal electrode is replaced by a semiconductor, introducing a depletion layer at the ferroelectric/semiconductor interface. The total capacitance C_{tot} is then determined by the series combination of the ferroelectric capacitance C_{FE} and the depletion-layer capacitance C_{dep}, with $C_{dep} = \varepsilon_s/d$. Polarization toward the semiconductor (P^+) widens the depletion region and lowers C_{tot}, while reversed polarization (P^-) narrows it and raises C_{tot}, enabling continuous analog capacitance tuning (Fig. 1(b)).

For the ferroelectric component, HfO_2–ZrO_2 superlattices (HZO-SLs) stabilize the orthorhombic phase, providing high remanent polarization and improved endurance [6], [7], [8], [9], [10]. GeSn alloys have recently emerged as a promising group-IV semiconductor platform, where Sn incorporation induces a direct-bandgap transition, enabling applications from photonics [11] to high-speed electronics [12] within a Si-CMOS-compatible framework. Polycrystalline (poly-) GeSn further offers low-temperature growth (< 400 °C) on insulators, making it compatible with back-end-of-line (BEOL) integration as well as display backplanes and flexible electronics. However, poly-GeSn typically exhibits a high hole concentration, limiting the maximum depletion-layer width [13], [14]. Despite this intrinsic constraint, the present MFS capacitors combining poly-GeSn with HZO-SL generate multiple stable analog capacitance states, demonstrating neuromorphic synaptic functionality.

II. Experiments

MFS capacitors were fabricated on thermally oxidized Si(100) substrates (SiO_2 thickness: 200 nm) using Si-compatible processing. A 200 nm poly-GeSn film incorporating 5.7 at.% Sn was grown by reduced-pressure chemical vapor deposition (RP—D) at 380 °C. Raman spectroscopy confirmed the crystalline nature of the as-deposited GeSn layer. Hall effect measurements revealed p-type conductivity with a hole concentration of 4.0×10^{18} cm^{-3} and a hole mobility of 40 $cm^2\ V^{-1}\ s^{-1}$. Prior to ferroelectric layer deposition, the GeSn surface was treated with a dilute HF/HCl solution to remove native oxides. A 9.6 nm HZO-SL was then deposited by plasma-enhanced atomic layer deposition (PE-ALD) at 300 °C, comprising four bilayer repetitions of HfO_2 (12 cycles, 0.11 nm $cycle^{-1}$) and ZrO_2 (12 cycles, 0.092 nm $cycle^{-1}$). A 50 nm TiN film was subsequently deposited, and rapid thermal annealing at 450 °C for 30 s in N_2 was performed to induce ferroelectric crystallization of the HZO-SL. Al electrodes (200 nm) were formed for both the top contact (on TiN) and the bottom ohmic contact (on GeSn). Device isolation was accomplished by selectively etching the TiN layer using the patterned Al pads as a hard mask.

III. Results and Discussion

A. C–V characteristics and memory operation

Figure 2(a) shows the dual-sweep capacitance–voltage (*C–V*) characteristics of the TiN/HZO-SL/p-GeSn capacitor measured at 50 and 100 kHz. A butterfly-shaped hysteresis loop is clearly observed, confirming ferroelectricity in the HZO-SL layer. Two distinct capacitance levels—a high-capacitance state (HCS) and a low-capacitance state (LCS)—are well separated near 0 V, defining a memory window ΔC that supports non-destructive readout, a favorable feature for energy-efficient operation. A pronounced capacitance peak appears in the negative-to-zero bias region, whereas no corresponding peak is observed under positive bias. This asymmetry reflects the polarization-modulated depletion layer and carrier response at the HZO-SL/GeSn interface, which will be discussed later. The nonvolatile memory operation, including the writing and erasing characteristics, is investigated in Figs. 2(b) and 2(c). Positive pulse voltages V_W for writing and subsequent negative pulse voltages V_E for erasing are applied with amplitudes gradually increasing from 2 to 5 V with 0.5 V steps and a fixed pulse duration of 0.1 s to ensure complete polarization switching. After applying each pulse voltage, the capacitance is read by sweeping from 2 to −2 V. Applying positive write pulses of increasing amplitude

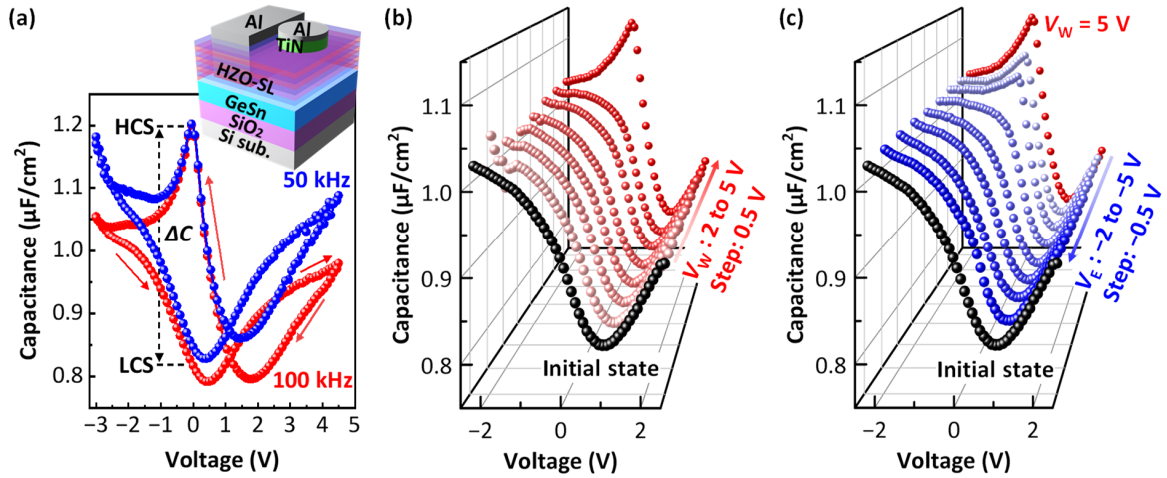

Fig. 2 Electrical characteristics of HZO-SL/GeSn capacitors. (a) Dual-sweep *C–V* curves at 50 and 100 kHz, showing distinct ferroelectric hysteresis with high- and low-capacitance states (HCS and LCS) near 0 V. (b, c) *C–V* curves at 100 kHz after (b) writing at various voltages (V_W) and (c) erasing at various voltages (V_E), where the duration is fixed at 0.1 s.

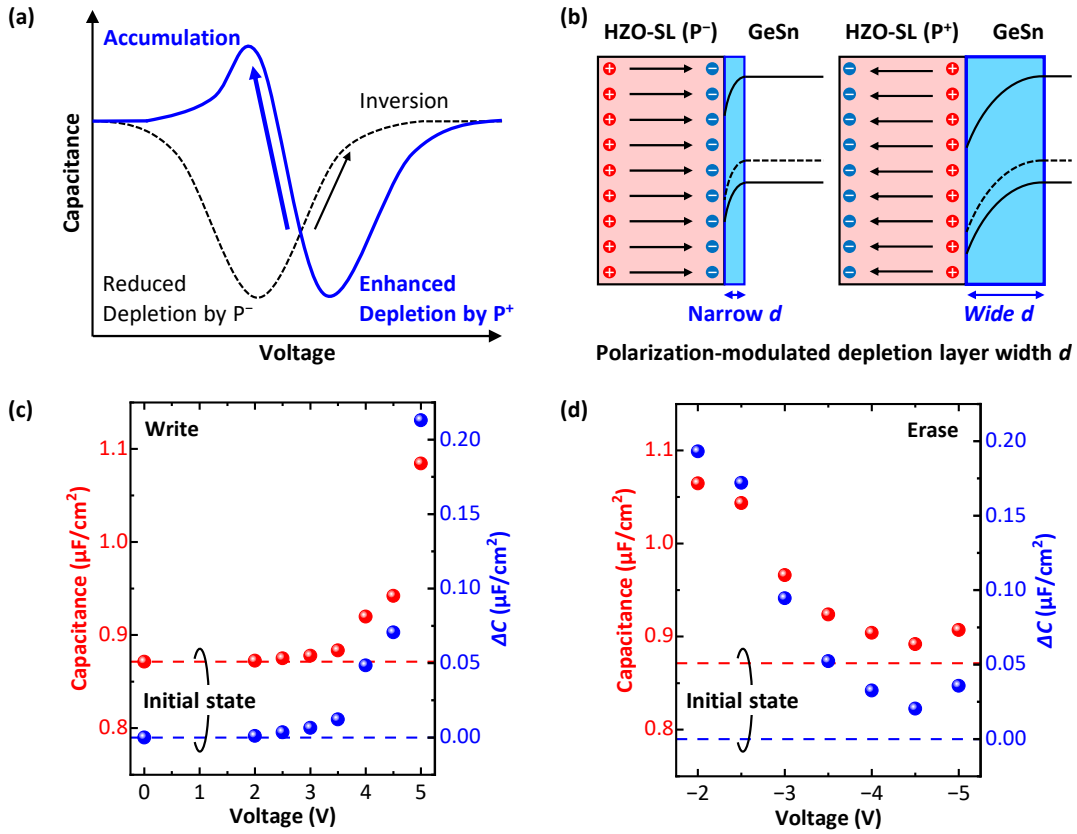

Fig. 3 Physical mechanism of depletion-layer modulation. (a) Band diagrams of the HZO-SL/GeSn interface under different polarization states. (b) Idealized *C*–*V* characteristics illustrating the asymmetry and peak resulting from polarization-modulated depletion. (c, d) Analog capacitance modulation under (c) writing (V_W) and (d) erasing (V_E) sequences, read at -0.1 V.

V_W progressively shifts the *C*–*V* curve toward higher capacitance, producing multiple well-resolved intermediate states. The capacitance increment per pulse is small for V_W below approximately 3.5 V but increases sharply above this threshold, indicative of a nonlinear domain-switching process with a critical depinning field. Conversely, negative erase pulses of increasing amplitude V_E drive the device back toward its initial low-capacitance state in a similarly stepwise fashion. The reversibility and the voltage-addressable nature of these transitions confirm robust multilevel nonvolatile memory operation.

B. Physical mechanism: polarization-modulated depletion

The capacitance modulation shown in Fig. 2 originates from the polarization-induced modulation of the depletion layer in the GeSn layer. Figure 3(a) illustrates the idealized *C*–*V* characteristic, while the corresponding energy band diagrams are shown in Fig. 3(b). In the MFS structure, polarization charges in the ferroelectric HZO-SL modify the electric field at the HZO-SL/GeSn interface and thereby modulate the depletion-layer width *d* in the GeSn layer. When the polarization state P^+ is induced by positive bias, the downward band bending increases, resulting in a wider *d* (right in Fig. 3(b)). This leads to a larger capacitance modulation during the transition from depletion to accumulation. In contrast, the P^- polarization induced by negative bias reduces the band bending and narrows *d* (left in Fig. 3(b)), resulting in a smaller capacitance change. This polarization-dependent depletion modulation explains the large capacitance variation near 0 V observed after positive voltage writing (V_W) in Fig. 2(b). The depletion-layer width increases with increasing V_W and subsequently decreases as the erase voltage $|V_E|$ increases (Fig. 2(c)). This coupling between ferroelectric polarization and depletion-layer modulation enables the observed analog multilevel behavior. Owing to the relatively small bandgap of GeSn, a capacitance increase toward inversion is observed, which helps clearly identify the ferroelectric-polarization-induced depletion modulation.

To further investigate these phenomena, the capacitance at –0.1 V is read after applying pulse voltages with varying V_W and then V_E (Figs. 3(c) and 3(d)). Clear capacitance increases and decreases are observed upon modulating V_W and V_E, respectively. This demonstrates that partial domain switching produces intermediate bound-charge densities and, correspondingly, intermediate values of *d*, i.e., C_{dep} (and hence C_{tot}). Note that the GeSn layer in this work has a high hole concentration of 4.0×10^{18} cm^{-3}, which limits the maximum *d* to only 17 nm. Despite this narrow *d* range, the analog write and erase sequences read at –0.1 V (Figs. 3(c) and 3(d)) demonstrate that the HZO-SL provides sufficient polarization charge to generate clearly distinguishable capacitance levels. These results demonstrate that the highly polarized ferroelectric HZO-SL enables poly-GeSn to serve as a viable semiconductor platform despite its limited depletion-layer response.

C. Neuromorphic synaptic emulation

Building on the multilevel analog memory behavior, synaptic potentiation and depression are explored using the identical pulse sequence with a short pulse width of 0.1 µs directly applicable to practical hardware (Fig. 4(a)). Sequences of fixed positive pulses (V_W = 4.5 V) and negative pulses (V_E = −2.5 V) are applied alternately, with the capacitance read at −0.1 V after each pulse. As shown in Fig. 4(b), repeated stimulation produces a gradual and cumulative increase and decrease in capacitance, closely resembling the potentiation and depression of synaptic weights in biological neural systems. Approximately 25 stable and distinguishable analog states are achieved over the full potentiation–depression cycle. The linearity factor for potentiation α_p and depression α_d are extracted by fitting the experimental data using the equations reported in [15]. The obtained values, α_p = 0.28 and α_d = 0.088, exhibit the same sign and comparable magnitude, resulting in an asymmetry $|\alpha_p - \alpha_d|$ = 0.19, where 0 represents ideal symmetry. These results indicate reasonably linear and symmetric weight updates during both potentiation and depression processes. Such gradual, reversible, and multilevel capacitance modulation is a key requirement for artificial synapses in neuromorphic hardware. The demonstrated behavior confirms that the HZO-SL/poly-GeSn MFS capacitor can effectively emulate synaptic plasticity while maintaining compatibility with a fully low-temperature fabrication process. To further improve the number and resolution of distinguishable states, defect engineering of the poly-GeSn layer will be pursued to reduce the defect-induced hole concentration and the density of interfacial traps and grain boundary traps, thereby enabling greater depletion-layer modulation. Approaches include advanced solid-phase crystallization (e.g., densified amorphous GeSn precursor [16], and appropriate insulating layer insertion at the GeSn/substrate or HZO-SL/GeSn interfaces [17], [18]) and post-thermal/plasma treatments [18], [19].

IV. Conclusion

This work demonstrates an analog memory effect in poly-GeSn-based MFS capacitor structures through ferroelectric-polarization-induced depletion-layer modulation. By leveraging the polarization of the ferroelectric HZO-SL, multilevel analog states are achieved by controlling the depletion-layer width of poly-GeSn, even with its high hole concentration. This analog memory capability enables the emulation of synaptic potentiation and depression with gradual and reversible weight updates. This MFS device concept, based on ferroelectric depletion-layer modulation, paves the way for integrating energy-efficient neuromorphic hardware into BEOL processes, large-area display backplanes, and flexible electronics—all achievable within a low thermal budget of 450 °C.

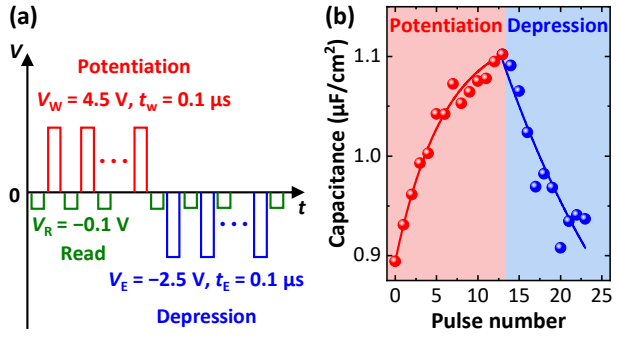

Fig. 4 Neuromorphic synaptic emulation. (a) Pulse scheme employing identical voltage pulses without amplitude or width modulation for synaptic weight updates. (b) Experimental potentiation and depression characteristics with fitted curves, demonstrating multiple stable and clearly distinguishable analog capacitance states.

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