14 dBm-Output-IP3 12-dB-Gain 50.7 MHz-Bandwidth 4th-Order Continuous-Time Analog Low-Pass Filter in 7-nm CMOS FinFET

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***Abstract* — This paper presents a 4th-order continuous-time analog low-pass filter implemented in 7 nm CMOS FinFET technology, specifically addressing the challenges of low-voltage operation and low-frequency noise. The proposed design achieves 12 dB gain, 50.7 MHz -3 dB bandwidth, and 14 dBm output IP3, while reliably operating from a reduced supply voltage of 0.75 V despite a relatively high threshold voltage of 0.4 V. This is made possible through a dedicated biasing circuit that ensures proper device operation and sufficient signal headroom. The filter also mitigates the typical high flicker noise (1/f) issues of FinFETs by optimizing transistor areas, allowing operation closer to the optimal g_m/I region. As a result, the design achieves an input-referred noise of 19.6 nV/√Hz, demonstrating that high linearity and low-noise performance can be obtained in advanced FinFET nodes under stringent dc voltage constraints. The prototype occupies a 0.031 mm² area and consumes 5.5 mA including all bias circuit for robust dc operation.**

Keywords—Continuous-Time Filters, Low-Pass Filters, Operational Transconductance Amplifiers (OTAs), Analog Integrated Circuits, FinFET.

I. Introduction

FinFET technology enables aggressive digital scaling down thanks to improved electrostatic gate control, reduced leakage, and enhanced robustness to Process, Voltage, and Temperature (PVT) variations and mismatch [1], while mitigating short-channel effects. However, leveraging these benefits in analog design remains challenging, and few works have addressed analog design in 7 nm [2].

Circuits operate at 0.75 V supply despite a 0.4 V threshold, while coping with increased 1/f noise. Moreover, the thermal noise factor (γ) increases in strong and moderate inversion, pushing MOS transistors (MOSTs) toward larger-area in weak inversion. The higher oxide capacitance (C'_{OX} = 57 fF/μm² versus 18 fF/μm² in 28 nm planar nodes [3]) increases the gate-source capacitance (C_{gs}) of the OTA input stage, degrading bandwidth and phase margin. While negligible in digital circuits, where device areas are a few tens of nm², this effect becomes critical in analog design, leading to the fact that MOS parasitic capacitances are more detrimental in 7 nm than in 28 nm or earlier planar technologies [4].

In this work, these challenges are addressed through a combination of architectural and circuit-level techniques. A closed-loop level-shifting biasing scheme, originally developed for active g_m-RC circuits [5], is adapted to the multi-path Rauch structure to ensure robust low-voltage dc operation. The noise introduced by the bias circuit is minimized by reducing the contribution of the R_2 resistor in the Rauch cell and connecting it to upstream of the virtual ground, lowering its induced noise power. Input-referred 1/f noise is mitigated through proper transistor sizing and explicit inclusion in the noise budget. Finally, bandwidth and phase margin degradation due to increased C_{gs} is counteracted by exploiting the Rauch cell's inherent two-pole, two-zero loop gain for partial self-compensation. A ~6 dB increase in single-cell gain preserves stability and closed-loop performance despite higher capacitances.

II. 4th-Order Filter Design

The proposed filter consists of the cascade of two biquadratic cells based on a Rauch multipath topology, as in Fig. 1 and in Fig. 2. The cell with the higher quality factor is placed at the input of the cascade to reduce the whole filter in-band integrated noise power. Both cells share the same architecture.

The design targets an input common-mode (CM) voltage of 0.25 V at the p-channel input pair of the OTA, while maintaining an overall input/output CM level equal to $V_{DD}/2$ = 0.375 V. This level shifting is achieved through a dedicated biasing network composed of two identical and symmetrical current sources (MB1-2), one per branch, which sink a constant current to reduce the intermediate node CM voltage, thereby setting the OTA input CM to the desired level. This gives about 0.35 V gate-source voltage for the p-channel OTA input pair operating them in subthreshold.

In addition, a low-power single-ended output auxiliary OTA is employed in a dc feedback loop to compensate for residual CM variations due to PVT fluctuations. This approach ensures a robust operating point, accurately stabilized by the proposed self-biasing scheme.

A. Filter Analog Design in 7 nm CMOS FinFET

The key implications of 7 nm CMOS FinFET technology on low-noise analog design are outlined. While FinFET devices provide superior electrostatic control and enhanced subthreshold transconductance efficiency, the severely limited voltage headroom ($V_{DD} - V_{TH}$=0.35 V) effectively precludes strong inversion operation, enforcing biasing in subthreshold or moderate inversion. This constraint is, to some extent, beneficial from a thermal noise standpoint. The input-referred thermal noise exhibits a minimum for V_{GS}=0.3/0.4 V, whereas at higher gate-source voltages the excess noise factor γ increases quasi-linearly due to enhanced carrier scattering, channel stress, and non-ideal transport effects [1].

Fig. 3 quantitatively illustrates this behaviour. The simulated g_m vs. V_{GS} characteristic of a minimum-sized RF FinFET device is shown in Fig. 3a). The device consists of 4 fingers, each composed of 4 fins (i.e., a 4×4 fin–finger configuration, where N_{fin} is the fin count of a single finger device and N_{finger} is the finger count), resulting in an effective device width (W_{eff}) of:

$$W_{eff} = N_{fin} \cdot N_{finger} \cdot \left(2 \cdot h_{fin} + W_{fin}\right) \cong 1.47\,\mu m \quad (1)$$

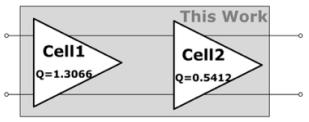

Fig. 1 – Filter Top View Scheme

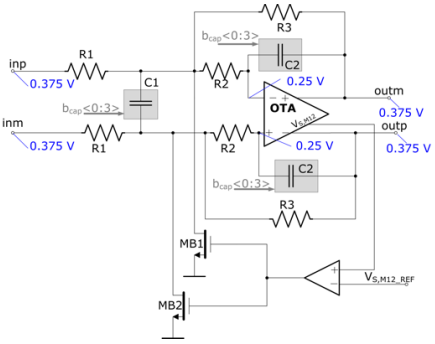

Fig. 2 – Biquadratic Cell Scheme

The corresponding drain current noise spectral density, proportional to $4 \cdot k \cdot T \cdot \gamma \cdot g_m$, is shown in Fig. 3b). The extracted γ factor, reported in Fig. 3c), highlights that in the subthreshold region its value remains approximately constant. Therefore, for a given transconductance, the thermal noise is minimized in this operating regime. Based on this observation, the filter is designed to operate in subthreshold, where a favourable noise–biasing trade-off is achieved.

B. Flicker Noise in OTA Differential Stages

The previously described approach is not practically exploitable for minimum-sized RF devices, as the flicker noise is dominant and masks the thermal noise contribution. As shown in Fig. 4, increasing the device area significantly suppresses the 1/f noise, leading to a critical design trade-off. Accordingly, in deeply scaled FinFET technologies, device sizing represents the primary design lever for low-noise analog circuits. The transistor area must be sufficiently increased to reduce the flicker noise corner frequency (f_{Corner}) below the desired bandwidth, so that the thermal noise floor becomes dominant. In this work, a maximum f_{Corner} of 1 MHz is targeted, which sets a lower bound on the device area as a function of technology parameters and target thermal noise, as expressed in (2):

$$W_{eff} \cdot L \geq 4 \cdot \frac{k'_f}{C'_{OX} \cdot IRN^2_{OP,THERMAL}} \cdot \frac{1}{f_{Corner}} \qquad (2)$$

where W_{eff} and L are the effective width and length of the OTA input stage transistors [5]. Assuming a standard MOST differential stage, the factor 4 accounts for both input pair and active load MOSTs flicker voltage noise. C'_{OX} is the gate-oxide equivalent capacitance and k'_f is the physical flicker constant (considered at this stage an average value and equal for the PMOS and NMOS devices, empirically set at 1.0×10^{-24} V^2F). This corresponds to a minimum device area of 2.85 µm². Therefore, for a channel length of L = 11 nm, this translates to a W_{eff} of approximately 260 µm. Since FinFETs can only be sized in discrete steps, the resulting design uses a 4x multiplicity device, composed of 32 fingers with 20 fins each, based on a W_{eff}/L per fin of approximately 92 nm/11 nm. In this work, L = 11 nm is chosen for all MOSTs to increase the output resistance compared to the 8 nm option, without unnecessarily introducing higher parasitic capacitances due to the adoption of transistors with higher lengths.

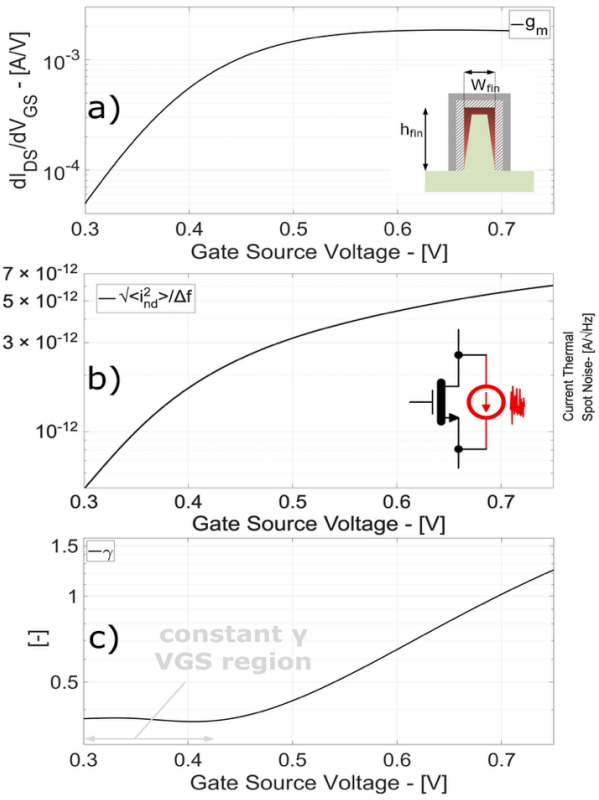

Fig. 3 – g_m, Drain-Source Current Noise and Noise γ factor vs. Gate-Source Voltage for minimum-sized RF FinFET Device (W/L=1.47 µm/8 nm)

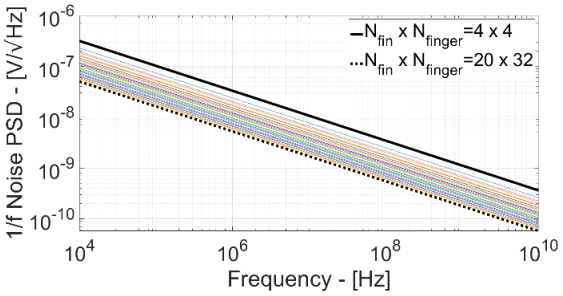

Fig. 4 – 1/f Noise Power Spectral Density vs. N_{fin} x N_{finger}

C. Noise Constraints

Assuming that the flicker noise contribution is sufficiently suppressed (2), the equivalent in-band noise power spectral density of the proposed cell can be expressed as in (3), accounting for the contributions of the resistive elements, the OTA, and the MB1–MB2 current sources. Table I summarizes the main design parameters and specification for 5G/WLAN baseband telecommunication systems [3]-[6], where R_2 is intentionally set four times smaller than R_1 to properly include the noise contribution of the MB1–MB2 current sources for proper voltage level shifting operation.

$$IRN^2_{CELL} = 8 \cdot k \cdot T \cdot R_1 + 8 \cdot k \cdot T \cdot R_2 \cdot (1 + 1/G)^2 + \\ + IRN^2_{OP} \cdot (1 + 1/G)^2 + 2 \cdot i^2_{nMB12} \cdot R_1^2 \qquad (3)$$

III. Experimental Results

The filter was integrated alongside other IP blocks within a 2 mm² area and occupies a footprint of 0.031 mm², as in Fig. 5. Fig. 6 shows the frequency response, which preserves the

TABLE I. DESIGN PARAMETERS

Parameter	Value	
Poles Frequency	50 MHz	
Quality Factor	1.3066 and 0.5412	
Passband Gain	6 dB per Cell	
R1, R2, R3	900, 225, 1800 Ω	
OTA dc gain	42 dB	
OTA ugbw	1.8 GHz	
OTA Thermal Noise (IRN_{OP})	≤ 5 nV/√Hz	
Cell IRN (Input-referred noise evaluated at midband frequency)	≤ 15 nV/√Hz	
Capacitances for Quality Factors	Q=1.3066	Q=0.5412
C1	4.73 pF	2.38 pF
C2	367 fF	1.08 pF

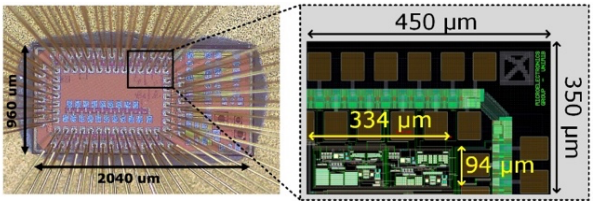

Fig. 5 – Chip Photo

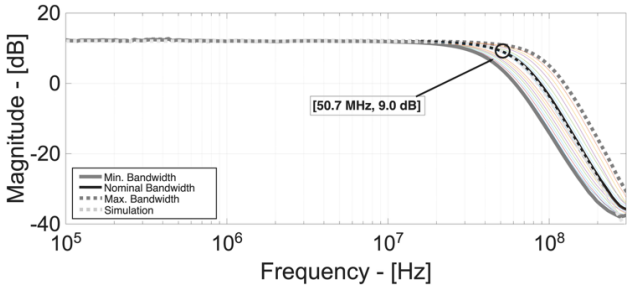

Fig. 6 – Low-Pass Filter Frequency Response

shaping of a 4th-order Butterworth filter, with a slight reduction of both cells quality factor (approximately 20%). The nominal -3 dB frequency is 50.7 MHz, with a minimum and maximum programmable frequency of 34.0 MHz and 74.0 MHz, respectively, achieved through 4-bit tunable capacitors, as illustrated in Fig. 2.

The in-band output noise power spectral density (PSD) is 78.0 nV/√Hz, as shown in Fig. 7, resulting in 19.6 nV/√Hz input noise PSD at the center frequency. The measured f_{Corner} is approximately 4 MHz, higher than the 1 MHz value set in Section II. This behavior can be attributed to the strong dependence of the normalized 1/f noise PSD on the inversion level, expressed through the gm/ID ratio, rather than on device area alone. As a consequence, operation in moderate and weak inversion increases the relative contribution of flicker noise, shifting f_{Corner} toward slightly higher values.

The output signal spectrum for single-tone input at 15 MHz, with third harmonics at 30 MHz and 45 MHz, is shown in Fig. 8 with a total harmonic distortion (THD) of 40 dB. The 1 dB compression point is 4.2 dBm and reported in Fig. 9. A minor output power resolution effect is observed at -40 dB THD, corresponding to approximately -3 dB, which can be attributed to a slight reduced loop gain, causing larger signal excursion at the inputs of the OTA shown in Fig. 2.

Intermodulation tests were conducted using two tone pairs, 15 & 16 MHz and 45 & 46 MHz, specifically to evaluate in-band linearity across different frequencies, a key parameter for feedback-based circuits. The spectra and

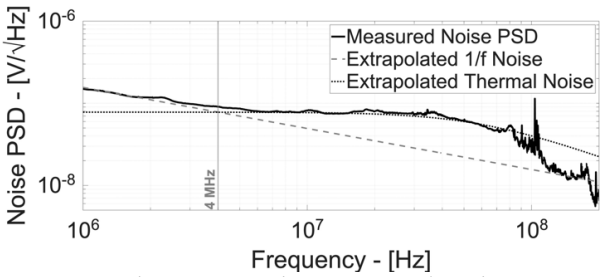

Fig. 7 – Output Noise Power Spectral Density

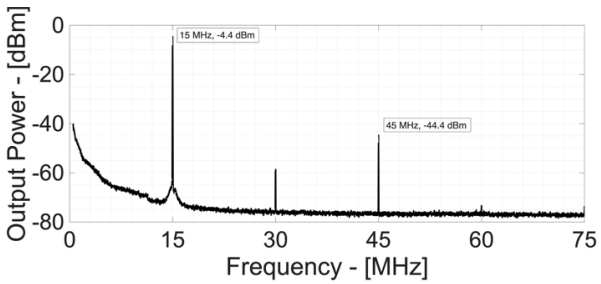

Fig. 8 – Output Spectrum with 15 MHz Input Tone (40 dB THD)

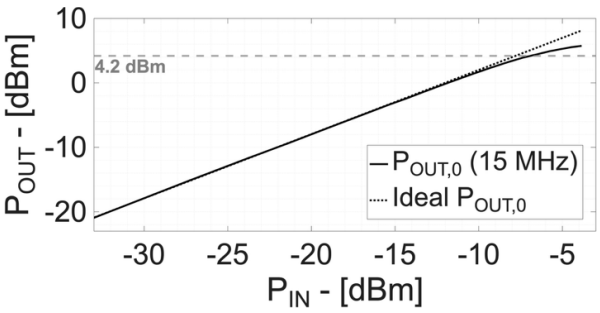

Fig. 9 – Output Power vs. Input Power for a Single Tone Excitation at 15 MHz (1 dB Compression Point Measurement)

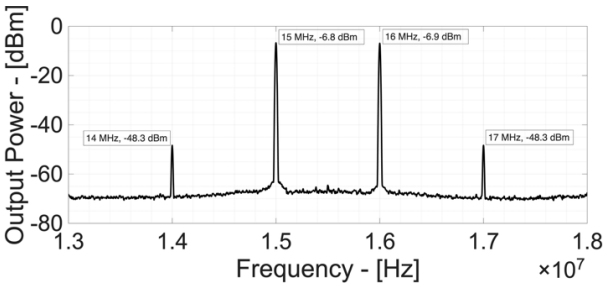

Fig. 10 – Output Spectrum with 15 & 16 MHz Input Tones

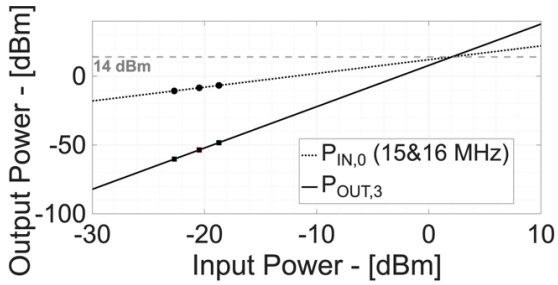

Fig. 11 – Output Power vs. Input Power for Two-tone Excitation at 15 & 16 MHz (OIP3 Measurement)

corresponding OIP3 measurements are plotted in Fig. 10 - Fig. 13.

The OIP3 within the passband, at 12 dB gain, varies from 14 dBm to 10 dBm. Finally, the filter is compared with selected literature works for telecommunication applications (Table II), showing a figure of merit [6] of 154.5–156.5 J^{-1}

TABLE II. PERFORMANCE RESUME AND STATE OF THE ART

Parameter	Units	This Work	[6]	[7]	[8]	[9]	[10]	[11]	[12]	[13]	[14]
Order	-	4th	4th	2nd	6th	3rd	4th	3rd	6th	5th	3rd
CMOS Tech.	nm	7	180	130	90	500	180	180	180	180	180
Supply Voltage	V	0.75	1.8	1.2	1	3.3	1.8	1.8	1.8	1.3	1.8
Power	mW	4.12	1.38	20.	4.3	4.62	4.5	205	8.04	0.65	1.52
dc gain	dB	12	0	-	-2.7	3.2	0	0	0	0	1.33
-3 dB Bandwidth	MHz	50.7	33	200	13.5	1.2	12	300	65	20	6.8
Input Noise PSD	nV/√Hz	19.6	7.8	21.8	75	-	112	3	40	15.3	5.73
In-Band Integrated Noise	μV_{RMS}	138	45	495	270	260	-	-	-	69	8.58
THD	dB	-40 (-4.4 dBm@15 MHz)	-40	-40	-40	-60	-	-	-	-	-
SNR@THD=-40 dB	dB	48 dB@15 MHz	70	54	61.8	-	-	-	-	76	75.5
Output IP3	dBm	14 dBm@15&16 MHz 10 dBm@45&46 MHz	18	14	22.1	2.6	8.7	20.7	12	24.5	22.4
1 dB CP	dBm	4.2 dBm@15 MHz	8	-	7.6	-7	-0.6	-	2	-	

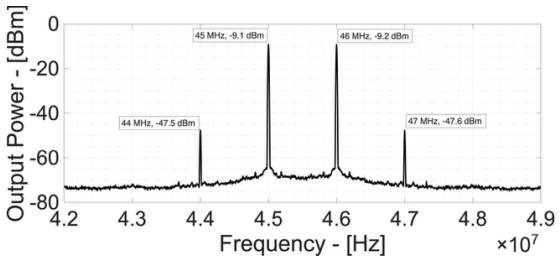

Fig. 12 – Output Spectrum with 45 & 46 MHz Input Tones

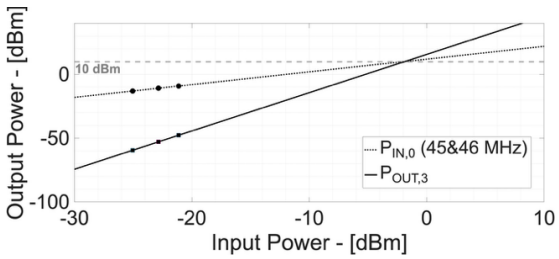

Fig. 13 – Output Power vs. Input Power for Two-tone Excitation at 45 & 46 MHz (OIP3 Measurement)

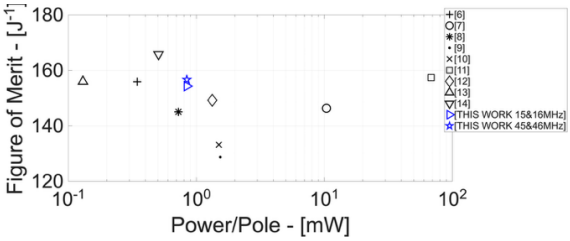

Fig. 14 – Figure of Merit [6] vs. Power per Pole

with 0.84 mW per pole, as in Fig. 14, making it one of the most area- and power-efficient filters reported to date.

IV. CONCLUSIONS

A 4th-order continuous-time analog low-pass filter has been integrated in 7 nm FinFET technology, achieving a nominal -3 dB frequency of 50.7 MHz with programmable tuning from 34.0 MHz to 74.0 MHz. The design maintains thermal noise dominance, with a center-band IRN PSD of 19.6 nV/√Hz and a corner frequency below 10 MHz, while preserving 4th-order shaping. Single-tone and intermodulation tests demonstrate a 1 dB compression point of 4.2 dBm and in-band OIP3 from 10 dBm to 14 dBm, confirming good linearity. With a figure of merit of 154.5–156.5 J^{-1} at 0.84 mW per pole, the filter achieves excellent scaling and suitability for high-performance telecommunication applications.

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REFERENCES

[1] K. Karimi *et al.*, "Comprehensive Review of FinFET Technology: History, Structure, Challenges, Innovations, and Emerging Sensing Applications," *Micromachines*, vol. 15, no. 10, Art. 1187, Sep. 2024.

[2] A. L. S. Loke *et al.*, "Analog/Mixed-Signal Design Challenges in 7-nm CMOS and Beyond," *Proc. IEEE CICC*, 2019, pp. 1–8.

[3] M. De Matteis *et al.*, "A 28.8-MHz 23-dBm-IIP3 3.2-mW Sallen-Key fourth-order filter with out-of-band zeros cancellation," *IEEE Trans. Circuits Syst. II, Exp. Briefs,* vol. 63, no. 12, 2016.

[4] F. Fary *et al.*, "A 28nm-CMOS 100MHz 1mW 12dBm-IIP3 4th-Order Flipped-Source-Follower Analog Filter," in *Proc. IEEE 44th Eur. Solid-State Circuits Conf. (ESSCIRC)*, 2018.

[5] M. De Matteis *et al.*, "A 0.55 V 60 dB-DR Fourth-Order Analog Baseband Filter," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, pp. 2973–2984, Nov. 2009.

[6] M. De Matteis *et al.*, "A 33 MHz 70 dB-SNR super-source-follower-based low-pass analog filter," *IEEE J. Solid-State Circuits*, vol. 50, pp. 1516–1524, 2015.

[7] M. Mobarak *et al.*, "Attenuation-predistortion linearization of CMOS OTA with digital correction of process variations in OTA-C filter applications," *IEEE J. Solid-State Circuits*, vol. 45, pp. 351–367, 2010.

[8] S. Oskooei *et al.*, "A CMOS 4.35-mW +22-dBm IIP3 continuously tunable channel-select filter for WLAN/WiMAX receivers," *IEEE J. Solid-State Circuits*, vol. 46, pp. 1382–1391, 2011.

[9] G. C. Alberdi *et al.*, "Tunable class-AB CMOS Gm-C filter based on quasi-floating-gate techniques," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 60, pp. 1300–1309, 2013.

[10] S. Hori *et al.*, "Low-power widely tunable Gm-C filter employing an adaptive DC-blocking triode-biased MOSFET transconductor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, pp. 37–47, 2014.

[11] K. Kwon *et al.*, "A 50- to 300-MHz CMOS Gm-C tracking filter based on parallel operation of saturation and triode transconductors for digital TV tuner ICs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 62, pp. 522–526, 2015.

[12] J. S. Mincey *et al.*, "Low-power gm-C filter employing current-reuse differential difference amplifiers," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 64, pp. 635–639, 2017.

[13] Y. Xu *et al.*, "A 77-dB-DR 0.65-mW 20-MHz 5th-order coupled source followers based low-pass filter," *IEEE J. Solid-State Circuits*, vol. 50, pp. 2810–2818, 2020.

[14] F. Rezaei *et al.*, "A 94.7-dB dynamic range fully passive switched-capacitor low-pass filter with enhanced selectivity and passive gain," in *Proc. ESSERC*, 2024, pp. 277–280.