An 18-22 GHz Direct 983 MHz Crystal Sinewave Sampling Fractional-N PLL

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***Abstract*—This work presents a Fractional-N PLL that directly samples the co-integrated crystal oscillator (XO) waveform. A capacitive DAC (CDAC) based phase detector directly samples the XO waveform. Before tracking starts, the CDAC is preconditioned to minimize charge sharing, and compensation is applied after sampling to cancel divider quantization error phase offset. The measured PLL in 22 nm FDSOI technology has 148 fs jitter and fractional spurs lower than −65 dBc at 18-22 GHz, resulting in a FoM of −244 dB including the XO power.**

***Keywords*—Phase-locked loop (PLL), Fractional-N, Direct reference sampling phase-locked loop (DRSPLL), Direct reference sampling phase detector (DRS-PD), Crystal oscillator (XO), Low-spurious**

I. Introduction

High-frequency, low jitter fractional-N PLLs are important to accommodate higher data-rates for future wireless communication standards such as 6G. To achieve this, reference sampling phase-locked loops (RSPLLs) have gained interest [1], [2], [3], [4] for their wide phase-detection range compared to a sub-sampling PLL (SSPLL) or bang-bang PLL (BBPLL). Furthermore, no power-hungry reference buffer is required to convert the crystal oscillator (XO) signal to a square wave while the sinusoidal phase detector curve is well-defined, beneficial for low-spurious fractional-N performance.

Prior-art RSPLLs often use external crystal references with embedded 50 Ω buffer, which may have a high (>100 mW) power consumption [5]. Integrating the XO electronics on-chip allows us to get rid of power-hungry buffers and save power on the system-level. As the XO-signal provides a high-quality reference, we like to stay as close to that as possible. Consequently, we propose a RSPLL with integrated XO that directly samples the crystal waveform. We leverage the well-defined sinusoidal waveform to achieve good fractional spur performance and jitter, while addressing challenges that come with direct sampling like charge injection and XO pulling.

II. Proposed Direct Reference Sampling PLL

In this work we propose the fractional-N PLL shown in fig. 1. It is based on a direct reference sampling phase detector (DRS-PD) that directly samples a 983 MHz crystal sinewave, while applying preconditioning and compensation for the accumulated divider quantization error phase offset using a capacitive DAC (CDAC). The PLL has simple Type-I analog control and a digital integral path to track the reference zero-crossing. A multi-modulus divider (MMD) is controlled by a digital delta-sigma modulator (DDSM) to provide fractional control, while its quantization error is cancelled in the phase detector (PD).

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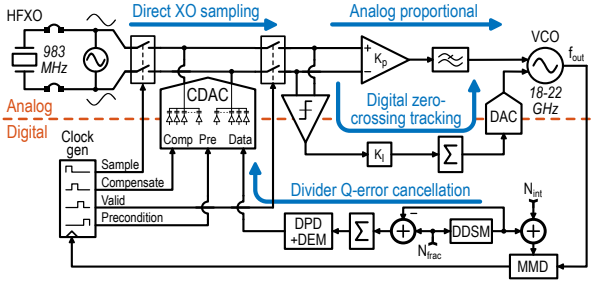


Fig. 1. Proposed PLL architecture

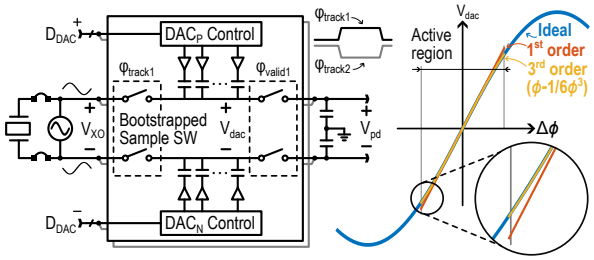


Fig. 2. Proposed Direct Reference Sampling Phase Detector

A. Direct Reference Sampling Phase Detector with CDAC

The concept of the DRS-PD is shown in fig. 2. It incorporates bootstrapped S/H switches to sample the XO waveform and a CDAC. By removing reference buffers and sampling the crystal waveform directly, we minimize the amount of added noise and distortion. A major benefit is that the phase detector follows a well-defined sinusoidal shape, seen at the right of fig. 2. The sampled voltage around the zero-crossing is

$$V_{\mathrm{dac}} = A_{\mathrm{ref}} \sin(\Delta\phi) \approx A_{\mathrm{ref}} \left(\Delta\phi - 1/6 \cdot \Delta\phi^3\right),$$

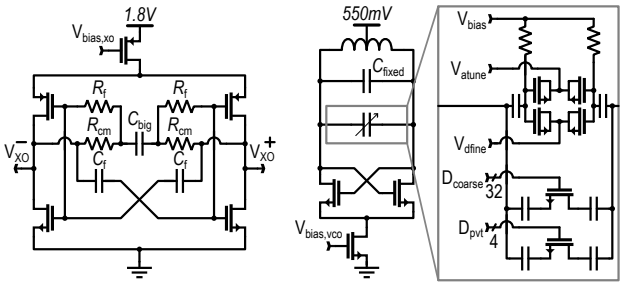
which can be accurately described with a linear and a third-order term. This allows us to cancel the fractional divider quantization error phase offset using the CDAC, employing only predefined third-order predistortion and no adaptive digital pre-distortion (DPD) [6] or LUTs [7], [8], [9]. The DRS-PD is complemented with an ENOP [10] divider DDSM to prevent residual second- and third-order nonlinearity from generating fractional spurs.

As we are directly sampling the XO, spurious tones may arise from variations in capacitive load, charge injection, and charge sharing effects similar to those observed in sub-sampling phase detectors directly loading the VCO [11]. To minimize the variation in capacitive load on the XO, two time-interleaved phase detectors take turns in tracking the reference. Additionally, to minimize charge sharing, the CDAC sampling capacitor is preconditioned to match the expected reference voltage at the moment the tracking switch is closed.

III. Implementation

A. High-Frequency Crystal Oscillator

The co-integrated XO (shown in fig. 3a) is a differential push-pull architecture similar to the core architecture presented in [12]. To ensure linear mode operation over PVT variations, both the number of parallel gm-stages and the bias current can be configured through an SPI. Operation in the linear regime with a minimum amount of harmonic distortion but with sufficient amplitude is essential for the DPD and CDAC optimal performance. The crystal at hand is a research prototype AT-cut quartz crystal with a nominal frequency of 983.04 MHz [13]. The very high reference clock frequency is well suited to the reference-sampling topology, as it delivers high phase-detection gain even with a sinusoidal waveform.



(a) XO (b) VCO

Fig. 3. Schematics of the XO and VCO.

B. Sampling Phase Detector with CDAC

The sampling phase detector (fig. 4) is combined with DAC functionality as in [3], [4], where the sampling is done on the top-plates of a CDAC. In this case two time-interleaved CDACs are taking turns in tracking the reference ($\phi_{\mathrm{track1,2}}$). A major difference from prior art is the pre-conditioning that the time interleaving enables. By applying the predistorted accumulated divider quantization error phase offset to the CDAC ($\mathrm{dac_{in}}$), while the output nodes are held at V_{CM} (ϕ_{rst}), it is possible to start tracking the reference with all capacitors charged to a voltage very close to the present reference clock voltage. The pre-conditioning is a prerequisite for direct sampling of the XO, especially operating in fractional-N mode as sample dependent excess charge pulled in or out of the XO core will impact the phase and cause unwanted memory effects.

Reference tracking occurs during a full MMD output period, until the other pre-conditioned CDAC takes over. Assuming fast switching, the capacitive load on the XO core of the sampling

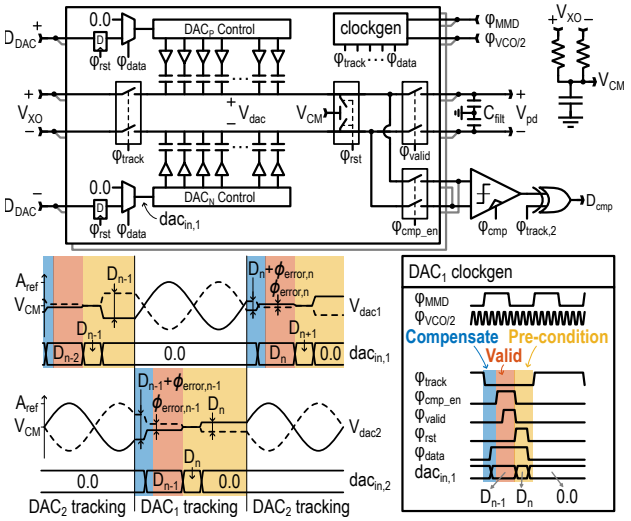


Fig. 4. Sampling PD with CDAC, including simplified timing and voltage waveforms

circuitry is constant. After tracking completes, the divider quantization error phase offset is canceled (ϕ_{data}, see bottom fig. 4) [3], [4]. Before the detected phase error is connected to the loop filter (ϕ_{valid}), a comparator detects the sign of the error (ϕ_{cmp}) enabling correlation between the DDSM phase error and the detected phase error to adjust the gain of the DDSM phase error cancellation. In addition, the comparator provides input to the digital integral loop taking care of the sampling point tracking.

C. Digital Controller

An overview of the digital controller is shown in fig. 5. The digital zero-crossing tracking loop (top) accumulates the output of the comparator multiplied by the integral gain K_{I}. This accumulated phase error is then fed into a MASH-1-1 DDSM, which drives a 6-element thermometer coded R-DAC controlling the VCO. During initial settling, the value of K_{I} is increased to improve settling time. After settling, the loop is disabled ($K_{\mathrm{I}} = 0$).

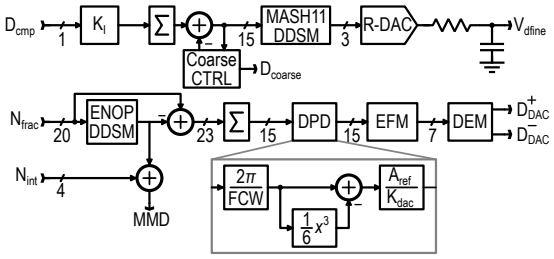
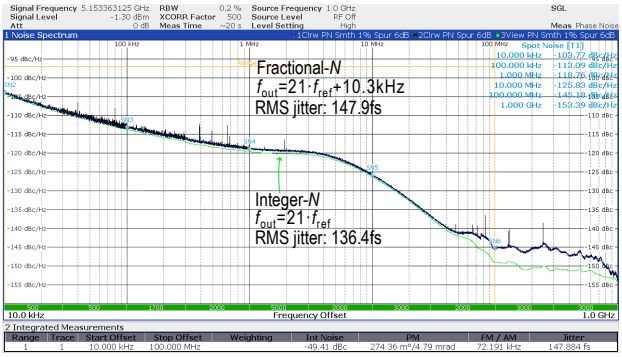
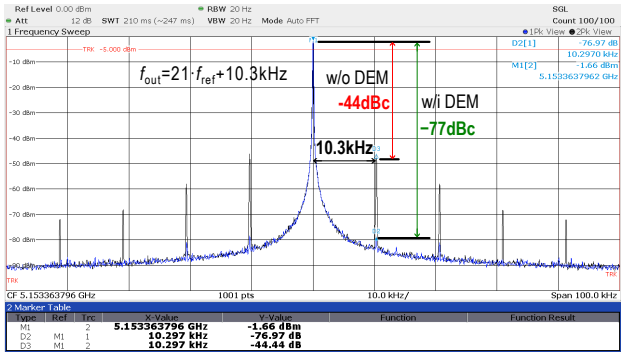


Fig. 5. Digital block overview

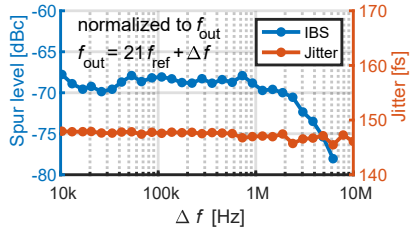
An ENOP-P1 DDSM [10] is used for modulating the MMD as it has spur immunity for third-order nonlinearity. The divider quantization error is accumulated and truncated to 15-bits before DPD is applied. The DPD gains are only dependent on the FCW and the ratio $A_{\mathrm{ref}}/K_{\mathrm{dac}}$, and no adaptive DPD is used, as shown in the bottom of fig. 5. $A_{\mathrm{ref}}/K_{\mathrm{dac}}$ depends on



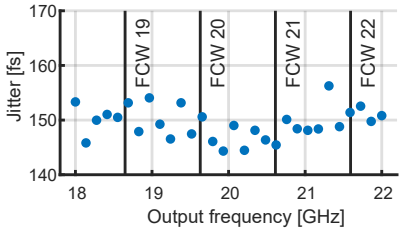
(a) Phase noise



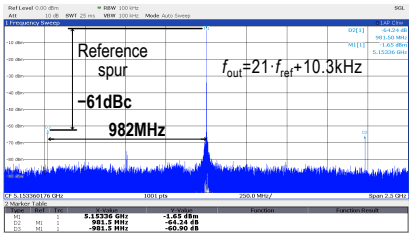
(b) Fractional spurs with and without DEM



(c) Fractional spur (IBS) and jitter



(d) RMS Jitter



(e) Reference spurs

Fig. 6. Measured phase noise, fractional spurs, reference spurs and jitter at the divide-by-4 output

circuit parameters and can be tuned with an LMS algorithm, but in our case it is calibrated only once for all measurements. The 15-bit DPD output is converted to 7-bit using an error-feedback modulator (EFM) to reduce generation of quantization spurs.

Dynamic element matching (DEM) is implemented to prevent mismatch-induced spurs from generating in the CDACs in the PD. The CDAC is segmented into 8 thermometer MSBs and 3-bit binary LSBs [14]. In order to achieve an effective resolution of 7-bit, the LSB is added to the positive 6-bit CDAC and the EFM carry-out bit is added to the negative CDAC.

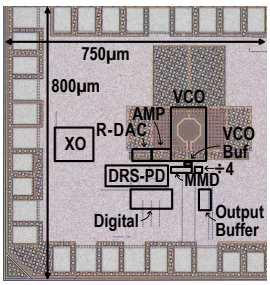
D. Loop Amplifier, VCO and Divider

Since most of the fractional divider quantization error is canceled by the CDAC PD, linearity requirements of the loop amplifier are relaxed. The loop amplifier is implemented as a differential difference amplifier with feedback to ensure high input impedance and independent common-mode voltages at the input and output. The gain is set using a resistor ratio in the feedback path.

The LC-VCO (fig. 3b) is based on NMOS switches and a tail current source providing the bias current. The 550 mV supply voltage is supplied via the center tap of the inductor. There are four tuning ports: A 4-bit binary switched capacitor bank for calibration of PVT effects (D_{pvt}), a 32-element thermometer coded switched capacitor bank for coarse tuning (D_{coarse}), and two varactor pairs to provide an analog tuning port for the digital loop (V_{dfine}) and the analog loop (V_{atune}). The digital varactor tuning range spans approximately 2 coarse tuning steps. The total tuning range is 18-22 GHz. A C^2MOS logic based MMD with integer division ratios between 16 and 31 is connected to this VCO via a self-biased inverter based buffer.

IV. Measurement

The PLL is implemented in a 22 nm FDSOI technology. The chip micrograph, area and power consumption are shown in fig. 7. Figure 6a shows the phase noise at 20.613 GHz (10 kHz offset to an integer-N setting). The integrated RMS jitter is 148 fs, resulting in a FoM_J of −243.9 dB. The jitter in Integer-N mode is 136 fs, indicating only a small jitter penalty in fractional mode.



(a) Chip micrograph

Block	Power [mW]	Area [mm²]
VCO	6.0	0.012
XO	2.3	0.016
DRS-PD & CDAC	1.9	0.009
Amp & R-DAC	0.25	0.003
Digital	2.5	0.006
VCO buf & MMD	5.9	0.001
Total	**18.8**	**0.05**

(b) Power consumption and active area

Fig. 7. Chip micrograph and measured power consumption.

Figure 6b shows the close-in spectrum with and without DEM enabled. With DEM enabled, the integer boundary spur (IBS) is at −65 dBc when normalized to f_{out} (+12 dB compensating divide-by-4). Without DEM the IBS is at −32 dBc, showing the effect of mismatch induced nonlinearity. The IBS and jitter for different offsets close to $N = 21$ are shown in fig. 6c.

The RMS jitter is measured throughout the 18-22 GHz output frequency range, shown in fig. 6d. The average jitter is 149 fs,

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH >20 GHz FRACTIONAL-N PLLS

	This Work	Tao [4] JSSC'25	Ek [12] JSSC'18	Siriburanon [7] OJSSC'24	Meng [8] TMTT'25	Grimaldi [15] ESSERC'24	Wu [6] RFIC'25
Architecture	DRS-PLL	CSS-DPLL	CP-PLL	ROS-PLL	BB-DPLL	DTC-DPLL	DTC-APLL
Technology	22 nm FDSOI	22 nm CMOS	28 nm FDSOI	28 nm CMOS	28 nm CMOS	28 nm CMOS	8 nm FinFET
Includes XO?	**Yes**	No	**Yes**	No	No	No	**Yes**
f_{out} [GHz]	$18-22$	$21-25$	$23.3-30.2$	$24-31$	$16.4-19.3$	$47.9-57.6$	$16-22$
f_{ref} [MHz]	983	250	491.5	50	100	100	153.6
RMS jitter [fs]	148	168	114	350	154	137	68
Integ. range [Hz]	10k – 100M	10k – 40M	20k – 500M	10k – 30M	1k – 100M	10k – 25M	10k – 10M
Ref spur [dBc][a]	-49	-61.6	-67.4	-68.2	-69.2	-58	-63
Frac spur [dBc][a]	-65	-49.4	-32.3	-32.2	-54.1	-58.5	-57
Power [mW]	18.8[b] (16.5)[c]	13.8	34.6[b] (31)[c]	11.9	14.8	30	38[b]
Active area [mm^2]	0.05	0.08	0.14	0.3	0.11	0.5	0.38
FoM_J [dB]	-243.9[b]	-244.1	-243.5[b]	-238.4	-244.6	-242.5	-247.3[b]

[a] Normalized to 20 GHz [b] Including XO power [c] Excluding XO power

while the maximum is 156 fs. The reference spur is −49 dBc, as shown in fig. 6e.

Simulations indicate that an unwanted interaction between the MMD and the /4 output divider generates a reference spur and noise bump around 100 MHz (see fig. 6a) at the measurement output. Redesign of the output path to increase isolation likely reduces this effect. A comparison with other works is shown in table I, showing excellent fractional spur performance with small active area.

V. CONCLUSION

We present a fractional-N PLL that directly samples the co-integrated crystal oscillator waveform. In order to minimize the generation of fractional spurs, we apply preconditioning and compensation in the phase detector using a CDAC and use DPD and DEM to minimize the generation of fractional spurs.

The PLL achieves fractional spurs below −65 dBc and consumes low power compared to other fractional-N PLLs at mm-wave frequencies, especially considering the included reference clock generation. It combines minimal analog and digital complexity with a small silicon footprint and is to the best of our knowledge the first PLL that requires no reference clock buffers.

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