A 37.3-fJ/b/dB 32-Gb/s Baud-Rate Receiver With JTOL-Enhanced CDR Using Phase Tracking Assistance and Embedded Real-Time QEC

Ho-Joon Shin[1*], Suil Kang[2*], Jeonghyeon Lee[1], Yoojin Jung[1], Sinho Lee[1], Haram Ju[3], Kwangho Lee[3], and Kwanseo Park[1]
[1]Yonsei University, Seoul, Korea, [2]SK Hynix, Icheon, Korea, [3]KETI, Seongnam, Korea, [*]Equally Credited Author (ECA)
Email: hjnshin@yonsei.ac.kr, kwanseo@yonsei.ac.kr

***Abstract*— This paper presents a baud-rate jitter tolerance (JTOL)-enhanced clock and data recovery (CDR) employing phase tracking assistance and embedded real-time quadrature error correction (QEC). An analog-assist circuit improves JTOL with minimal power overhead, while a shared-logic approach enables QEC without additional circuitry. Fabricated in a 40-nm CMOS process, the prototype improves JTOL at 100 MHz from 0.22 UI to 0.30 UI and corrects quadrature error from 23.4° to within 2°. Operating at 32 Gb/s under 22-dB channel loss, it achieves an energy efficiency of 0.82 pJ/b, yielding a 37.3 fJ/b/dB FoM.**

Keywords*— Analog proportional path, baud rate, clock and data recovery (CDR), jitter tolerance (JTOL), phase interpolator (PI), quadrature error correction (QEC).

I. Introduction

With the rapid growth of AI-driven data centers, the bandwidth demand of high-speed data links continues to increase. As the data rate increases, the shrinking unit interval significantly reduces the timing budget of wireline receivers, making them more vulnerable to jitter components arising from inter-symbol interference (ISI), path mismatch, and circuit noise [1]. As a result, achieving a wide loop bandwidth for rapid timing-variation tracking has become increasingly important in high-speed clock and data recovery (CDR) circuits.

Phase interpolator (PI)-based CDRs have been widely adopted in high-speed receivers due to their digital-friendly implementation and ease of multi-phase clock generation. However, as shown in Fig. 1(a), the use of demultiplexed data in the digital loop filter (DLF) inevitably incurs a large loop latency, which limits the loop bandwidth and degrades high-frequency jitter tracking. One approach to mitigate this limitation is to incorporate an analog proportional path. In oscillator-based CDRs [2], [3], this can be easily implemented using a varactor, as illustrated in Fig. 2(a). In PI-based CDRs, however, the same approach is not straightforward because phase control is not accumulated; instead, the output clock is generated by interpolating among the phases of a forwarded clock, as shown in Fig. 2(b). As a result, extending the loop bandwidth in the conventional PI-based CDRs remains fundamentally challenging.

To overcome this limitation, prior work [4] proposed a dual-loop architecture, as shown in Fig. 1(b), that combines a phase-locked loop (PLL) with a PI and implements an analog proportional path in the PLL. Although this approach extends the loop bandwidth, it incurs additional area and power overhead due to the extra PLL. In addition to loop bandwidth limitations, quadrature error in multi-phase receivers degrades sampling margin and signal integrity [5]. Prior works either do not correct quadrature error [6], [7] or rely on dedicated calibration logic [8], [9], which further increases implementation complexity and hardware overhead.

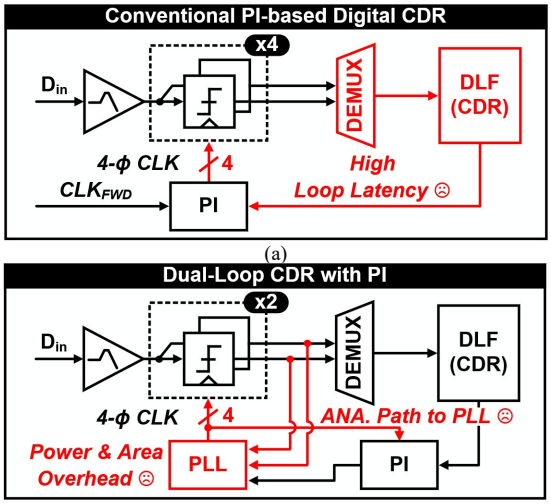


Fig. 1. Comparison of PI-based CDR architectures.

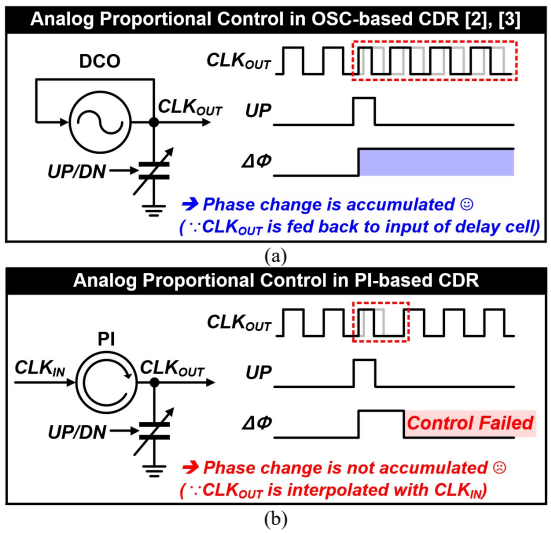


Fig. 2. Analog proportional path implementation in (a) oscillator-based and (b) PI-based CDR.

In this work, these limitations are addressed by (1) incorporating an analog proportional path directly into the PI to extend the loop bandwidth and enhance jitter tolerance (JTOL); and (2) reusing existing CDR logic to implement quadrature error correction (QEC) with minimal power and area overhead.

II. Proposed JTOL-Enhanced Baud-Rate CDR

A. Operation of Phase Tracking Assist Circuit

Fig. 3 shows the block diagram of the proposed phase-tracking assist circuit (PTAC). To implement an analog proportional path in the PI with minimal power overhead, the

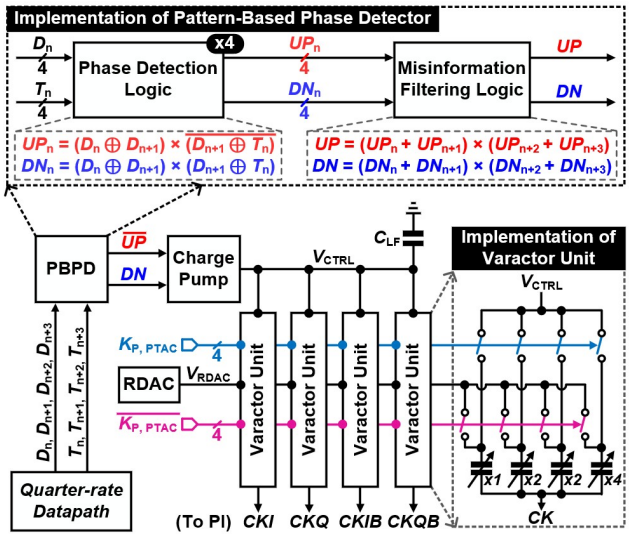


Fig. 3. Block diagram of PTAC and schematics of PD and varactor unit.

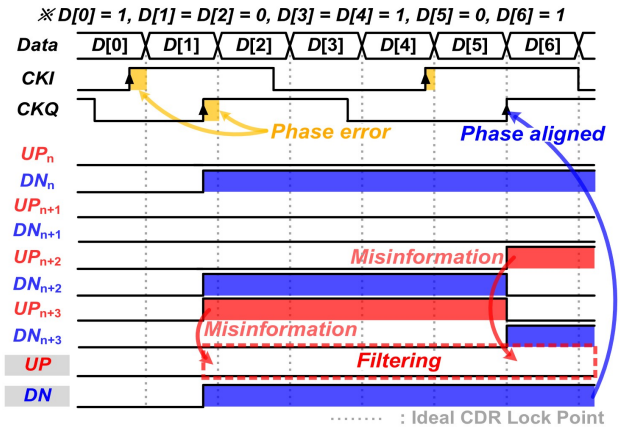


Fig. 4. Ideal timing diagram of MFL and PTAC operation.

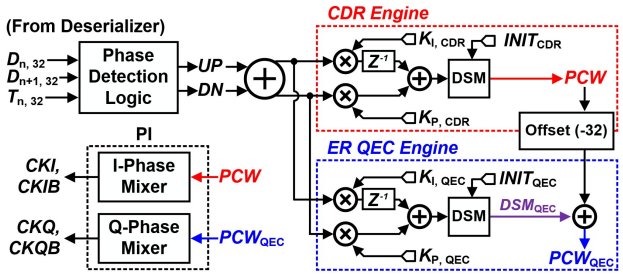


Fig. 5. Block diagram of CDR engine and ER QEC engine.

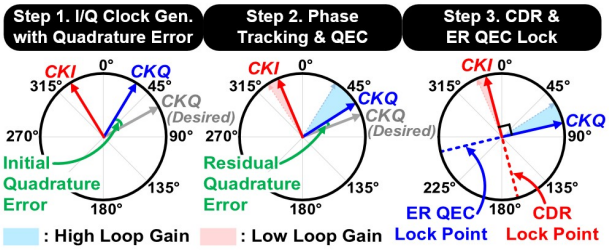


Fig. 6. Operation diagram of proposed ER QEC.

integrator-based summer from [6] is adopted, and its quarter-rate datapath outputs are reused. D_n denotes the data sample, and T_n denotes the integrated error sample that encodes phase error when combined with D_n according to the phase detection (PD) logic in [6]. These two signals are fed into the pattern-based phase detector (PBPD), which is implemented in the analog domain using combinational logic to determine the phase state (late/early) and generate UP_n/DN_n signals.

However, due to the stochastic characteristics of the PD logic, spurious UP_n/DN_n decisions can occur, as illustrated in Fig. 4. For example, when the clock is in an early state, only *DN* should be generated; however, erroneous *UP* can appear. Unlike digital control, the charge pump responds directly to every pulse. Thus, spurious signals immediately perturb the analog control voltage, leading to unwanted jitter and signal integrity degradation. To suppress this, the proposed misinformation filtering logic (MFL) first ORs the UP_n/DN_n signals from adjacent datapaths and then ANDs the resulting signals. As a result, the final *UP*/*DN* outputs reflect the common trend across all four datapaths rather than isolated erroneous pulses.

To realize analog proportional control from these *UP*/*DN* signals, they must be accumulated rather than applied instantaneously. Accordingly, a charge pump accumulates the *UP*/*DN* into a control voltage (V_{CTRL}), which is then applied to varactor units. Each varactor unit is connected to one of the four PI output clocks. According to the varactor's C–V characteristic, V_{CTRL} modulates the effective capacitance at the PI output node, which adjusts the RC delay and fine-tunes the output phase. Since the PTAC operates on quarter-rate 8-Gb/s signals, the phase update rate is higher than that of the demultiplexed digital path, enabling rapid phase tracking and improved jitter tracking. The PTAC proportional gain ($K_{P,PTAC}$) controls the number of active varactors to adjust the phase tuning step. Meanwhile, inactive varactors are terminated by a resistor-based digital-to-analog converter (RDAC) output at a fixed bias voltage (V_{RDAC}) to prevent unintended control.

B. Operation of Real-Time Quadrature Error Correction

Fig. 5 shows the circuit diagram of the digitally synthesized CDR and the proposed embedded real-time QEC (ER QEC). Although the PI generates I/Q clocks, PVT variations and PI nonlinearity can introduce an initial quadrature error between *CKI* and *CKQ*. To correct this error, the proposed ER QEC shares the same PD logic as the CDR engine, thereby minimizing hardware overhead.

The demultiplexed $D_{n,32}$ and $T_{n,32}$ are processed by the PD logic to generate *UP*/*DN*, which are simultaneously fed into both the CDR engine and the ER QEC engine. Since the PI is controlled by a 7-bit code covering 360° in 128 steps, a difference of 32 codes corresponds to 90°. The CDR engine uses its delta-sigma modulator (DSM) output as *PCW* to drive the I-phase mixer and generate *CKI*/*CKIB*. The ER QEC engine, on the other hand, generates $PCW_{QEC} = PCW + (DSM_{QEC} - 32)$ to drive the Q-phase mixer and generate *CKQ*/*CKQB*. Since both DSMs are initialized to 64, the initial relation becomes $PCW_{QEC} = PCW + 32$, which provides a nominal quadrature starting point. The ER QEC loop then adjusts DSM_{QEC} so that *CKQ* converges to the actual quadrature phase with respect to *CKI*.

Although both engines share the same *UP*/*DN*, they converge to different phase targets because the ER QEC engine continuously adjusts the PCW_{QEC} toward the actual quadrature point; therefore, the loop gains are carefully

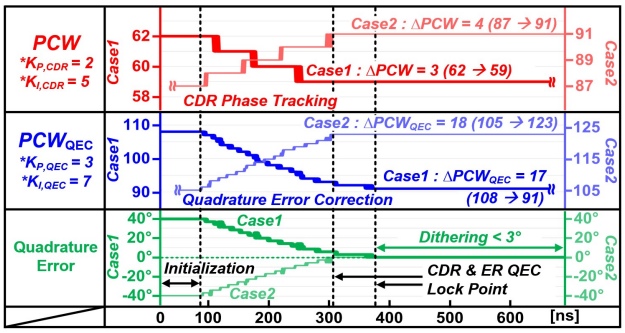


Fig. 7. Simulation results of ER QEC including two representative cases.

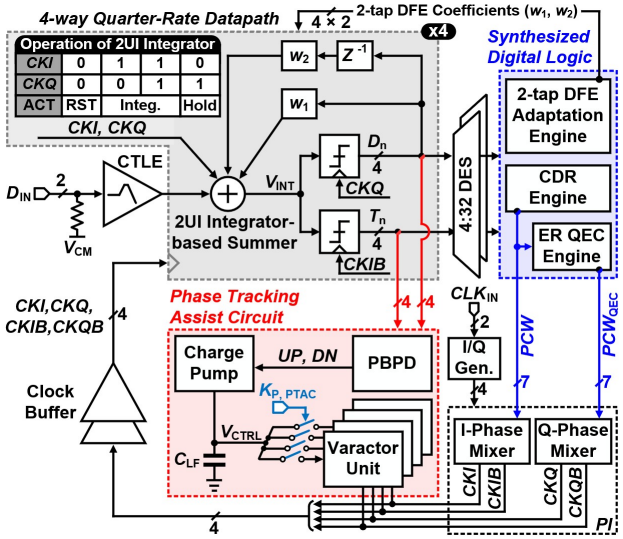


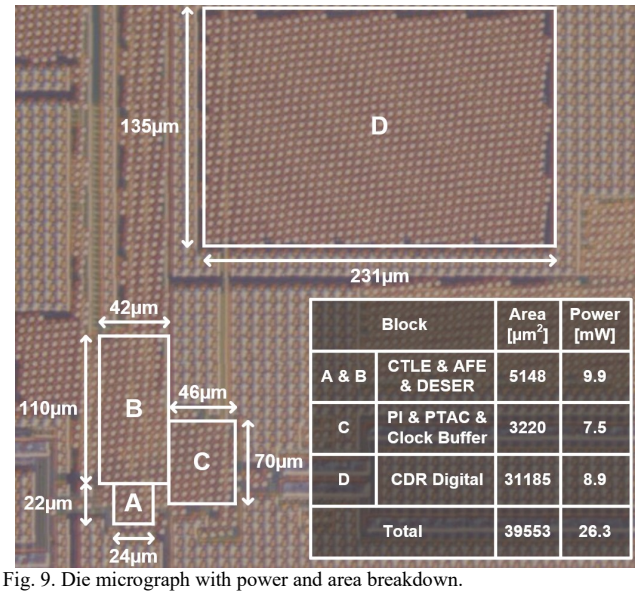
Fig. 8. Overall architecture of proposed baud-rate receiver.

designed to separate the loop bandwidths and prevent mutual interference. As shown in Step 1 of Fig. 6, an initial quadrature error exists. In Step 2, the CDR engine tracks the data lock point through the I-phase with a low loop gain for stable operation, while the ER QEC engine adjusts the Q-phase toward the actual quadrature point with a higher loop gain for faster correction. As a result, in Step 3, both loops converge with the quadrature error corrected. Fig. 7 shows simulation results for initial quadrature errors of +40° and −40°, demonstrating that the ER QEC converges toward 0° quadrature error in both cases. This confirms robust convergence behavior for both positive and negative initial error conditions.

III. Circuit Implementation

Fig. 8 illustrates the overall receiver architecture. The analog front-end (AFE) consists of a differential termination, a continuous-time linear equalizer (CTLE), and a 4-way datapath. The CTLE employs a Cherry–Hooper topology to achieve AC gain peaking with minimal area and power overhead. It provides a DC gain range from −8 dB to 1.8 dB, a maximum AC gain of 14.4 dB, and a tunable peaking frequency from 11 GHz to 22 GHz. An integrator-based summer is adopted for low-power dynamic operation, and its D_n and T_n outputs are reused as inputs to the PTAC and DLF. The use of this summer enables pattern-based phase detection in the analog domain, making it compatible with the PTAC. The deserialized outputs are forwarded to the DLF, where the CDR and ER QEC engines employ first-order DSMs to generate phase control words for the PI mixers. In addition, an adaptation engine for a 2-tap decision feedback equalizer (DFE) is incorporated to provide adaptive equalization operation across various channel conditions.

In the clock path, the forwarded differential clock is converted into four phases by the I/Q generator and interpolated by current-mode logic (CML)-based PI mixers to produce quarter-rate clocks for the datapath. The PTAC varactor units are connected to the PI output clocks, enabling fine phase tuning through RC-delay modulation. To ensure linear phase control with $K_{P,PTAC}$, the varactor units are weighted with scaling factors of ×1, ×2, ×2, and ×4. A first-order loop filter is employed at the charge-pump output to ensure stable operation. The logic gates in the PBPD and MFL are implemented using a full-custom layout to minimize area and power consumption.



Block		Area [μm²]	Power [mW]
A & B	CTLE & AFE & DESER	5148	9.9
C	PI & PTAC & Clock Buffer	3220	7.5
D	CDR Digital	31185	8.9
Total		39553	26.3

Fig. 9. Die micrograph with power and area breakdown.

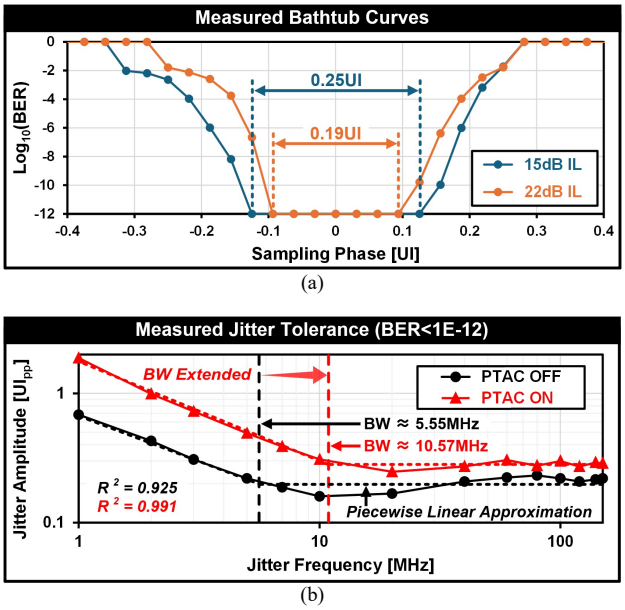


Fig. 10. Measurement results of (a) bathtub curves and (b) jitter tolerance at 32 Gb/s with and without PTAC.

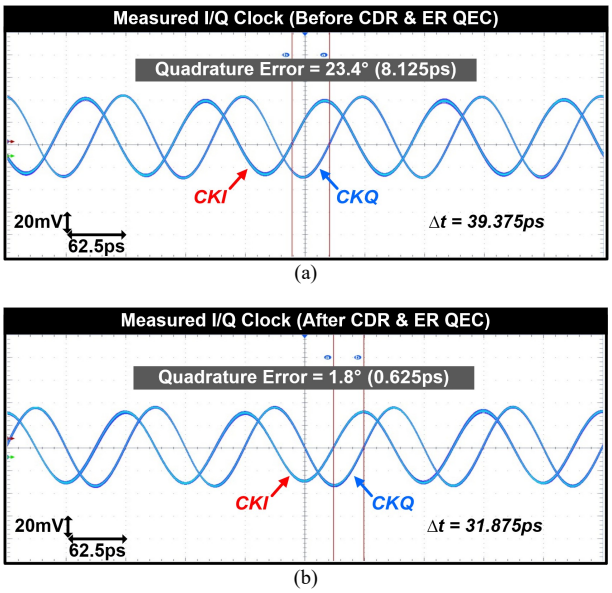


Fig. 11. Measurement results of the recovered 8-GHz I/Q clocks (a) before and (b) after enabling CDR and ER QEC.

IV. Measurement Results

The proposed receiver prototype is fabricated in a 40-nm CMOS process and occupies an active area of 0.039 mm^2, as shown in Fig. 9. Operating at 32 Gb/s from a 0.9-V supply, it consumes 26.3 mW with an energy efficiency of 0.82 pJ/b. To demonstrate the PTAC and ER QEC under various conditions, two channels comprising SMA cables and FR4 traces are used, providing insertion losses of 15 dB and 22 dB. Fig. 10(a) presents the measured bathtub curves for the two channels, achieving sampling margins of 0.25 UI and 0.19 UI, respectively. Fig. 10(b) shows the measured JTOL at 32 Gb/s with a BER under 10^{-12}. When the PTAC is disabled, a piecewise linear approximation yields an effective bandwidth of 5.55 MHz and a JTOL of 0.22 UI at 100 MHz. With the PTAC enabled, the effective bandwidth increases to 10.57 MHz, and the JTOL at 100 MHz improves to 0.30 UI. Fig. 11 shows the measurement results of the recovered clock. Before enabling the CDR and ER QEC, the quadrature error is 23.4°. When both loops are enabled, the error is corrected to 1.8°. The recovered clock shows a 1.583 ps RMS jitter and an 11.02 ps peak-to-peak jitter. Thanks to a power-efficient AFE and shared logic, the proposed receiver achieves the best figure-of-merit (FoM) of 37.3 fJ/b/dB, as summarized in Table I.

TABLE I. Comparison with State-of-the-Art PI-Based CDRs.

	JSSC '23 [4]	ISSCC '24 [8]	JSSC '25 [7]	ISSCC '25 [9]	This Work
Technology	22nm	28nm	28nm	28nm	40nm
Clocking Type	PLL + PI	PI	FDIV + PI	PI	PI
CDR Loop Control Type	Ana. : VCO Dig. : PI	Ana. : X Dig. : PI	Ana. : X Dig. : PI	Ana. : X Dig. : PI	Ana. : PI Dig. : PI
Jitter Tolerance Enhancement	O	X	X	X	O
Quadrature Error Correction	X	O	X	O	O
Modulation	NRZ	PAM-4	NRZ	NRZ	NRZ
Data Rate [Gb/s]	26	112	32	56	32
Channel Loss [dB]	32	8.5	15	34.6	22
Jitter Tolerance @100MHz [UI_{pp}]	0.45	0.08[$]	0.12	0.17	0.3
Area [mm^2]	0.251	0.236	0.105	0.208	0.039
Power [mW]	86	140.3[&]	57.92	218.9	26.3
Energy Efficiency [pJ/b]	3.3	1.25[&]	1.81	3.91	0.82
FoM [fJ/b/dB]	103	147[&]	121	113	37.3

[&]Tx Excluded [$]BER<1E-7

V. Conclusion

This paper presents a 32-Gb/s baud-rate receiver with a JTOL-enhanced CDR employing PTAC and ER QEC. The proposed PTAC realizes an analog proportional path by using an analog phase detector, charge-pump-based accumulation, and varactor-based delay control, thereby overcoming the limitation of the conventional PI-based CDR. As a result, the proposed CDR obtains faster timing-variation tracking than phase updates performed through the DLF, effectively compensating for jitter components and improving the loop bandwidth and high-frequency JTOL. In addition, the proposed ER QEC reuses the CDR logic while introducing a separate loop gain and an independent PI mixing scheme for the I- and Q-phases. This approach corrects quadrature error caused by PI nonlinearity and PVT variations without requiring dedicated calibration hardware. Both simulation and measurement results demonstrate that the proposed scheme corrects the quadrature error to within 2° regardless of its polarity. The proposed receiver operates robustly under channel losses of up to 22 dB and achieves an FoM of 37.3 fJ/b/dB.

Acknowledgment

This work was supported by the NRF grant funded by the MSIT (RS-2024-00414230, RS-2025-00554635), and the EDA tool was supported by the IDEC, Korea.

References

[1] J. Liang *et al.*, "On-Chip Jitter Measurement Using Jitter Injection in a 28 Gb/s PI-Based CDR," *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 750-761, Mar. 2018.

[2] K. Park *et al.*, "A 6.4-to-32Gb/s 0.96pJ/b Referenceless CDR Employing ML-Inspired Stochastic Phase-Frequency Detection Technique in 40nm CMOS," *IEEE ISSCC*, pp. 124-126, Feb. 2020.

[3] Y. Jung *et al.*, "A 16-to-30-Gb/s 1.03-pJ/b Baud-Rate Receiver With Referenceless CDR Employing Integrated Pattern Decoding Technique in 28-nm CMOS," *IEEE TCAS-I*, vol. 72, no. 11, pp. 6517-6527, Nov. 2025.

[4] Y. -C. Liu *et al.*, "A 103 fJ/b/dB, 10–26 Gb/s Receiver With a Dual Feedback Nested Loop CDR for Wide Bandwidth Jitter Tolerance Enhancement," *IEEE Journal of Solid-State Circuits*, vol. 58, no. 10, pp. 2801-2811, Oct. 2023.

[5] Y. Shin *et al.*, "A Digital-PLL-Based Quadrature Clock Generator for a Low-Power and Jitter-Filtering-Capable Clock Distribution Scheme in High-Speed DRAM Interfaces," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 2, pp. 509-518, Feb. 2025.

[6] S. Kang *et al.*, "A 1.19-pJ/b 32-Gb/s Baud-Rate Receiver Employing 2UI Integrated Pattern-Based CDR and DFE Adaptation Without Data-Level Reference," *IEEE Journal of Solid-State Circuits*, vol. 61, no. 2, pp. 434-447, Feb. 2026.

[7] J. Kim *et al.*, "A 4 × 32 Gb/s 1.8 pJ/bit Collaborative Baud-Rate CDR With Background Eye-Climbing Algorithm and Low-Power Global Clock Distribution," *IEEE Journal of Solid-State Circuits*, vol. 60, no. 8, pp. 2751-2764, Aug. 2025.

[8] Y. -P. Lin *et al.*, "A 2.16pJ/b 112Gb/s PAM-4 Transceiver with Time-Interleaved 2b/3b ADCs and Unbalanced Baud-Rate CDR for XSR Applications in 28nm CMOS," *IEEE ISSCC*, pp. 136-138, Feb. 2024.

[9] Y. -P. Lin *et al.*, "A 2.06pJ/b 106.25Gb/s PAM-4 Receiver with 3-Tap FFE and 1-Tap Speculative DFE in 28nm CMOS," *IEEE ISSCC*, pp. 146-148, Feb. 2025.