A High-Side Current-Sensing Instrumentation Amplifier with 10 V/ns Common-Mode Transient Tolerance and −8 V to 70 V Input Range

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***Abstract*—High-side current sensing requires high precision amplifiers capable of handling wide-range and fast-varying common-mode (CM) voltages. This paper presents a capacitively coupled instrumentation amplifier (CCIA) that operates in low-voltage domain while tolerating up to 70 V CM and transients as fast as 10 V/ns. An adaptive PWM-rejection scheme actively resets the input and feedback capacitors to enhance resilience against fast CM transients. A charge-pump-driven high-voltage (HV) chopper tracks large CM swings, preventing device overstress. In addition, a segmented ripple reduction loop (SRRL) suppresses chopping-induced ripple without disturbing square-wave inputs, thereby overcoming the limitation of conventional RRLs that cannot handle discontinuous inputs. A negative charge pump further extends the input CM range to −8 V, enabling robust operation under negative inputs. Fabricated in a 0.18-µm BCD process without using HV-MOSFETs, the prototype achieves a −8 V to 70 V CM range, 160 dB CMRR, 30 nV/√Hz input-referred noise, and 8µV offset, consuming 1.12 mA from a 5 V supply.**

***Keywords*—capacitively coupled instrumentation amplifier, PWM rejection, high-side current sensing, ripple reduction, high-voltage chopper, negative charge pump.**

I. Introduction

In industrial systems, accurate high-side current sensing is essential in applications such as three-phase AC motors, battery management systems (BMS), power management, and overcurrent protection. Compared with low-side sensing, high-side sensing eliminates the influence of load-to-ground resistance and so enables more precise current measurement and protection. The primary challenges for high-side sensing include accommodating a wide input common-mode (CM) range and tolerating fast CM transients associated with pulse width modulation (PWM). Furthermore, integrating key on-chip auxiliary circuits, such as charge pump and HV clock generator, is desirable to reduce the board-level complexity. Finally, to prevent latch-up during negative input excursions, the amplifier should support negative-voltage operation.

State-of-the-art high-side current sensors tend to employ high-voltage (HV)-tolerant amplifiers to handle HV signals [1]-[3]. Current balancing instrumentation amplifiers (CBIAs) provide high bandwidth-power efficiency and CMRR [2][3], both of which are critical for current sensing. However, HV-MOSFETs are still required, which limits the achievable CM transient tolerance to approximately 70 V/µs. Capacitively-coupled architectures provide an alternative, where the input capacitors suppress slow HV-CM variations while preserving the differential signal integrity [4][5]. However, charging and discharging of these input capacitors restrict the speed of CM transient response. Moreover, integrating HV choppers poses challenges in maintaining fast CM transient response [3].

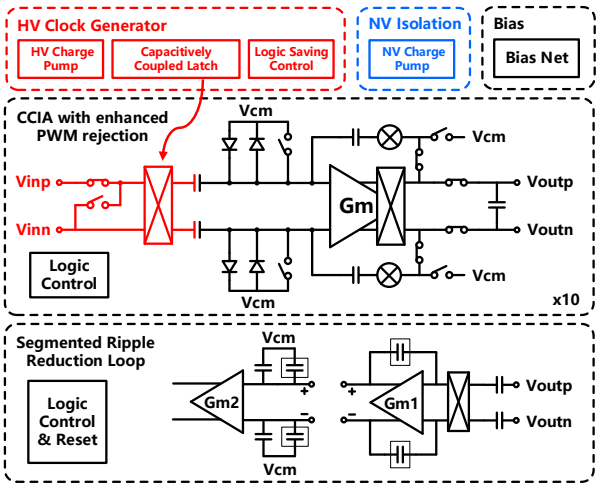

Fig. 1. System architecture of the proposed CCIA.

To overcome the challenges of high-side current sensing under large and fast CM transients, this work (Fig.1) presents a capacitively coupled instrumentation amplifier (CCIA) that operates with a low-voltage (LV) core while tolerating HV input CM signals. Key techniques include a dead-time reset (DTR) scheme for enhanced PWM rejection up to 10 V/ns, a switch-free charge pump for driving the HV input chopper, a segmented ripple reduction loop (SRRL) for suppressing chopping-induced ripple while preserving square-wave input signals, and an auxiliary negative charge pump to extend the input CM range to −8 V. Together, these innovations address the key challenges of high-side current sensing, resulting in a robust, low-noise, and wide-input-range CCIA.

II. System Architecture

A. HV Input Chopper

Conventional HV clock generators based on capacitive coupling [4] suffer from device breakdown because of their limited CM transient tracking capability. Level shifter-based generators [1][3] can achieve faster CM transient response (~60 V/µs), but require an additional HV supply and remain speed-limited. In this work, a switch-free charge pump is implemented to generate a stable +4 V output referenced to the input CM voltage. Operating with 5-V LV devices, the charge pump rapidly tracks CM variations, preventing device breakdown and enabling robust HV clock generation (Fig. 2, top).

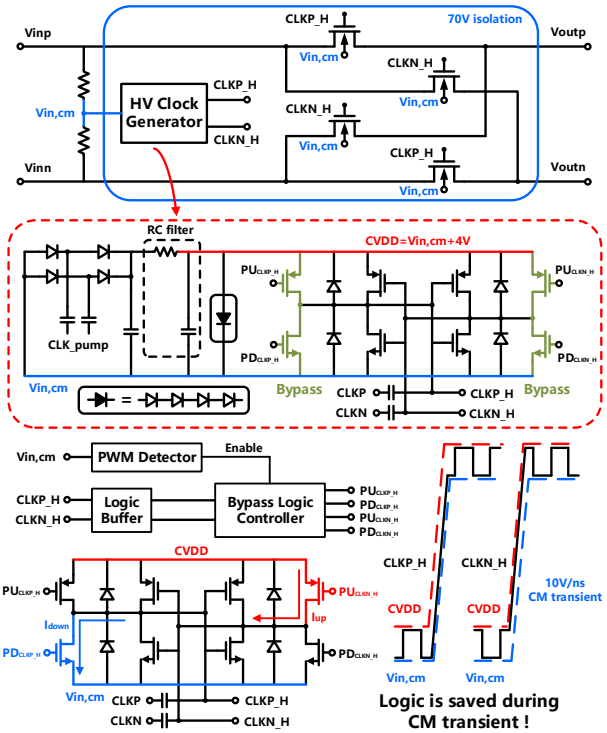

Fig. 2. HV chopper (top), HV clock generator (middle), logic controller (bottom left), and illustration of HV chopping clock during CM transients (bottom right).

As illustrated in Fig. 2 (middle), the HV clock generator consists of a switch-free charge pump, a capacitively coupled latch, and a logic-saving controller. The charge pump is based on Schottky barrier diodes instead of switches, enabling fast tracking of HV CM transients without device overstress. The output voltage is clamped to 4 V by cascaded diode-connected devices. An RC filter suppresses the ripple before the output serves as CVDD, the local supply of the HV chopper driver. By capacitively coupling a LV clock into the latch, an HV clock is produced to drive the HV chopper.

Although this charge pump provides a relatively stable output superimposed on the input CM voltage, the HV clock remains susceptible to fast CM transients (>100 V/μs), which may result in incorrect clock logic. Under this condition, the coupling capacitors are primarily charged through the diodes, as the latch must remain small to ensure easy switching. Consequently, both HV clock outputs (CLKP_H, CLKN_H) may temporarily collapse to the same logic level during fast CM transients, resulting in incorrect clock polarity. To solve this issue, a logic-saving controller with two bypass drivers is introduced (Fig. 2, bottom left). During fast CM transients, the controller restores the correct HV clock states through the bypass drivers based on the buffer logic, thereby preserving the intended clock polarity and preventing logic errors.

B. Enhanced PWM Rejection

The CCIA inherently provides HV isolation, as the input capacitors reject low frequency CM voltage without affecting the differential-mode (DM) signal. However, during fast CM transients, the large bias resistors in the CCIA cannot supply sufficient current to rapidly charge and discharge the input capacitors, potentially leading to device overstress. Therefore, further techniques are required to enhance PWM rejection.

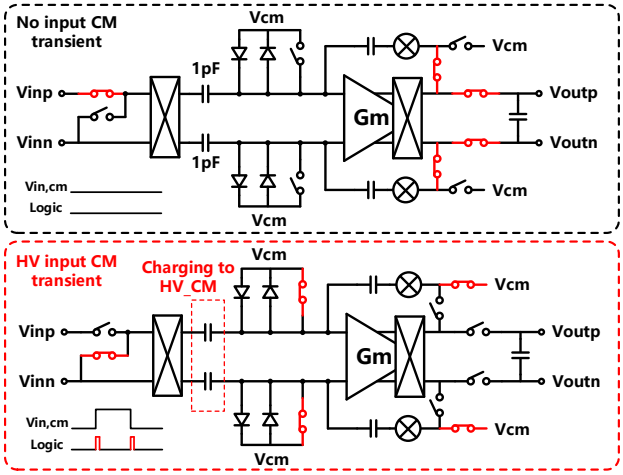

Fig. 3. Enhanced PWM rejection using the proposed dead-time reset (DTR) technique.

Common-mode feedforward (CMFF) is a widely adopted technique [6], but its effectiveness degrades under large CM inputs due to mismatch in the feedforward capacitors. Dead-time reset (DTR) [7] has also been demonstrated to enhance PWM rejection. As illustrated in Fig. 3 (bottom), when a fast CM transient (> 20 V/μs) is detected, the CCIA enters a reset state. Unlike [7], both the input and feedback capacitors are reset simultaneously, and the input capacitors are connected to the same HV node to block the CM input. Meanwhile, the CCIA output is temporarily disconnected and held by a load capacitor. After the transient subsides, the CCIA returns to normal operation and reconnects to the load.

In [7], if the DM input varies during the CM transient, the DM signal will be stored in the input capacitors, resulting in large output ripple after the transient ends. In contrast, the proposed scheme prevents the DM signal propagation into the CCIA during the reset period, thereby eliminating the resulting ripple. The reset duration is typically less than 1 μs and so has negligible impact on the output signal.

C. Segmented Ripple Reduction Loop (SRRL)

Ripple reduction loops (RRLs) are widely employed to suppress the output ripple introduced by chopping [4]. By generating notches at the chopping frequency and its higher-order harmonics, the RRL can effectively attenuate the ripple components at these frequencies. However, this mechanism inherently limits the usable signal bandwidth to below the chopping frequency. In particular, when processing square-wave signals (Fig. 4, top right), high-frequency harmonics may couple into the integration capacitor, producing voltage deviation and residual ripple that the monolithic, bandwidth-limited RRL cannot suppress effectively.

To address this limitation, a segmented ripple reduction loop (SRRL) is proposed that enables ripple-free processing of square-wave signals. Since offset and the associated ripple are relatively static, the ripple and square-wave output can be distinguished according to their amplitudes. As illustrated in Fig. 4 (bottom), the integrator and feedback transconductor G_{m2} are separated into two segments to selectively forward ripple to G_{m2} while blocking square-wave transitions. These two segments are interconnected by two pairs of ping-pong capacitors C_{pp} operating at 2× the chopping frequency. While one capacitor pair performs integration, the other transfers

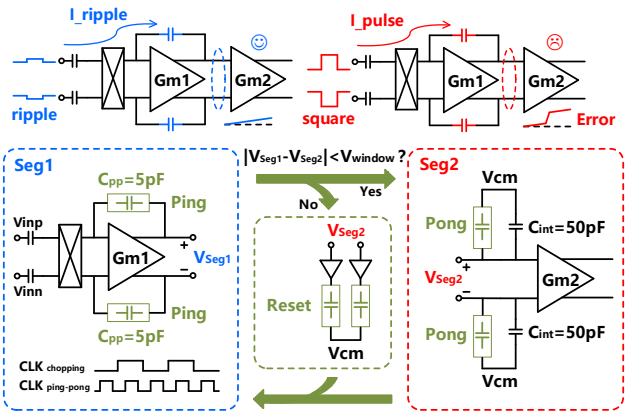

Fig. 4. Mechanism of ripple reduction and square-wave-induced integration error (top), segmented ripple reduction loop (SRRL) (bottom).

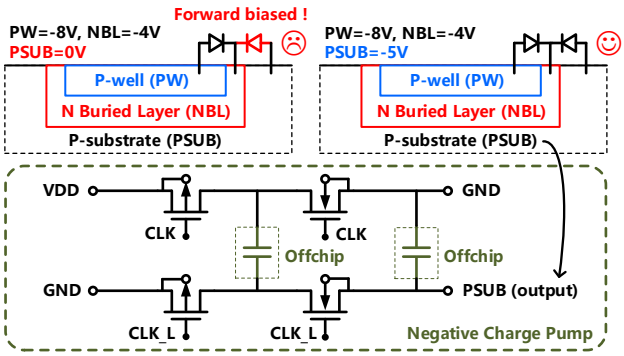

Fig. 5. Negative voltage isolation (NVI) and the negative charge pump.

charge to the actual 50 pF integration capacitors C_{int}, thereby allowing continuous ripple reduction.

A decision mechanism (Fig. 4, bottom) compares $|V_{Seg1}-V_{Seg2}|$ with a predefined threshold V_{window} to identify square waves (i.e., $|V_{Seg1}-V_{Seg2}| > V_{window}$) and reset the ping-pong capacitor by the buffers in the next cycle. This ensures V_{Seg2} remains stable and prevents residual ripple generation. Noted that the ping-pong operation introduces additional phase shift in the loop, which can be mitigated by increasing the ping-pong frequency and the capacitance of C_{int}.

D. Negative Voltage Isolation (NVI)

In BCD process, HV isolation is typically implemented using isolation rings. The PN junction between P-well (PW) and N-buried layer (NBL) can only tolerate a reverse voltage of about 5 V. In this work, the PW potential follows the input CM voltage, while the NBL is powered by a charge pump. As shown in Fig. 5 (top left), when the input CM voltage drops below -4 V, the PN junction between the NBL and the p-substrate (PSUB) may become forward-biased, potentially triggering latch-up.

To solve this issue, the PSUB is no longer tied to ground. Instead, an on-chip negative charge pump (NVCP) generates a -5 V bias for the PSUB (Fig. 5, top right). Since all active devices reside in the PW and are fully isolated from the PSUB, the NVCP introduces negligible ripple or noise into the signal path.

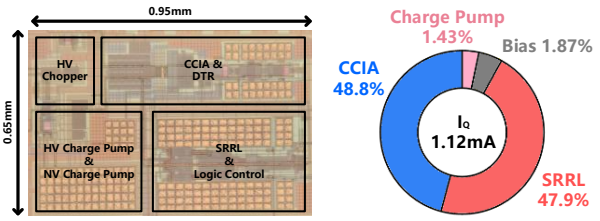

Fig. 6. Chip photo and power consumption distribution

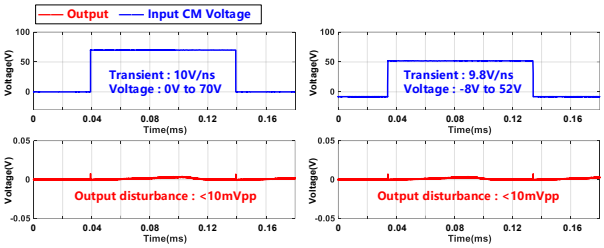

Fig. 7. Differential response of HV CM transient

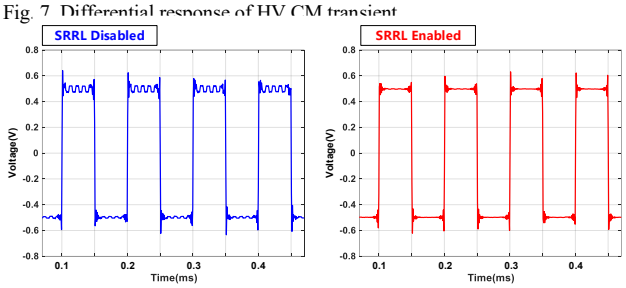

Fig. 8. Measured square-wave output with and without the proposed SRRL.

With this scheme, the NBL voltage is allowed to fall below 0 V. In the worst case, when the input CM voltage reaches -8 V, the NBL voltage becomes -4 V, leaving the PN junction between the NBL and PSUB nearly zero-biased and thereby preventing latch-up. The chip ESD structures are also implemented following this scheme to ensure safe operation under negative input voltages.

III. Measurement Results

The proposed CCIA was fabricated in a 0.18-μm BCD process, occupying an active area of 0.62 mm^2 (Fig. 6). The chip is packaged in DIP48 and consumes 1.12 mA from a 5V supply. Since no HV-MOSFETs are used in the CCIA, the area is smaller than that of conventional HV amplifiers [2][3].

The CCIA achieves a wide input CM range from -8 V to 70 V. The maximum CM voltage is limited by the process, while the minimum CM voltage is enabled by the proposed negative voltage isolation (NVI). Thanks to the enhanced PWM rejection, as is shown in Fig. 7, the CCIA can tolerate CM transients up to 10 V/ns and provide robust performance under negative CM input. In both cases, the CM transients cause negligible influences to the output, and the maximum output disturbance due to transients is less than 10 mV_{pp}.

Fig. 8 shows the measured output waveforms with and without the SRRL under a 10 kHz 100 mV_{pp} square-wave input. When the SRRL is disabled, the square-wave output is interpreted as ripple by the conventional RRL, resulting in an output ripple of approximately 50–60 mV. When the SRRL is enabled, the square-wave signal is correctly preserved, and no additional ripple is generated.

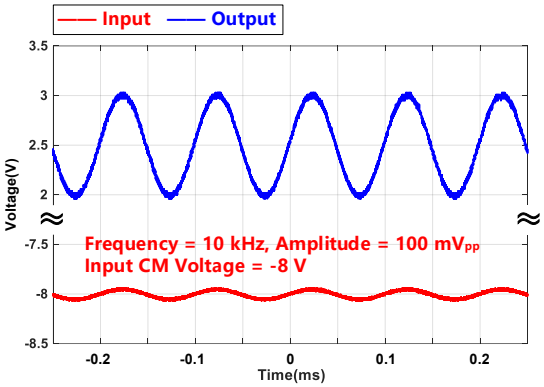

Fig. 9. Sine wave response under -8V input CM voltage

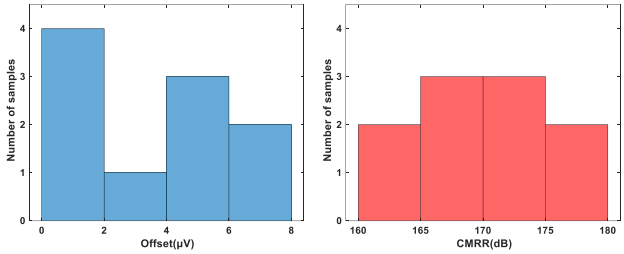

Fig. 10. Measured offset and CMRR across 10 samples.

Fig. 9 shows the CCIA output under a 10 kHz sine wave input when the input CM voltage drops to -8 V. The output remains stable without latch-up, validating the effectiveness of the proposed NVI technique.

Fig. 10 plots the measured input-referred offset and CMRR distributions across 10 chips. The maximum offset is below 8 μV with an average of 4 μV, while the minimum DC CMRR exceeds 160 dB. Fig. 11 shows the measured input-referred noise PSD. With chopping at 100 kHz, the 1/*f* noise is effectively suppressed, leaving a noise floor of 30nV/√Hz and a corner frequency below 10 Hz.

Table I compares this work with state-of-the-art HV-IAs and HV-OPAs. With the proposed DTR technique, the CCIA achieves a CM transient tolerance up to 10 V/ns (10000 V/μs) for enhanced PWM rejection, while the CMRR at 10 kHz is 94 dB. The proposed NVI technique enables reliable CCIA operation with negative CM input voltages down to -8 V. Operating from a single 5 V supply, this work also achieves highly competitive noise performance, offset, DR, and power efficiency (FoM).

IV. Conclusion

This paper addresses the challenges of high-side current sensing under large and fast CM transients. A capacitively coupled instrumentation amplifier (CCIA) enables a LV core while tolerating high CM voltages. To enhance robustness, a dead-time reset (DTR) technique improves PWM rejection under fast CM transients, while a segmented ripple reduction loop (SRRL) suppresses chopping-induced ripple without degrading square-wave inputs. In addition, an on-chip charge pump drives the HV chopper and a negative charge pump extends the input CM range. As a result, the proposed CCIA achieves robust operation with a wide CM input range and high precision, demonstrating competitive performance for high-side current sensing applications.

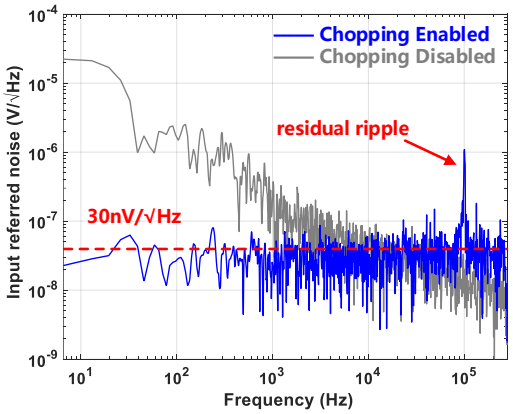

Fig. 11. Measured input-referred noise power spectral density (PSD).

TABLE I. Comparison with State-of-the-Art

	[4]	[1]	[2]	[7]	[3]	This work
Technology	0.7μm CMOS	0.18μm BCD	0.18μm BCD	0.18μm BCD	0.18μm BCD	0.18μm BCD
Topology	CCIA	CCOPA	CBIA	CCIA	CBIA	CCIA
Input CM range [V]	-30-30	0-47.6	0-34.5	-4-80	0.7-56.3	**-8-70**
NV Isolation	N/A	No	No	No	No	**Yes**
CM transient tolerance [V/μs]	0.002	1.3	N/A	15000	54	**10000**
CMRR @ DC [dB]	160	140	140	N/A	140	**160**
CMRR @ 10kHz [dB]	N/A	N/A	N/A	N/A	N/A	**94**
Noise density [nV/ √Hz]	31	14	39	12	19	30
Offset [μV]	5	N/A	5	3	10	8
Supply voltage [V]*	30/3	50	36	5	60/4.2	5
Supply current [mA]	0.026	1.15	0.7	0.546	0.3	1.12
Gain error [%]	N/A	N/A	N/A	0.15	0.2	**0.15**
DR [dB]	91	N/A	102	89	115	92
GBW [MHz]	1	3.55	400	N/A	40	14.2
FoM [dB]	172	N/A	184	170.7	192.7	176

N/A=No data available *HV supply +LV supply
FoM=Dynamic range + 10log(Bandwidth/Power)

Acknowledgment

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