A 0.1mm² 35GHz Octa-Phase Series-Resonance VCO with Dual Magnetic Coupling Achieving 198.1dBc/Hz FoMA in 65nm CMOS

Jiaming Pan, Haikun Jia, Huanyu Ge, Wei Deng, Baoyong Chi
School of Integrated Circuits, Tsinghua University, Beijing 100084, China
Email: jiahaikun@tsinghua.edu.cn

***Abstract*—This paper presents an octa-phase series-resonance (SR) voltage-controlled oscillator (VCO) introducing a dual-magnetic-coupling technique. To the best of the authors' knowledge, it is the first reported SR-VCO to support octa-phase outputs. By employing controlled intra-stage and cross-stage coupling, the proposed phase-shifting network breaks the inherent 90° limitation of transformer-based SR tanks to generate stable 45° phase steps. Fabricated in 65nm CMOS, the octa-phase VCO achieves a phase noise (PN) of −133.6dBc/Hz at a 10MHz offset, yielding the lowest PN normalized to 10GHz among the reported octa-phase oscillators. Consuming 36–53mW from a 0.75 V supply within a 0.1mm² core area, the proposed VCO realizes a peak FoM of 188.1dBc/Hz and a peak FoMA of 198.1dBc/Hz.**

Keywords—CMOS, millimeter-wave (mmWave), transformer, voltage-controlled oscillator (VCO), series resonance, multiphase, phase noise (PN)

I. Introduction

The rapid advancement of high-speed serial links towards 224Gb/s and 448Gb/s places unprecedented demands on low-jitter, multiphase clock generation. To minimize power and routing complexity in high-speed clock distribution, advanced SerDes systems typically adopt sub-rate multiphase clocking, with 1/8-rate clocking becoming a promising technique. This approach fundamentally relies on an ultra-low phase-noise (PN) oscillator to provide precisely spaced multiphase clocks.

Parallel-resonance (PR) oscillators are commonly used for multiphase generation. In conventional implementations, a capacitor-coupling network interconnects multiple resonant cores for multiphase clock generation (Fig. 1 top-left) [1]. This configuration, however, introduces weak passive coupling and suffers from phase-mode ambiguity. Magnetic and dual-injection coupled oscillators (Fig. 1 middle-left) strengthen inter-core coupling [2], but are still subject to phase-mode ambiguity, and present undesirable single-ended outputs. Alternatively, the rotary traveling-wave oscillator (Fig. 1 bottom-left) features inherent multiphase operation but typically yields a poor figure-of-merit (FoM) [3], with phase-mode ambiguity remaining as a critical issue. Due to such phase-mode ambiguity and inherent PN constraints imposed by the physical nature of the parallel-resonance tank, these structures cannot meet stringent timing demands.

An alternative approach is the series-resonance (SR) oscillator. With an equivalent resonant resistance of $1/Q^2$ relative to PR tanks, SR oscillators inherently facilitate ultra-low PN. Since transformers provide 90° phase shifts, it is intuitive to implement a transformer-based series-resonance oscillator with quadrature-phase outputs (Fig. 1 top-right) [4]. Directional ambiguity is avoided due to the strong asymmetry between forward and backward propagation. Although two resonant frequencies still exist, one can be suppressed by tuning the coupling coefficient. However, this topology is inherently limited to the 90° phase shift dictated by transformer physics and cannot be extended to higher-order multiphase operation. As a variant, [5] and [6] introduced the transformer pole-convergence technique (Fig. 1 middle-right) to reduce power consumption, at the cost of only supporting bi-phase outputs with the fixed 180° phase shift.

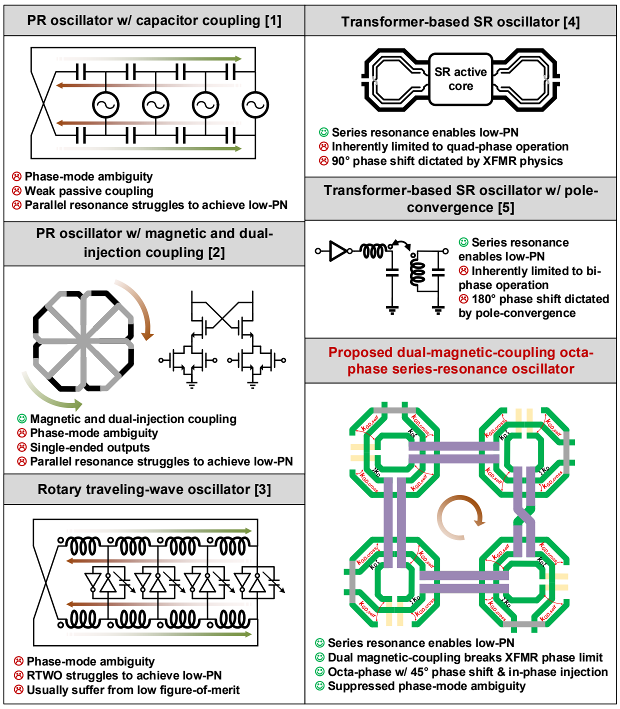

Fig. 1. Conceptual diagrams and key features of the existing parallel-resonance and series-resonance multiphase oscillators, and the proposed dual-magnetic-coupling octa-phase series-resonance oscillator.

To obtain multiphase clocks while achieving ultra-low PN, this paper presents an octa-phase series-resonance VCO with a dual-magnetic-coupling technique, which employs controlled intra-stage and cross-stage magnetic coupling to generate stable 45° phase steps while maintaining the optimal operating point of the series-resonance tank. To the best of the authors' knowledge, this is the first reported SR-VCO to achieve octa-phase outputs. Prototyped in 65nm CMOS, the proposed VCO achieves a FoMA of 198.1dBc/Hz with 0.1mm² core area.

II. Proposed Octa-Phase Series-Resonance VCO with Dual Magnetic Coupling

The key to realizing a multiphase low-PN SR-VCO lies in establishing the appropriate phase relationship between the

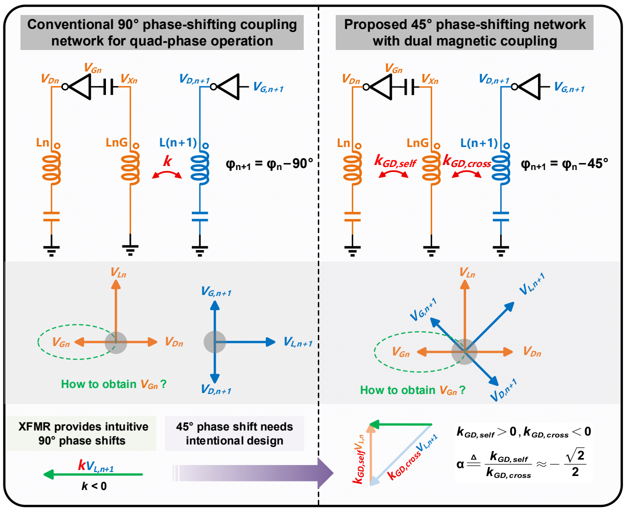

Fig. 2. Phase diagrams of the conventional 90° phase-shifting coupling network for quad-phase operation and the proposed 45° phase-shifting network with dual magnetic coupling.

input and output of the active stages via a passive coupling network. Fig. 2 (left) illustrates the simplified schematics and phase diagrams of a conventional 90° phase-shifting coupling network for quad-phase operation. The n-th stage comprises a drain inductor (L_n), a gate inductor (L_{nG}), and series capacitors. To analyze the phase behavior, the gate voltage (V_{Gn}), drain voltage (V_{Dn}), and the inductor voltage drop (V_{Ln}) are depicted as phasors, where V_{Gn} is in anti-phase with V_{Dn}. At resonance, the passive network presents a purely real impedance so that the drain current (I_{Dn}) is in phase with V_{Dn}, and V_{Ln} leads V_{Dn} by 90°.

For quad-phase resonance, assuming the (n+1)-th stage lags the n-th stage by 90° (i.e. $\varphi_{n+1} = \varphi_n - 90°$), the phasor diagram of the (n+1)-th stage can be obtained by rotating that of the n-th stage clockwise by 90°. Considering the passive network as a black box, the drain voltages V_{Dn} (n = 1, 2, 3, 4) serve as its inputs, while the gate voltages V_{Gn} (n = 1, 2, 3, 4) act as its outputs. The phasor condition for stable oscillation is satisfied only if the network can derive the required V_{Gn} from the injected V_{Dn}.

In the quad-phase topology, the transformer intuitively provides the 90° phase shift, aligning V_{Ln+1} parallel to the desired V_{Gn}. Consequently, the appropriate V_{Gn} can be successfully synthesized solely through the cross-stage coupling between L_{nG} and L_{n+1}.

Fig. 2 (right) illustrates the octa-phase case. Assuming $\varphi_{n+1} = \varphi_n - 45°$, the phasor diagram of the n-th stage remains consistent with the quad-phase case, while the phasor diagram of the (n+1)-th stage can be obtained by rotating that of the n-th stage clockwise by 45°. Since there is no voltage component directly parallel to V_{Gn}, intentional design is needed. Specifically, let V_{Ln+1} multiplied by negative $k_{GD,cross}$ serve as the first phasor, and V_{Ln} multiplied by positive $k_{GD,self}$ serve as the second phasor, with α defined as $k_{GD,self} / k_{GD,cross}$. If α is approximately $-\sqrt{2}/2$, the vector synthesis of these two phasors yields a V_{Gn} that satisfies the oscillation phase condition. In fact, four valid sign combinations of ($k_{GD,self}$, $k_{GD,cross}$) satisfy $\alpha \approx \pm\sqrt{2}/2$, corresponding to phase shifts of −45°, 45°, −135°, and 135°, respectively, though only the one depicted in the figure is utilized in this design.

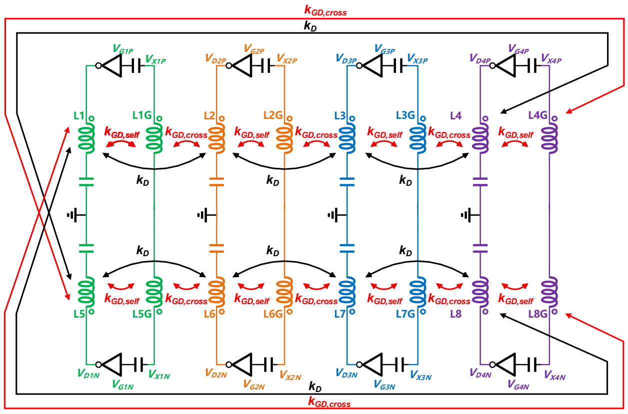

Fig. 3. Schematic of the proposed 45° phase-shifting network with dual magnetic coupling.

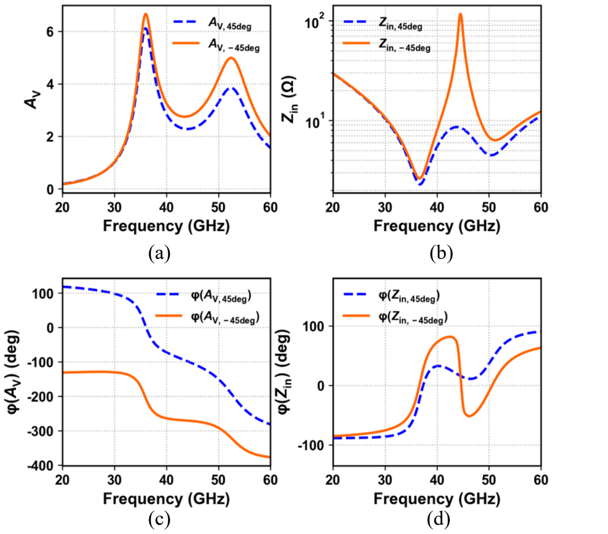

Fig. 4. Simulated passive gain, input impedance, and their phase shifts (a) A_V (b) Z_{in} (c) $\varphi(A_V)$ (d) $\varphi(Z_{in})$.

To realize the aforementioned coupling coefficients, a proposed 45° phase-shifting network utilizing dual magnetic coupling is illustrated in Fig. 3. The gate inductor L_{nG} is designed as localized to improve the quality factor (Q_G), rendering the magnetic coupling between gate inductors of different stages negligible. Meanwhile, the drain inductor L_n spans two adjacent stages, enabling cross-stage coupling with $L_{n-1,G}$. This arrangement inherently introduces a coupling coefficient, k_D, between adjacent drain inductors. However, since a given L_n is simultaneously coupled to both L_{n-1} and L_{n+1}, the extra voltage drops induced by these two couplings are strictly parallel to the intrinsic voltage drop across L_n itself. As a result, they can be equivalently modeled as a mere modification to the inductance value of L_n, thereby validating the preceding phasor analysis without introducing phase errors.

Though the network incorporates dual magnetic coupling, it can still be equivalently modeled as a transformer, which inherently possesses two oscillation modes. As illustrated in Fig. 4(c), the lower-frequency mode satisfies the −45° phase condition ($\varphi(A_V) = -180°$), while the higher-frequency mode satisfies the +45° phase condition. This phase discrepancy is reflected in the passive gain (A_V), as shown in Fig. 4(a). This

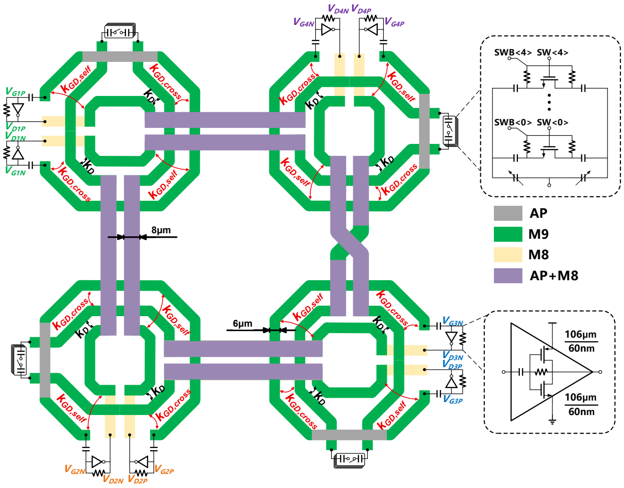

Fig. 5. Layout floorplan and detailed schematic of the proposed octa-phase series-resonance oscillator.

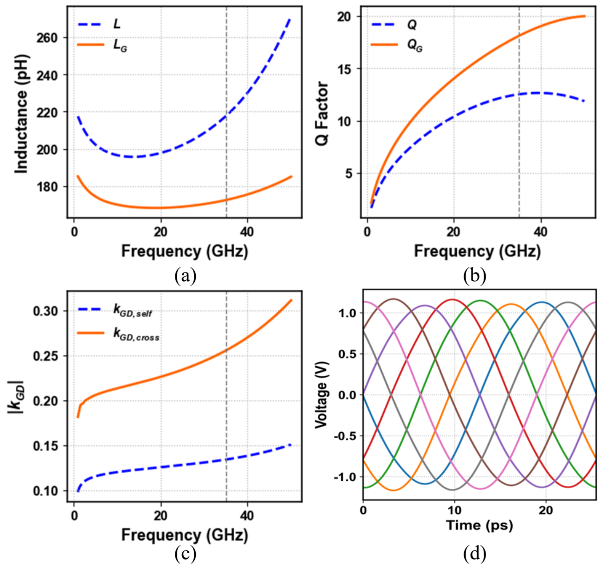

Fig. 6. (a)(b)(c) EM-simulated characteristics and (d) differential waveform of gate voltages of the implemented dual magnetic-coupling network.

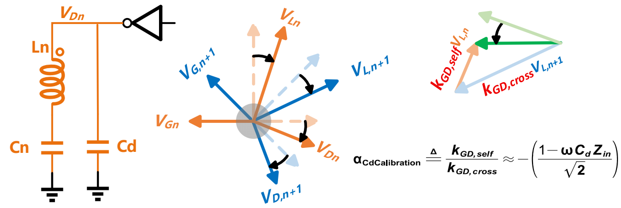

Fig. 7. Phase diagram with corrections for drain parasitic capacitance.

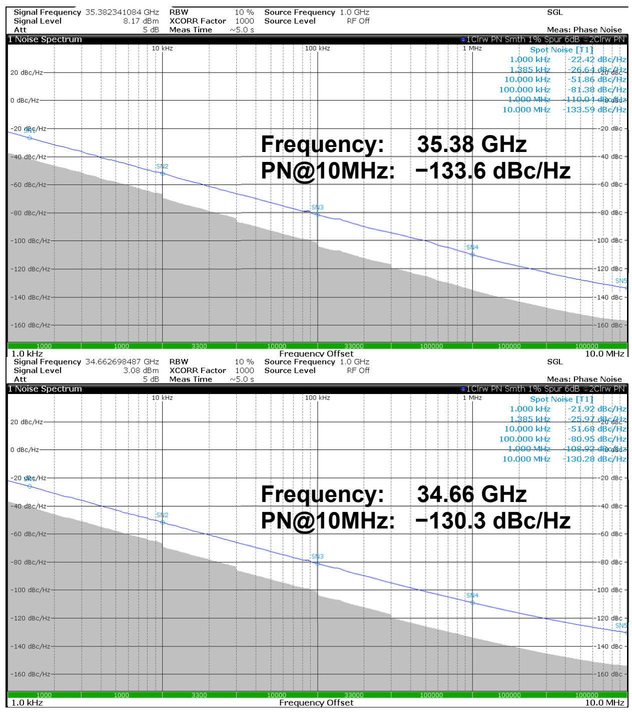

Fig. 8. Measured phase noise profiles at 35.4 and 34.7GHz.

indicates that the actual passive gain for the high-frequency parasitic mode must be evaluated under the +45° phase condition, resulting in a desired smaller gain. Specifically, the peak passive gain for the −45° mode around 36GHz is 6.6, whereas the peak gain for the +45° mode around 52GHz is 3.8, with a ratio of 1.74. The input impedance (Z_{in}, see Fig. 4 (b)) for the two modes are 2.7Ω and 4.5Ω, respectively, yielding a ratio of 1.7.

III. Circuit Implementation

Fig. 5 shows the layout floorplan and detailed schematic of the proposed octa-phase series-resonance oscillator, with the eight phases organized within four differential SR cores. The localized design of gate inductors enhances the quality factor (Q_G), which is crucial for PN especially when the equivalent transformer turns ratio is moderate. The drain inductors span two adjacent stages, enabling cross-stage coupling. Each core features an independently tuned 5-bit capacitor bank, thereby allowing for the frequency tuning and the calibration of mismatches. By employing self-biased inverters as the active core, external bias voltages are eliminated. Both PMOS and NMOS transistors are sized at 106μm/60nm.

EM-simulated characteristics are presented in Fig. 6. Differential inductances at drain and gate terminals measure 220 pH and 170 pH, with Q factors of 12 and 18, respectively. The coupling coefficients are $k_{GD,self} = 0.14$ versus $k_{GD,cross} = -0.25$. |α| is slightly less than 0.6 because parasitic drain capacitance introduces an additional gate-to-drain phase shift, as illustrated in the phasor diagram in Fig. 7. Under typical conditions in this work, this correction term is around 0.1. With appropriate capacitor bank control words, uniformly distributed differential gate voltage waveforms are simulated, as shown in Fig. 6(d).

IV. Measurement Results

The proposed octa-phase series-resonance oscillator with dual magnetic coupling was designed and fabricated in a 65nm CMOS process. Fig. 9 shows the die micrograph of the VCO, with the core area of only 0.32mm × 0.32mm, excluding the output buffers and pads. Under a 0.75V supply voltage, the oscillator dissipates 36–53mW. Measured using an R&S FSWP50 phase-noise analyzer, the VCO achieves a PN ranging from −133.6 to −130.2dBc/Hz at a 10MHz offset across the carrier frequency band of 34.5–37.0GHz, as shown in Fig. 10(a). The oscillator achieves a peak FoM of 188.1dBc/Hz and a peak FoM_A of 198.1dBc/Hz according to Fig. 10(b).

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH THE PRIOR-ART MM-WAVE MULTIPHASE AND SERIES-RESONANCE OSCILLATORS

	Series Resonance			Parallel Resonance		
	This work	S. Zhang JSSC'2025 [4]	J. Guo ISSCC'2025 [5]	Y. Zhao ISSCC'2024 [2]	X. Chen JSSC'2023 [7]	M. Shehata JSSC'2021 [3]
Technology	**65nm CMOS**	65nm CMOS	65nm CMOS	65nm CMOS	28nm CMOS	22nm FD-SOI
Topology	**Dual-magnetic-coupled SR**	SR	SR w/ pole-convergence	Magnetic + dual-injection-coupled PR	Class-F PR	RTWO with distributed stubs
No. of Phases	**8**	4	2	8	4	16
Supply (V)	**0.75**	1.2	1.2	0.55	0.6	0.8
Power (mW)	**36–53**	228–330	159–164	5.8	29.2	20
Tuning Range (GHz)	**34.5–37.0**	10.3–11.1	7.7–9.1	20–23.8	25.7–30.7	26.2–30
PN@10MHz (dBc/Hz)	**−133.6 to −130.2**	−152.5 to −145.7	−152.9	−129.3	−133.3	−128.9
PN@10MHz Norm. to 10GHz (dBc/Hz)	**−144.6 to −141.0**	−152.8 to −146.6	−152	−136.8	−141.2	−138.4
FOM@10MHz (dBc/Hz)	**188.1–185.4**	187.3–183.0	190	189.2	186.8	185.4
FOM_A@10MHz (dBc/Hz)	**198.1–195.4**	190.8–186.5	197.2	200.7	192.7	191.6
Core Area (mm^2)	**0.1**	0.45	0.192	0.07	0.26	0.24

$FoM = |PN| + 20\log_{10}(f_0/\Delta f) - 10\log_{10}(Pdc/1mW)$ $FoM_A = FoM + 10\log_{10}(1mm^2/Area)$ $PN\ Norm.\ to\ 10GHz = PN - 20\log_{10}(f_0/10GHz)$

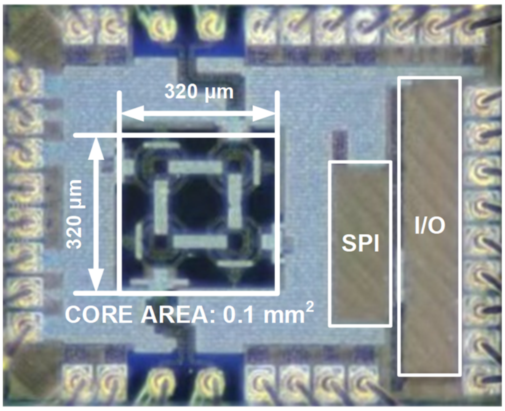

Fig. 9. Die micrograph of the proposed octa-phase series-resonance oscillator with dual magnetic coupling.

TABLE I provides a performance summary and comparison between the proposed octa-phase SR-VCO and the prior-art mm-wave multiphase and series-resonance oscillators. By employing the proposed dual-magnetic-coupling technique, this work realizes octa-phase signal generation in a SR-VCO, whereas prior arts are limited to four phases. It also achieves a smaller core area, a higher operating frequency, and a superior FoM_A at a 10MHz offset compared with the other listed SR-VCOs. Benefiting from the inherent advantages of the SR topology, the proposed VCO exhibits lower PN and normalized PN at a 10MHz offset compared with the PR-VCOs summarized in TABLE I. A detailed comparison with a broader range of representative multiphase oscillators is presented in Fig. 10(c)(d). Notably, this work achieves the lowest normalized PN at a 10MHz offset among the surveyed octa-phase oscillators, while maintaining competitive FoM and FoM_A.

V. CONCLUSION

To the best of the authors' knowledge, this paper presents the first octa-phase series-resonance VCO utilizing a dual-magnetic-coupling technique. By employing controlled intra-stage and cross-stage magnetic coupling, the proposed design overcomes the inherent 90° limitation of the conventional transformer-based SR-VCO, successfully generating stable 45° phase steps with suppressed phase-mode ambiguity. Prototyped in 65nm CMOS, the VCO operates from 34.5 to 37.0GHz while achieving a phase noise of −133.6 to −130.2dBc/Hz at a 10 MHz offset, resulting in a peak FoM of 188.1dBc/Hz, and demonstrating the lowest normalized PN among surveyed octa-phase oscillators. With a compact core area of 0.1 mm^2, it realizes a peak FoM_A of 198.1dBc/Hz.

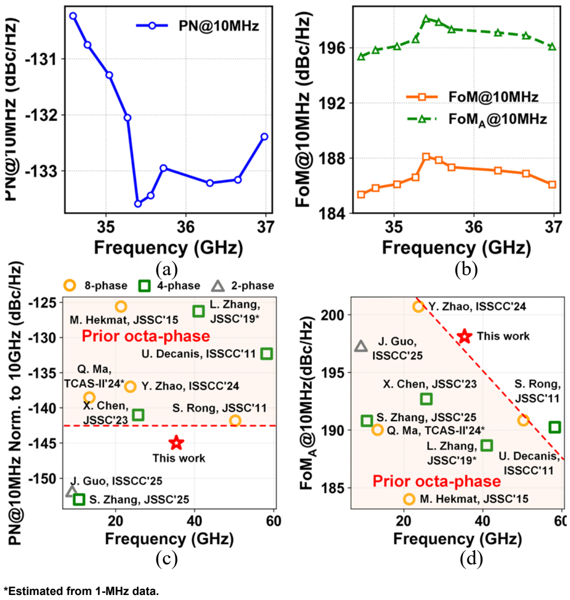

Fig. 10. Measured (a) PN, (b) FoM and FoM_A across the frequency-tuning range and detailed comparison of (c) PN normalized to 10GHz and (d) FoM_A at a 10MHz offset.

REFERENCES

[1] G. Li and E. Afshari, "A Low-Phase-Noise Multi-Phase Oscillator Based on Left-Handed LC-Ring," IEEE J. Solid-State Circuits, vol. 45, no. 9, pp. 1822–1833, Sep. 2010.

[2] Y. Zhao et al., "19.4 A 0.07 mm^2 20-to-23.8GHz 8-phase Oscillator Incorporating Magnetic + Dual-Injection Coupling Achieving 189.2dBc/Hz $FoM_{@10MHz}$ and 200.7dBc/Hz FoM_A in 65nm CMOS," in 2024 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, Feb. 2024, pp. 354–356.

[3] M. A. Shehata, M. Keaveney, and R. B. Staszewski, "A Distributed Stubs Technique to Mitigate Flicker Noise Upconversion in a mm-Wave Rotary Traveling-Wave Oscillator," IEEE J. Solid-State Circuits, vol. 56, no. 6, pp. 1745–1760, Jun. 2021.

[4] S. Zhang et al., "A Transformer-Based Series-Resonance CMOS VCO," IEEE J. Solid-State Circuits, vol. 60, no. 2, pp. 529–542, Feb. 2025.

[5] J. Guo et al., "A differential series-resonance CMOS VCO with pole-convergence technique achieving 202.1 dBc/hz FoM_{TA} at 10MHz offset," in 2025 IEEE International Solid-state Circuits Conference (ISSCC), San Francisco, CA, USA, Feb. 2025, pp. 332–334.

[6] J. Chen, K. Xu, T. Siriburanon, and R. B. Staszewski, "An 8.1-to-9.9GHz Single-Core Pseudo-Series-Resonance Oscillator Achieving -128.7dBc/Hz PN at 1MHz," in 2025 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, Feb. 2025, pp. 1–3.

[7] X. Chen, Y. Hu, T. Siriburanon, J. Du, R. B. Staszewski, and A. Zhu, "A 30-GHz Class-F Quadrature DCO Using Phase Shifts Between Drain–Gate–Source for Low Flicker Phase Noise and I/Q Exactness," IEEE J. Solid-State Circuits, vol. 58, no. 7, pp. 1945–1958, Jul. 2023.