An Ultra-Compact Transformer-based 3-Way Series Doherty Power Amplifier in 22-nm CMOS FD-SOI for Q-band SATCOM Applications

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***Abstract*— This work presents an ultra-compact 3-way series Doherty power amplifier operating in the Q-band for satellite communications applications. Implemented in the 22-nm FD-SOI CMOS technology, the proposed design features a highly compact area of $0.148mm^2$, suitable for high-density Q-band SATCOM phased-arrays, while achieving deep power back-off efficiency enhancement. It achieves an average output power (P_{avg}) of 14 dBm and an average PAE of 13.2% under a single-carrier 100 MHz 64-QAM modulation signal, and supports 400MHz/100MHz 64QAM/256QAM signals.**

***Keywords*— Doherty PA, mm-Wave, Compact, Power-Added Efficiency (PAE).**

I. Introduction

Next-generation LEO SATCOM systems are increasingly targeting the Q/V-band due to its larger capacity compared to Ku/Ka-band, ideal for internet feeder links and the emerging Orbital Data Centers (ODCs) processing high-demand AI applications in orbit [1]. However, realizing these networks presents several RF front-end hardware challenges. The shorter wavelength in the Q-band dictate highly compact phased array antennas with strict area constraints on the RF front-end. Furthermore, complex modulation schemes with high Peak-to-Average Power Ratios (PAPR) force power amplifiers (PAs) to operate in deep power back-off (PBO) to maintain spectral integrity at the expense of efficiency [2]. Consequently, developing ultra-compact Q-band PAs with deep PBO efficiency enhancement is a fundamental requirement to minimize thermal dissipation and meet the strict power budgets of solar-powered LEO satellites.

The Doherty PA has been presented in literature as one of the most prominent power back-off (PBO) efficiency enhancement techniques as it provides a great balance between efficiency, area, and bandwidth [3]. Furthermore, deep PBO efficiency enhancement Doherty PAs have been presented in [4], [5]. However, a common drawback of these implementations is the large silicon area, which is incompatible with compact antenna spacing in Q-band arrays. On the other hand, multiple techniques have been recently proposed in literature for compact single-transformer two-way Doherty PAs [6], [7], [8]. However, these implementations are limited to -6 dB PBO efficiency enhancement and doesn't efficiently handle higher PAPR signals. Thus, this work demonstrates a highly compact 3-way series Doherty PA for deep PBO efficiency enhancement, illustrating a systematic technique to reduce silicon area. The reported PA has the smallest core chip area (more-than 6x smaller) and the highest power density (more-than 6x higher) compared to all the reported CMOS PAs with PBO efficiency enhancement in the Q-band.

II. Proposed Doherty Power Amplifier

A. Proposed 3-way Series Doherty PA Top-Level Schematic

Fig. 1 illustrates the proposed symmetric 3-way Series Doherty PA implementation. it consists of a compact input power division network, followed by the proper phase compensation to achieve correct Doherty load modulation at the output. Furthermore, two-stage PAs are identically used as the main and auxiliary PAs, each auxiliary PA with their respective adaptive biasing circuits, which turn the PAs on at their respective PBO levels controlling their peaking Class-C operation. Finally, a compact 3-way Series Doherty Output Network (SDON) that combines the three PAs output powers as well as providing the Doherty load modulation to achieve the deep PBO efficiency enhancement.

B. Proposed 3-way Series Doherty Output Network

1) Ultra-Compact Doherty PA Design

The area reduction technique applied to the output matching network is summarized in Fig. 3. The proposed technique starts with the conventional 3-way SDON. As shown in Step I in Fig. 3, a transformer-based impedance inverting network as presented in [6] follows. Considering the transformer model presented in [9], along with two shunt capacitors at the primary and secondary sides. As shown in Fig. 2, a qualitative analysis follows: The output capacitor C_s can be referred to the primary side of the ideal transformer. Based on the CLC pi-network lumped-model of the quarter-wave section, we may deduce the following conditions:

$$\omega_o(1-K^2)L_p = Z_o \tag{1}$$

$$\omega_o C_p = \omega_o C_s(\frac{n}{K})^2 - \frac{1}{\omega_o K^2 L_p} = \frac{1}{Z_o}, \tag{2}$$

Where, Z_o is the characteristic impedance of the quarter-wave section, n is the transformer turns ratio, K is the transformer coupling factor, and L_p is the transformer primary self-inductance. Thus, Eq. 3 follows:

$$\omega_o C_s(\frac{n}{K})^2 - \frac{1}{\omega_o K^2 L_p} = -\frac{1}{\omega_o(1-K^2)L_p}, \tag{3}$$

Which sets an upper limit on the coupling factor ($K < 1/\sqrt{2}$) in order to have positive values for ω_o, C_s, L_p,

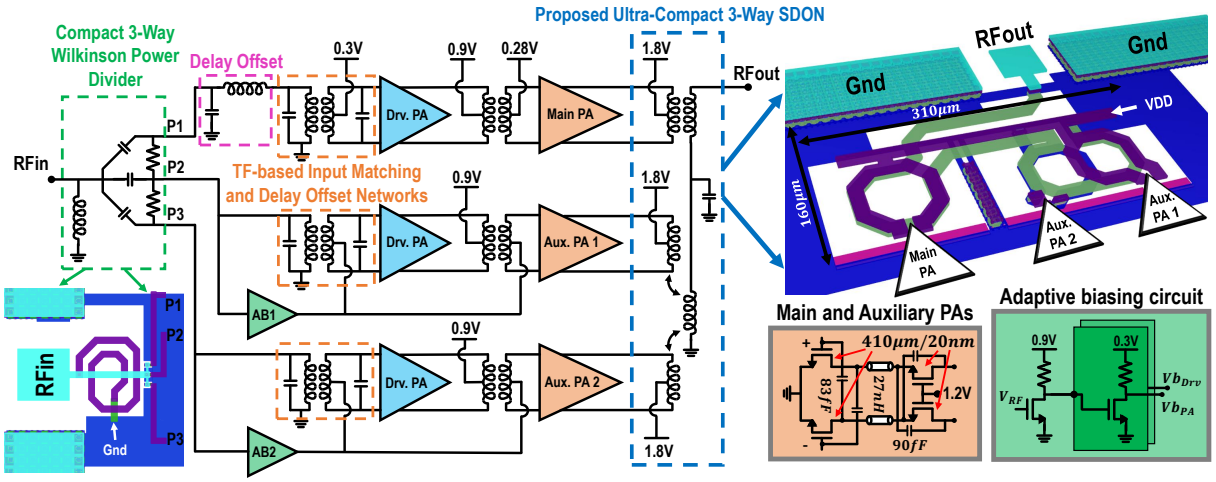

Fig. 1. Top-level schematic of the proposed compact 3-way series Doherty power amplifier.

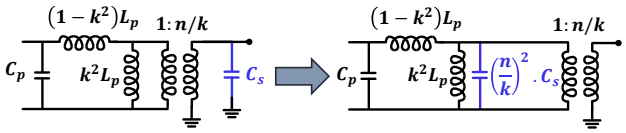

Fig. 2. A qualitative analysis of the transformer-based impedance inverting network.

and n. Furthermore, the secondary shunt cap C_s is also lumped into the secondary inductance of the transformer. As shown in Step II in Fig. 3, an equivalent circuit model of the impedance-inverting network is obtained by equating the Impedance-matrices of both networks, as shown in Eq. 4 and 5.

$$\mathbf{Z_{IIN}} = \begin{bmatrix} j\omega_o L_p \frac{1-\omega_o^2 L_s C_s (1-K^2)}{1-\omega_o^2 L_s C_s} & \frac{j\omega_o M}{1-\omega_o^2 L_s C_s} \\ \frac{j\omega_o M}{1-\omega_o^2 L_s C_s} & \frac{j\omega_o L_s}{1-\omega_o^2 L_s C_s} \end{bmatrix} \quad (4)$$

$$\mathbf{Z_{IIN}}|_{eq.} = \begin{bmatrix} j\omega_o L_p' & j\omega_o M' \\ j\omega_o M' & j\omega_o L_s' \end{bmatrix} \quad (5)$$

This equivalent network is more narrowband due to the removal of the frequency dependence of C_s. In addition to that, the equivalent network is only valid up to a certain frequency, set by the following condition: $\omega < 1/(\sqrt{L_s C_s})$, which needs to be made higher than the frequency of operation. Thus, as shown in Step III in Fig. 3, the two auxiliary transformers are unified into a 3-coil transformer with minimal coupling between the two primary sides. Finally, based on the aforementioned transformer-based impedance inverting network, as shown in Fig. 2. The 3-coil transformer is also used as an impedance inverting network by adding primary and secondary shunt capacitances and lowering the coupling factors, as shown in Step IV in Fig. 3. The aforementioned area reduction technique can potentially be scaled to an N-way series Doherty output network.

2) *Achieving Low Transformer Coupling-Factor*

As shown in Fig. 4, The proposed 3-coil transformer implementation addresses two key design constraints: the placement of the two auxiliary PAs, and minimizing the coupling between the two primary inductors. The latter is achieved by proper placement and excitation. As shown in Fig. 4, the overlapping distance of the primary inductors is chosen to minimize the coupling factor while allowing the placement of the two auxiliary PAs.

C. *Proposed Doherty PA Input Network*

The proposed 3-way Doherty input network is required to provide equal power splitting and appropriate phase alignment within a compact footprint. To achieve this, a compact 3-way Wilkinson power divider is employed using the quarter-wave LCL pi-network lumped-model, allowing the parallel input shunt inductors to be merged into a single smaller inductor, and enabling the removal of the output shunt inductors for further area reduction, as shown in Fig. 1. Although this introduces symmetric mismatch loss, the equal-split and phase alignment are preserved. Additional phase alignment is realized in a compact fashion through the proposed transformer-based input matching networks, which achieves proper matching with different phase offsets, as illustrated in Fig. 1.

III. Measurement Results

The proposed 3-way Doherty PA is fabricated in the 22-nm CMOS FD-SOI technology, with a compact core area of 455 μm x 325 μm (0.148 mm^2), as shown in Fig. 7. Moreover, Fig. 5 presents the measured small-signal performance of the proposed 3-way Doherty PA, and the large-signal performance under a continuous wave (CW) excitation over the targeted frequency range. As shown in Fig. 5(a), the measured input return loss (S_{11}) shows good matching in band (from 27 GHz to 43 GHz), while the proposed Doherty PA exhibits a peak small-signal gain (S_{21}) of 14.3 dB at 37 GHz, with 3-dB

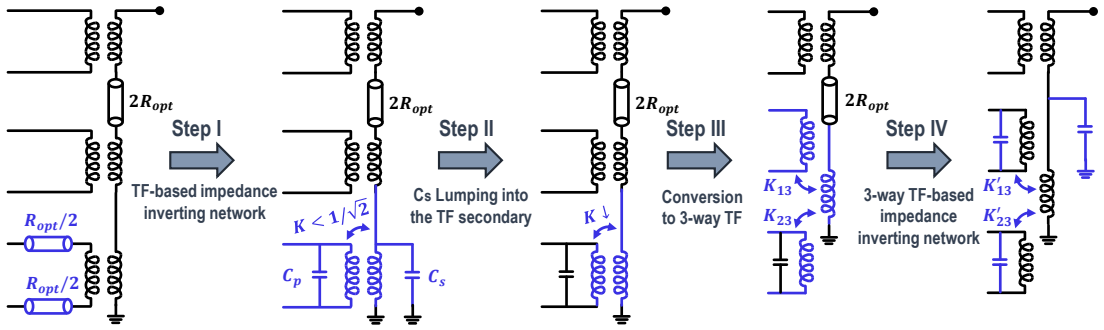

Fig. 3. The area reduction procedure of the proposed compact SDON.

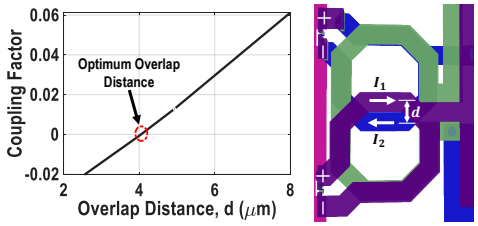

Fig. 4. The 3-way transformer implementation to minimize the mutual coupling between the two primary coils.

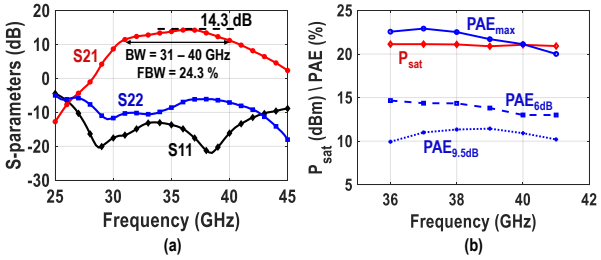

Fig. 5. Measured performance of the proposed PA: (a) small-signal performance, and (b) Large-signal CW characteristics over frequency.

fractional-bandwidth of 24.3%. Under the large-signal CW signal, the proposed Doherty PA exhibits a saturated output power (P_{out}) of 21 dBm, with peak Power-Added Efficiency (PAE) of 23% at 37 GHz, -6 dB PBO PAE of 14.4% at 38 GHz, and -9.5 dB PBO PAE of 11.4% at 39 GHz. Additionally, Fig. 6 illustrates the large-signal CW performance at 38 and 39 GHz, clearly showing the 3-way Doherty PBO efficiency enhancement.

Furthermore, the proposed Doherty PA is measured under 64-QAM (PAPR $\approx$ 6 dB) and 256-QAM (PAPR $\approx$ 8 dB) modulation signals, achieving P_{avg} of 14 dBm and PAE_{avg} of 13.2% under a single-carrier 100 MHz 64-QAM signal, while maintaining EVM of -24.3 dB. Moreover, the proposed Doherty PA is also measured under a 400 MHz 64-QAM signal and a 100 MHz 256-QAM signal, as shown in Fig. 8.

Table 1 summarizes the measured performance of the state-of-the-art mm-Wave CMOS PAs employing PBO efficiency enhancement at similar frequency. Compared to

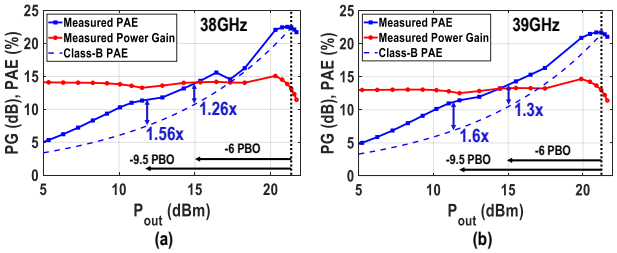

Fig. 6. Measured large-signal CW performance at (a) 38 GHz, and (b) 39 GHz.

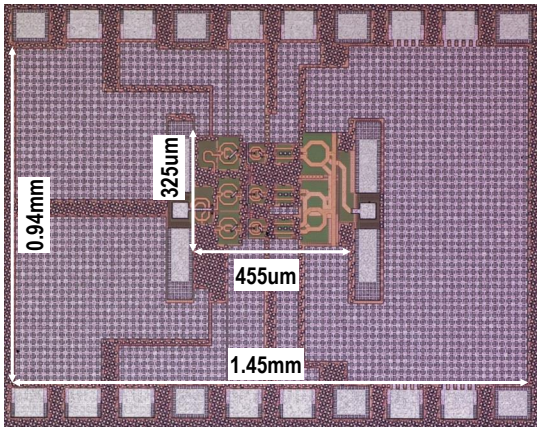

Fig. 7. Chip micro-photograph of the 3-way Doherty PA (core area: 0.148 mm^2) fabricated in a 22-nm CMOS FD-SOI process.

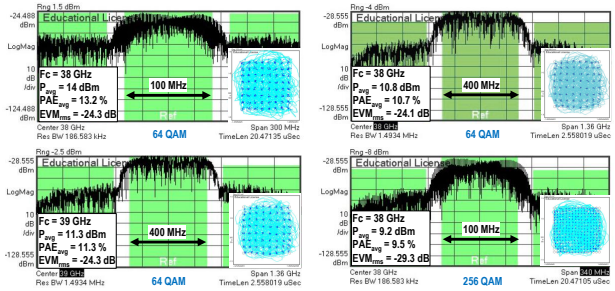

Fig. 8. Modulation measurement results.

Table 1. Performance Comparison with the State-of-the-Art Q-Band CMOS PAs with PBO Efficiency Enhancement

	This work			X. Zhang, JSSC '23 [5]	E. Liu, JSSC '23 [10]	H. Yu, IMS '23 [11]	N. Mannem, JSSC '20 [12]		V. Qunaj, JSSC '21 [13]		L. Chen, JETCAS '24 [14]
Architecture	**Transformer-based 3-way Series Doherty**			Coupled-inductor-based 3-way Doherty PA	Coupler-based Parallel-Series Doherty PA	Enhanced linearity 2-way Doherty	Coupler-based Reconfigurable Series/Parallel Doherty		Doherty-like LMBA		Doherty-like unequal power-split LMBA
Frequency (GHz)	**38**			38	38	37 – 43	39		36		39
Technology	**22nm CMOS SOI**			45nm CMOS SOI	45nm CMOS SOI	45nm CMOS SOI	45nm CMOS SOI		28nm CMOS		45nm CMOS SOI
Supply (V)	**1.8**			1.8	2	2.4	2		1		1.2
Gain (dB)	**14**			15	12.4	15	12.2*		18		12.8
P_{sat} (dBm)	**21**			18.9	22.9	21.5	20.8		22.6		22.1
OP1dB (dB)	**19**			18.4	22.7	20.5	20.2		19.6		17*
PAE_{max} (%)	**22.5**			23.3	26.8	30	33.3		32		25.7
PAE @ -6dB (%)	**14.3**			17.1	21.9	19	22.3*		18.8*		19
PAE @ -9.5dB (%)	**11.3**			13.7	16.4*	10.8*	14*		10.7*		12.2*
Core area (mm^2)	**0.148**			1.4	2.91	0.91	1.18		1.44		1.56
PD‡ (mW/mm^2)	**954.4**			55.4	67	155.2	101.9		126.4		104
Modulation	**64-QAM**		**256-QAM**	5G NR 1-CC 64-QAM OFDM	5G NR 1-CC 64-QAM OFDM	64-QAM	64-QAM		64-QAM		64-QAM
BW (MHz)	**100M**	**400M**	**100M**	100	100	100	100	500	2000	3000	200
EVM (dB)	**-24.3**	**-24.1**	**-29.3**	-25	-25.1	-25.2	-23.6	-22.9	-25	-25.1	-22.5
P_{avg} (dBm)	**14**	**10.8**	**9.2**	11.3	16.7	15.3	13.8	12.2	16	15.5	13.1
PAE_{avg} (%)	**13.2**	**10.7**	**9.5**	14.7	22.6	18.6	19	16.1	22	20	14.4

*Graphically estimated ‡Power Density = Psat (mW) / Core Area (mm^2)

the state-of-the-art, the proposed 3-way Doherty PA achieves competitive performance under different modulation scenarios, in an ultra-compact area (more-than 6x smaller), and an exceptional power density (more-than 6x higher) among CMOS PBO-enhanced PAs in the targeted Q-band frequency.

IV. Conclusion

This paper presents an ultra-compact 3-way series Doherty PA, implemented in the 22-nm FD-SOI CMOS technology. A systematic area reduction methodology is presented, highlighting the design-space limitations. The proposed design achieves saturated output power (P_{sat}) of 21 dBm at 38 GHz, with 22.5% peak PAE, and PAE of 14.3% and 11.3% at -6 dB and -9.5 dB PBO respectively. Resulting in an average output power (P_{avg}) of 14 dBm and an average PAE of 13.2% under a single-carrier 100 MHz 64-QAM modulation signal. The PA also supports 400MHz/100MHz 64QAM/256QAM signals. This is achieved in the smallest die area reported for a multi-way Doherty PA.

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