A 9.7mW 70.3dB-SNDR 100MHz-BW CT ΔΣ Modulator with 1ps$_{rms}$-Jitter Tolerance Using Evolved-Direct-Charge-Dump Feedback with Efficient Positive-Feedback Charger

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***Abstract*—This work evolves the prior direct-charge-dump feedback to extend bandwidth of a CT ΔΣ modulator and reduce reference buffer power, while preserving its merits. To fast charge the feedback capacitor power-efficiently, a positive-feedback charger is proposed: stimulated by the positive feedback, charging current circulates locally with the assistance of the local decoupling capacitor, significantly reducing the reference buffer power. Without linearity calibration, the prototype achieves 70.3dB SNDR in 100MHz bandwidth, and consumes 9.7mW including reference buffer power, leading to 170.4dB Schreier FoM, which is comparable to the state-of-the-arts. The measured SNDR drop is only 0.6dB at band edge when suffering from 1ps$_{rms}$ jitter.**

***Index Terms*—Wideband CT ΔΣ modulator, evolved-direct-charge-dump feedback, positive-feedback charger, reference buffer, power efficiency, jitter-insensitivity, anti-aliasing**

I. Introduction

CT ΔΣ modulators (CTDSMs) prevail in communication systems due to their resistive input and inherent anti-aliasing. However, CTDSMs with resistive/current/switched-capacitor feedback are either jitter-sensitive or imposing stringent linearity requirement on the 1st OTA, OTA1. And propagating low-jitter clock is power hungry [1]. Alternatively, a direct-charge-dump feedback (DCD FB), which implements feedback by charge sharing without OTA1 involvement (Fig. 1, top), is jitter-insensitive and significantly alleviates linearity requirement on OTA1 [2]. However, it is dedicated to a 1b quantizer (QTZ), constraining bandwidth (BW) from extending. Furthermore, high sampling rate helps for BW extension, but charging the feedback capacitor C_{fb} at GHz is power hungry. Hence, in prior works, jitter-insensitivity, wideband (≥80MHz) and high power efficiency are barely achieved simultaneously. This work evolves prior DCD FB in a CTDSM to accommodate an arbitrary-bit QTZ and a novel power-efficient charging technique, in order to extend BW power-efficiently while remaining jitter-insensitive and low linearity-requirement for OTA1.

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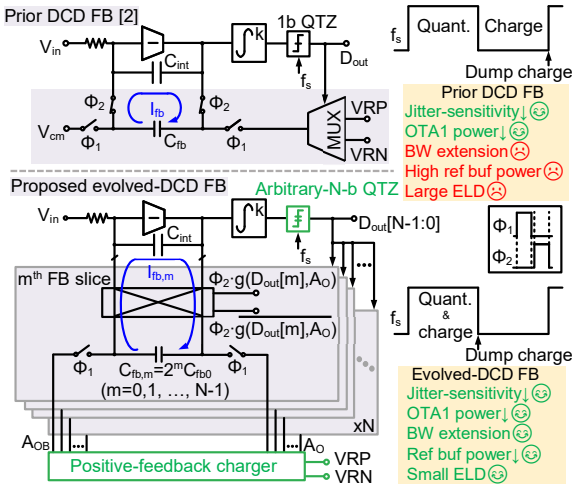

Fig. 1. Prior DCD FB (top) and the proposed evolved-DCD FB with the proposed positive-feedback charger (bottom).

II. Evolved-DCD FB with Positive-Feedback Charger

As shown in the bottom of Fig. 1, for an arbitrary-N-bit QTZ, the proposed evolved-DCD (E-DCD) FB consists of N FB slices and a shared positive-feedback charger (PFC); each FB slice consists of a weighted $C_{fb,m}$ corresponding to the mth bit of QTZ output, and control switches; as shown in Fig. 2, the PFC consists of two back-to-back inverters supplied by reference voltages VRP and VRN which are provided by a reference buffer. As shown in Fig. 1, bottom and Fig. 2, during charging phase, the N sets of $C_{fb,m}$ are connected between the input/output of the inverters, and the positive feedback rapidly brings the voltage across the capacitors to VRP-VRN; upon finishing charging, the N sets of $C_{fb,m}$ dump weighted amounts of charge to the loop filter by shorting themselves with the integrating capacitor C_{int} of the 1st integrator, fulfilling the feedback by charge sharing without the participation of OTA1. As illustrated by the timing diagram in the top-right of Fig. 1, in the prior DCD FB, C_{fb} won't get charged until the QTZ decision is ready, hence an extra dedicated time, half a sampling period $0.5/f_s$, has to be assigned to capacitor charging. In the E-DCD FB, instead of waiting for QTZ

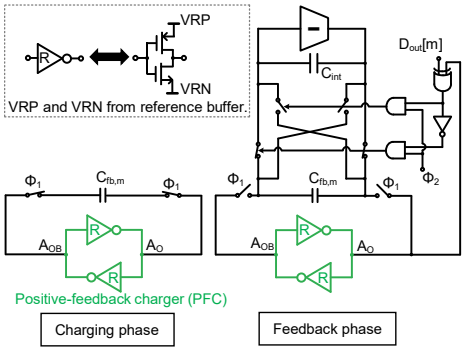

Fig. 2. Working procedure of the proposed E-DCD FB for the m[th] bit.

decision, $C_{fb,m}$s are charged while QTZ making decision; once the QTZ decision is ready, $C_{fb,m}$s are immediately shorted with C_{int} to dump charge to the loop filter, and the connection polarities are determined by the QTZ output together with the final state of the PFC. Hence, the excess-loop delay (ELD) is $0.5/f_s$ less than that in the prior DCD FB, beneficial to loop stability; and there is no need to reset the PFC.

The speed advantage of the PFC is illustrated in Fig. 3. Without reset, the PFC output could be at any potential when the charging starts. Since it takes longest if it starts around the middle of VRP-VRN, we explain the speed advantage with this worst case: initially, each inverter works as an amplifier with voltage gain of A_V, and a strong positive feedback rapidly enlarges the voltage across $C_{fb,m}$ until one transistor in the inverters enters triode region. Then the PFC gradually degenerates to the reference buffer which provides VRP/VRN with a weak positive feedback, working to enhance charging accuracy; the weak positive feedback mainly originates from the V_{GS}-dependent resistance of the triode-region transistors. When the reference buffer in the PFC and the scenario directly using a regular reference buffer consume the same power for 1% settling accuracy, the proposed PFC only requires 1/3 of the time required when directly using a regular reference buffer (Fig. 3, right). The speed advantage is mainly because the strong positive feedback already charges the capacitor to 81% of its final voltage before the PFC degenerates to a regular reference buffer with a weak positive feedback.

The high power efficiency of the PFC is ascribable to the locally charge recycling stimulated by positive feedback. Due to positive feedback, the two inverters' outputs change inversely, so do their corresponding supply rails, if neglecting the delay (at the order of ps). Hence, a local decap, C_{dec}, is introduced between VRP and VRN to self-contain the supply ripple (Fig. 4, top-left). Furthermore, with the assistance of C_{dec}, the majority of charge demanded by the PFC from VRP/VRN is recycled locally, which is stimulated by positive feedback. The reference buffer (Fig. 4, top-right) is to set the voltage potential and compensate charge loss; it doesn't supply instantaneous current at sampling rate (Fig. 4, bottom), thus its power is significantly reduced. For comparison, a regular reference buffer and a sole decap are used to charge

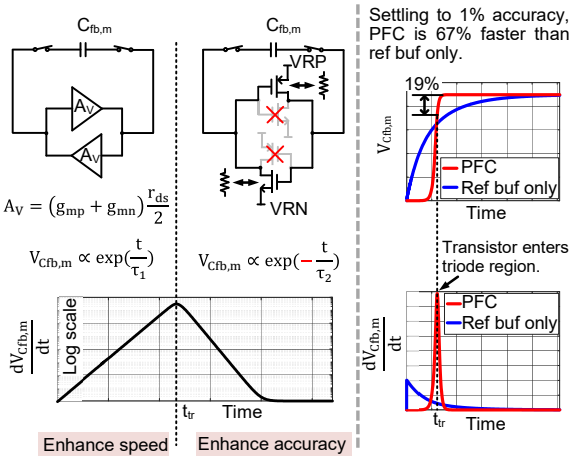

Fig. 3. Working procedure of the PFC (left), and charging speed comparison between PFC and directly using a reference buffer when both consume the same power for settling to the same accuracy (right).

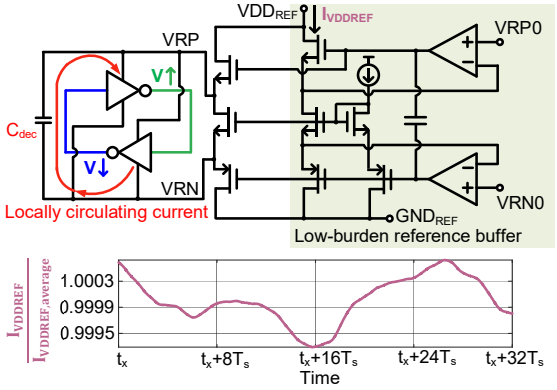

Fig. 4. Charge recycling locally in the PFC (top), and simulated reference buffer supply current when charging 160fF capacitor at rate $1/T_s$ (bottom).

the same capacitor, respectively; to achieve the same settling accuracy in the same duration under the same bonding wire model, the power and decap size required are shown in Fig. 5. Compared with the regular reference buffer, the power of the PFC is reduced by 74%, while the required decap size is only increased by 150%. If solely using a decap, the decap size has to be 20 times larger than that with the PFC.

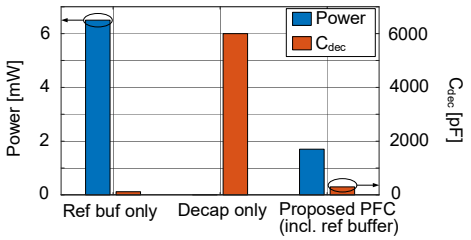

Fig. 5. Power & decap size comparison among different charging techniques.

III. CTDSM Implementation

To validate the BW-extending capability of the E-DCD FB, and the high power efficiency of the PFC, a 1.5b, 4[th] order

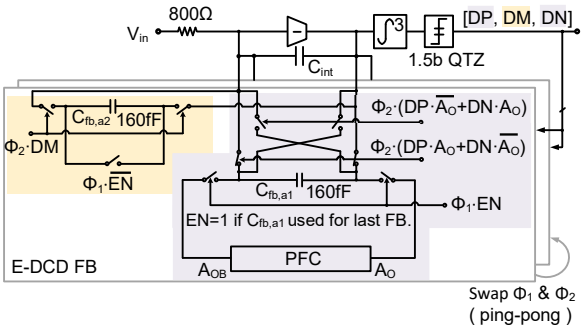

Fig. 6. Implementation of the 1.5b E-DCD FB with PFC.

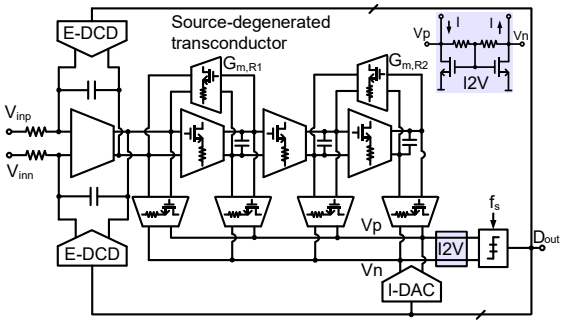

Fig. 7. Architecture of the 1.5b, 4th order CTDSM.

CTDSM clocked at 4GHz is designed, and the implementation of the 1.5b E-DCD FB is shown in Fig. 6. The proposed PFC is applied to charge $C_{fb,a1}$, which feeds back the high-level and low-level QTZ output DP and DN; and $C_{fb,a2}$, nominally identical to $C_{fb,a1}$, feeds back the medium-level QTZ output DM. "Charging" $C_{fb,a2}$ is shorting its two plates. Either $C_{fb,a1}$ or $C_{fb,a2}$ being "charged" in the charging phase depends on which of them is used in the last clock cycle, and such information is logged by signal EN. Monte Carlo simulation shows that capacitor mismatch in this 1.5b FB barely affects the target performance; hence no calibration is applied for capacitor mismatch. To save area, the decap of the PFC is implemented by placing MOSFET underneath MOM cap to utilize gate capacitor increasing capacitance density. To prevent switching at the loop filter's early stage from degrading the aliasing rejection, ping-pong operation is used [2]. The CTDSM architecture is in Fig. 7: the 1st integrator is an active RC integrator for linearity, and the rest are G_m-C integrators for speed. Feedforward compensation is implemented to maintain the modulator stability, which is implemented by source-degenerated transconductors. Two resonators are formed with auxiliary $G_{m,R1}$ and $G_{m,R2}$ which absorb the equivalent transconductance of the 1st and 3rd integrator respectively. ELD compensation is done by including the current-steering DAC (*i.e.*, I-DAC in Fig. 7) together with tuning the feedforward coefficients.

IV. Measurement Results

The prototype is fabricated in a 28nm CMOS process, taking 0.025mm^2 (Fig. 13, left). R/C variation is foreground-calibrated. In 100MHz BW, the measured SNDR and SFDR are 70.3dB and 84.1dBc, respectively. The measured SNDRs for different input amplitudes and input frequencies are illustrated in Fig. 9, indicating a DR of 72.6dB and HD3 as the SFDR limiter. To evaluate the jitter-sensitivity of the design, phase modulation is used to generate jittery clock, and spectrum analyzer is used to evaluate the jitter rms value of the artificial jittery clock. The measured SNDRs at band edge 99.6MHz for various jitter values are illustrated in Fig. 10: with 1ps$_{rms}$ jitter, the SNDR drop is only 0.6dB, 11.2dB less than that with a non-return-to-zero(NRZ) FB. The measured STF magnitude given in Fig. 11 verifies the alias-rejection of the design even though there are switching behaviors at the loop filter's early stage. Four chips are measured with 10% variation applied on the reference buffer supply and the measurement results are plotted in Fig. 12: for the same chip, the SNDR variation is less than 0.49dB, validating the robustness of the PFC against reference buffer supply variation. And this is because that the charging accuracy of the PFC is determined in the duration when the PFC degenerates to a regular reference buffer (c.f. Fig. 3), which possesses a high PSRR. The CTDSM consumes 9.7mW, including reference buffer (Fig. 13, right).

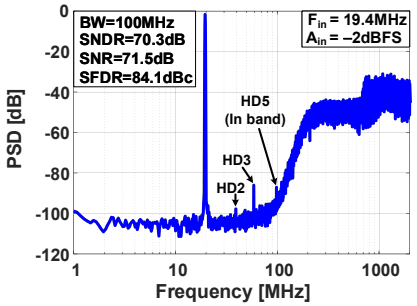

Fig. 8. Measured output spectrum (41k-point FFT; Blackman window).

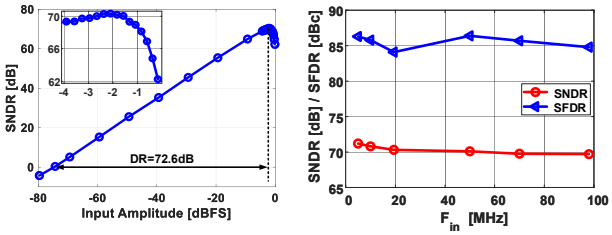

Fig. 9. Measured SNDR versus input amplitude (left) and versus input frequency (right).

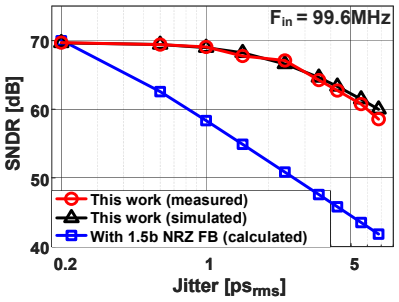

Fig. 10. Measured & simulated jitter-sensitivity at band edge and calculated jitter-sensitivity of a CTDSM with a NRZ FB.

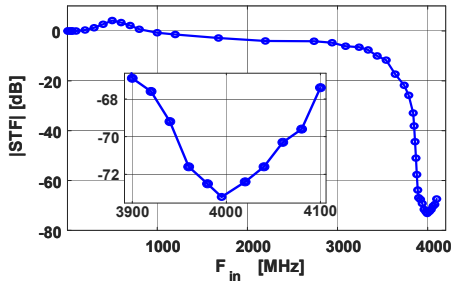

Fig. 11. Measured STF magnitude (20-time average for each point).

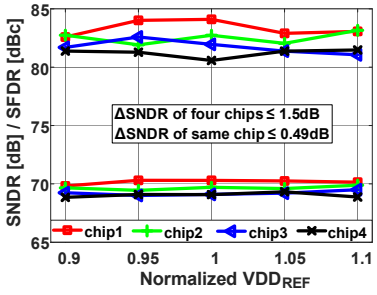

Fig. 12. Four-chip measurement results with 10% reference buffer supply variation (with identical R/C-variation calibration code).

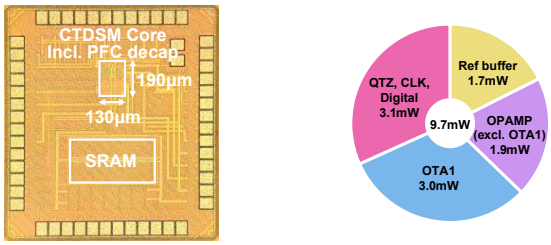

Fig. 13. Chip microphotograph (left) and measured power breakdown (right).

V. Conclusions

Direct-charge-dump feedback in CTDSMs is evolved to extend bandwidth and reduce reference buffer power while preserving its jitter-insensitivity and low linearity-requirement for OTA1. The reduction of the reference buffer power is achieved by the proposed positive-feedback charger. A prototype employing these proposed techniques is designed and measured; its performance, which is summarized and compared with the state-of-the-art (SotA) CTDSMs in TABLE I, validates the effectiveness of the proposed techniques: this design's BW is approaching the SotA of single-loop CTDSMs with SotA power efficiency while being jitter-insensitive, which is normally not reflected by the modulator FoM. Although the positive-feedback charger demands larger decap than directly using a regular reference buffer, the modulator area increase is mild. The power efficiency-BW relation of the SotA CTDSMs in Fig. 14 reveals: compared with the prior jitter-insensitive CTDSMs, this design's BW is 2.5× extended, while achieving SotA power efficiency and being jitter-insensitive.

TABLE I. Performance summary and comparison with state-of-the-art single-loop CTDSMs with BW≥50MHz.

	This work	ISSCC 18 He	ISSCC 19 Wang	JSSC 20 Wang	VLSI 25 Javvaji	ISSCC 22 Bolatkale
Feedback scheme	E-DCD	NRZ	NRZ	NRZ	RO	RZ
QTZ bits	1.5	4	6	4	2	2
Jitter sensitivity	Low	Moderate	Moderate	Moderate	High	High
Linearity cal. free?	Yes	No	No	No	No	No
Process [nm]	28	28	28	28	28	28
Area [mm²]	0.025	0.250	0.06	0.019	0.1	0.130
Power [mW]	9.7**	64.3	7.33	17.7	49.5	108.8
F_s [GHz]	4	2.0	0.96	2	4	6.0
SFDR [dBc]	84.1	95	80*	83.6	101.7	114
BW [MHz]	100	50	80	100	100	120
SNDR [dB]	70.3	79.8	64.9	72.6	74.5	71.5
FoM_s [dB]	170.4	168.7	165.3	170.1	167.6	162.0
FoM_w [fJ/con-step]	18.1	80.5	31.9	25.4	57	147.6

FoM_s=SNDR+10*log10(BW/P) FoM_w=P/(2*BW*2^((SNDR-1.76)/6.02))

*Estimated from spectra **Including reference buffer power

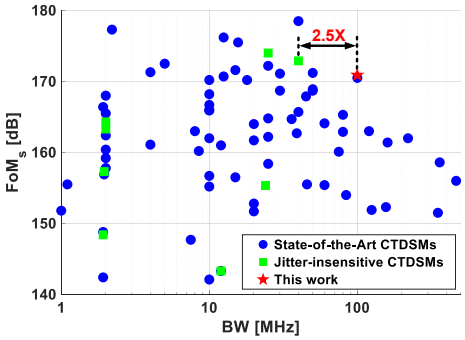

Fig. 14. Power efficiency-BW relation of the state-of-the-art CTDSMs with BW≥1MHz.

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