Aggressive Area Scaling and Superior Performance of Staggered CFET with Novel Segmented Staggered Architecture

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***Abstract*—In this work, a staggered complementary FET (SCFET) with an innovative process flow, integrating bipolar staggered SD and split gate (SG) structure, is proposed. It results in a 20.6% reduction in RO power at iso-frequency compared to CFET. This SCFET enables the implementation of segmented staggered (SS) architecture (SSCFET), effectively isolating adjacent transistors without single diffusion break (SDB) structure, thereby driving aggressive standard cell scaling. Thanks to these above innovations, a novel SRAM layout design of SSCFET is presented, which achieves a 42.3% area reduction compared to CFET and significant enhancements in overall SRAM performance.**

Keywords—complementary FET (CFET), staggered CFET, segmented staggered architecture, area scaling.

I. Introduction

CFET with vertically stacked nFET and pFET [1, 2], as well as backside power delivery network (BSPDN) technology, provides a promising pathway for the continuous scaling of advanced logic devices [3]. However, this complex vertical stacking architecture introduces severe interconnect routing challenges and signal access conflicts, as shown in Fig. 1(b) [4]. To address these interconnect challenges, the staggered CFET (SCFET) has been proposed, achieving striking channel width and scalability potential (Fig. 1(a) and (c)) [5, 6]. Furthermore, the isolation between adjacent transistors poses another critical bottleneck hindering further dimensional scaling. To mitigate this, the single diffusion break (SDB) structure has been introduced [7]. By replacing the dummy gate between adjacent transistors with dielectric, the SDB achieves effective isolation and maximizes spatial utilization. Nevertheless, it still inevitably incurs an area waste.

In this work, we introduce several critical innovations to achieve aggressive area scaling and superior performance. First, we propose a novel process flow integrating bipolar staggered SD and SG for SCFET. Second, segmented staggered (SS) architecture is introduced to form SSCFET to address the space waste issue of SDB. Third, leveraging these innovations, we propose a novel 6T-SRAM design to optimize both the bitcell layout and array-level routing. Finally, design technology co-optimization (DTCO) is employed to conduct a comprehensive power-performance-area (PPA) analysis of the SRAM array for CFET and SSCFET.

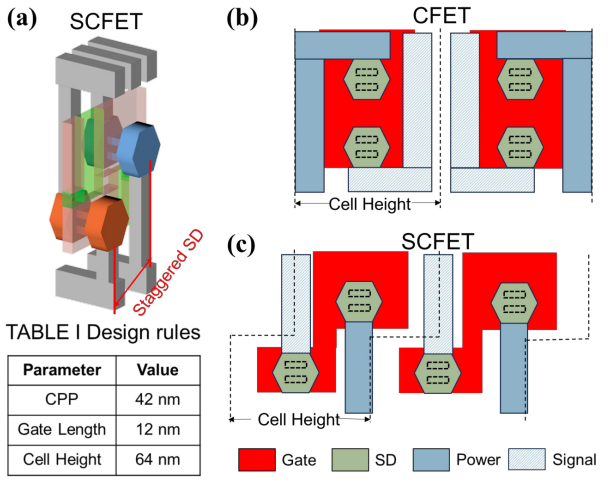

TABLE I Design rules

Parameter	Value
CPP	42 nm
Gate Length	12 nm
Cell Height	64 nm

Fig. 1. Process flow of SCFET. (a) 3D structure of SCFET. Power and signal interconnect design of (b) CFET and (c) SCFET.

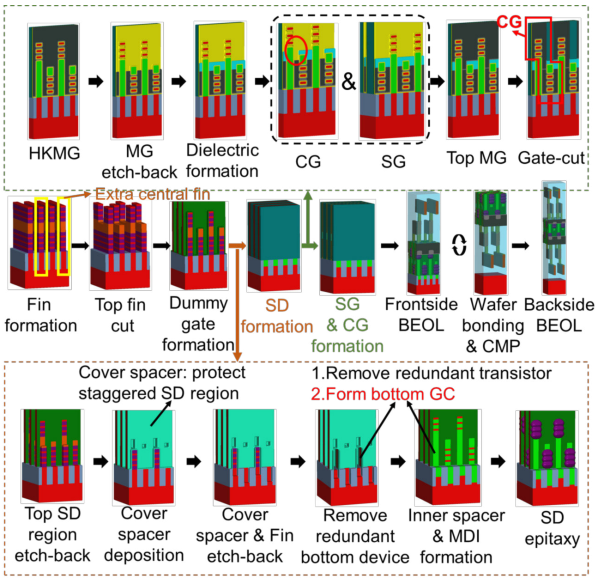

Fig. 2. Process flow of SCFET.

II. Process Flow and Parasitic Analysis of SCFET

A. Process flow

This novel process flow of SCFET is compatible with CFET, as shown in Fig. 2. Different from CFET, the fin formation process requires the addition of the extra central

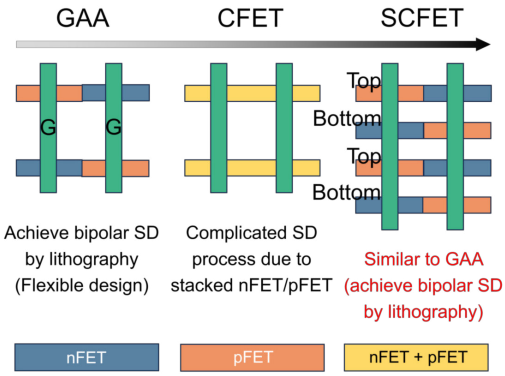

Fig. 3. From a top-down perspective, benefited from staggered SD, SCFET exhibits a layout similar to GAA.

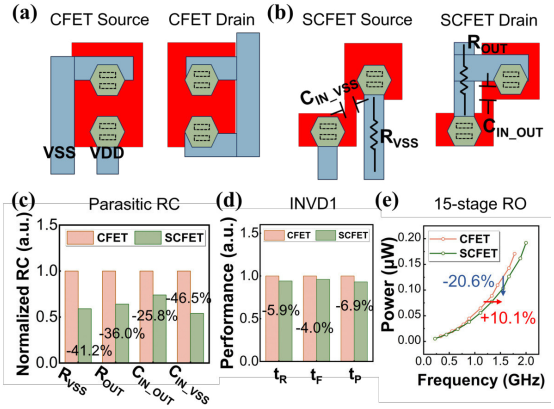

Fig. 4. The INVD1 interconnect design of (a) CFET and (b) SCFET. (c) The key parasitic RC for INVD1. (d) The rise time (tR), fall time (tF) and propagation delay (tP) values of CFET and SCFET INVD1. (d) Power-frequency curves of 15-stage RO with a fan-out of 2.

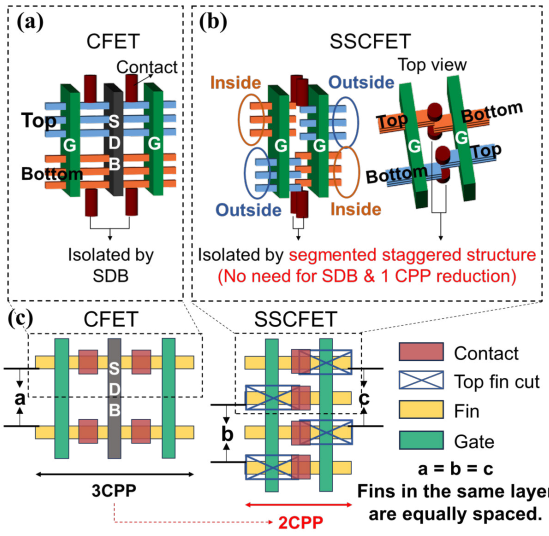

Fig. 5. (a) SDB is required for adjacent transistors isolation in CFET. (b) Schematic of the SS architecture for SSCFET.

fin, followed by top fin cut process to form staggered SD. A different SD module is employed, where the top SD region is etched and a cover spacer is deposited to protect the staggered SD region during the removal of the redundant fin. Subsequently, the MDI, inner spacer, and bottom gate-cut (GC) are formed simultaneously via dielectric fill and etch-back, followed by SD epitaxy. It is observed that although

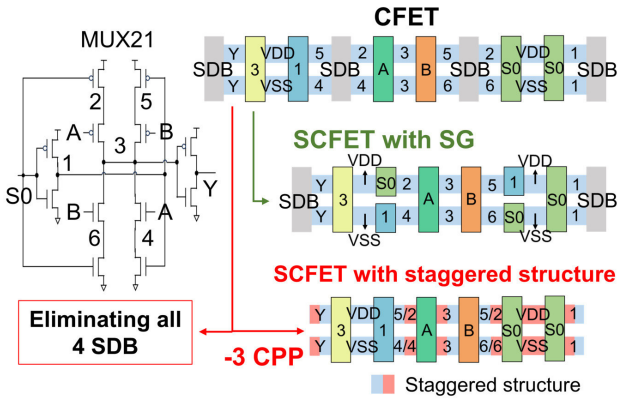

Fig. 6. Schematic of the MUX21 circuit and 3 designs for CFET and SSCFET.

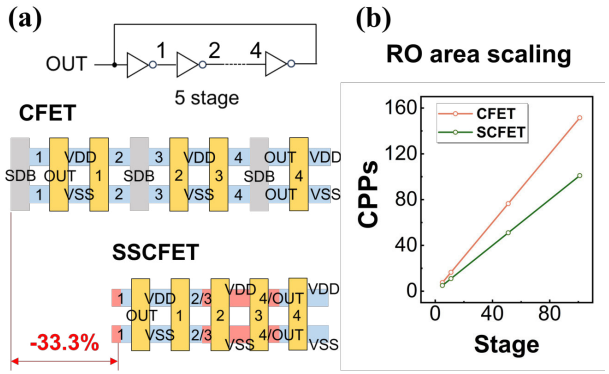

Fig. 7. (a) Schematic of the 5-stage RO circuit and 2 designs for CFET and SSCFET. (b) CPP vs. stage curves for CFET and SSCFET.

the fin pitch is reduced during the fin formation process, within each tier, it could remain consistent with CFET after the SD module. Notably, each tier of SCFET can achieve the bipolar SD, which is like GAA, rather than the vertical nFET/pFET stacking of CFET, as shown in Fig. 3. Therefore, SCFET enables a simplified implementation of bipolar SD compared to CFET. In addition, its gate module remains consistent with SG CFET [8].

B. Parasitic Analysis

The introduction of the staggered SD architecture optimizes the interconnect design by alleviating vertical obstruction, which significantly reduces routing complexity as shown in Fig. 4(a)-(b). All simulations in this study adhere to identical design rules (TABLE I), including a consistent fin pitch within each tier, to ensure a fair comparison. The DTCO framework employed in this study is based on our previous works [6, 9]. By extracting the main parasitic RC components of the INVD1 cell, the structural advantages of the SCFET become obvious. As shown in Fig. 4(c), the SCFET achieves significant reductions in both interconnect resistance and parasitic capacitance. Specifically, the interconnect resistances R_{VSS} and R_{OUT} are decreased by 41.2% and 36.0%, respectively. Meanwhile, the parasitic capacitances C_{IN_OUT} and C_{IN_VSS} are reduced by 25.8% and 46.5%. These optimized parasitic components directly contribute to the improvement of the INVD1's transient characteristics. As illustrated in Fig. 4(d), the rise time (t_R), fall time (t_F), and propagation delay (t_P) of the SCFET INVD1 are improved by 5.9%, 4.0%, and 6.9%, respectively,

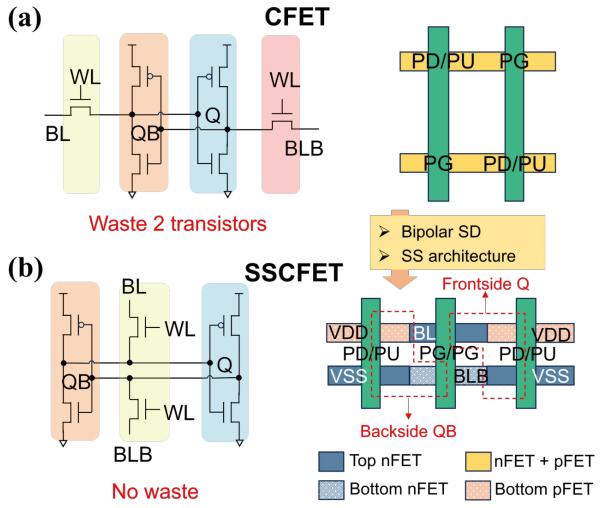

Fig. 8. SRAM layout designs for (a) CFET and (b) SSCFET.

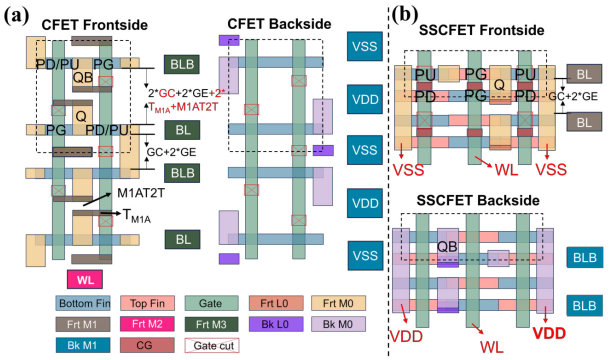

Fig. 9. 1*2 SRAM subarray layouts of (a) CFET and (b) SSCFET.

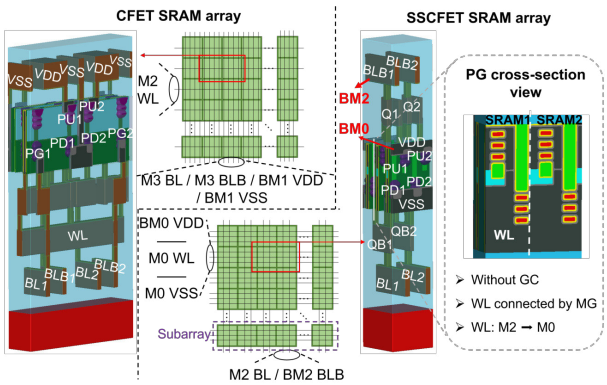

Fig. 10. 1*2 SRAM subarray 3D structures of (a) CFET and (b) SSCFET.

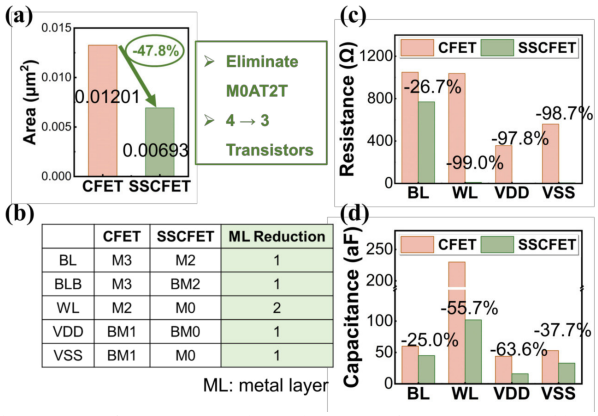

Fig. 11. (a) The area comparison of CFET and SSCFET SRAM bitcell under identical design rules. The SSCFET achieves a breakthrough reduction of 42.3%. (b) ML assignments for the CFET and SSCFET SRAM. (c) Resistance values for BL, WL, VDD, and VSS.

compared to the CFET. To further evaluate the circuit-level performance, a 15-stage INVD1-based ring oscillator (RO) with a fan-out of 2 was simulated. The power-frequency curve in Fig. 4(e) validates the superiority of the SCFET, which demonstrates a 10.1% frequency improvement at iso-power and a 20.6% power reduction at iso-frequency.

III. SSCFET DTCO

A. SS Architecture

To enable aggressive cell area scaling for the SCFET, we introduce a novel SS architecture between adjacent transistors. As illustrated in Fig. 5(c), this configuration is formed following the top fin cut process, while maintaining equal fin spacing (a=b=c) within the same layer. Fig. 5(a) and (b) compare the SDB method with the SS architecture. The SS architecture provides effective electrical isolation simply by staggering adjacent devices in the same tier. This structural optimization eliminates the SDB entirely, resulting in a direct footprint reduction of 1 CPP. This area advantage becomes highly pronounced in complex standard cells. Fig. 6 demonstrates the layout optimization for a MUX21 cell. While the SG SCFET can remove two SDBs, SSCFET enables the complete elimination of all four SDBs, achieving an overall cell width reduction of 3 CPPs for the MUX21 design. A 5-stage RO is also investigated. As depicted in Fig. 7(a), the SSCFET layout shows a significant 33.3% reduction in the total cell area compared to the CFET. Furthermore, the CPP versus stage curves presented in Fig. 7(b) confirm that this area scaling benefit expands linearly as the number of stage increases, highlighting the strong area-efficiency of the SSCFET for future high-density logic application.

B. SRAM Layout Design

In CFET SRAM, the presence of two redundant transistors results in area waste, as shown in Fig. 8(a). To maximize area utilization, by utilizing the bipolar SD and SS architecture, we propose a novel SSCFET SRAM layout design, where all transistors are fully utilized. Fig. 8(b) depicts the proposed SRAM layout of SSCFET. The two n-type PGs are positioned between the PD/PU pairs. Q (QB) and BLB (BL) are routed on the frontside and backside of wafer, respectively. The SRAM layouts show that CFET SRAM needs additional space to isolate Q and QB, as shown in Fig. 9(a). Fortunately, SSCFET successfully addresses this issue, resulting in a substantial reduction in cell height (Fig. 9(b)). Collectively, these advantages enable a 42.3% area reduction for SSCFET SRAM over CFET (Fig. 11(a)). Simultaneously, its advantages are reflected not only in area reduction but also in the reconfigured routing design. From the perspective of SRAM array, for SSCFET, all PGs in every subarray along the gate direction are continuous, allowing WL to be directly connected at MG level (Fig. 10). A similar structural advantage applies to VDD/VSS: all

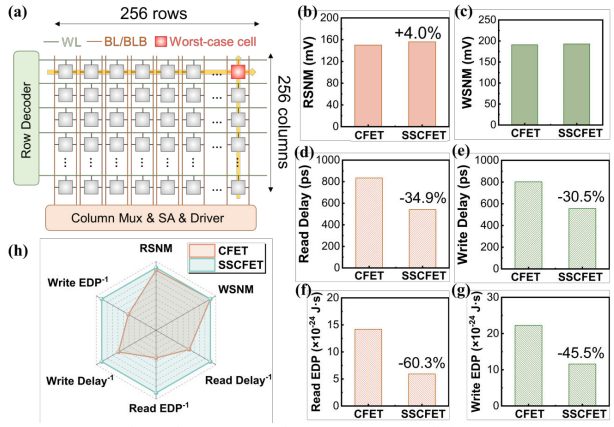

Fig. 12. (a) The schematic of the worse-case cell in 256*256 SRAM array. The (b) RSNM, (c) WSNM, (d) read delay, (e) write delay, (f) read EDP, (g) write EDP comparison between CFET and SSCFET SRAM. (h) Comprehensive performance comparison.

PDs/PUs are adjacent on the frontside/backside of every subarray, facilitating VSS/VDD connections at M0 level. Benefiting from the reduction in metal layer (ML) required for WL, VDD, and VSS, BL and BLB can be routed at M2 level. This architecture shows many benefits. First, the lengths of both power and signal metal lines are significantly reduced, leading to lower parasitic RC. Second, the connections of VDD/VSS/WL at M0 alleviates routing congestion and coupling on M1 and above. Third, despite SSCFET SRAM achieving higher integration density, the track density on ML remains nearly unchanged. The distribution of all power and signal tracks is summarized in Fig. 11(b).

C. SRAM Performance

As a result, significant RC reductions are observed, as shown in Fig. 11(c-d), and the interconnect resistances (R_{WL}, R_{VDD}, and R_{VSS}) are reduced to negligible levels. To evaluate the impact of these reduced parasitics, circuit simulations are conducted on the worst-case cell within a 256 × 256 SRAM array, as shown in Fig. 12(a). Identical nFET and pFET configurations are used for a fair comparison. Fig. 12(b) and (c) present the static performance, where the SSCFET exhibits a 4.0% improvement in read static noise margin (RSNM), but there is a slight degradation in the write margin (WM). Meanwhile, the SSCFET still shows clear advantages in both dynamic speed and overall energy efficiency. Specifically, owing to the optimized interconnect resistances and parasitic capacitances, the read and write delays of the SSCFET SRAM are reduced by 34.9% and 30.5%, respectively, as shown in Fig. 12(d)-(e). These speed improvements, combined with lower dynamic power, lead to much better energy-delay products (EDPs). As shown in Fig. 12(f)-(g), the read and write EDPs are decreased by 60.3% and 45.5%, respectively. Fig. 12(h) summarizes these metrics for comprehensive performance comparison. Overall, the results confirm that the proposed SSCFET architecture provides significant speed and energy efficiency benefits for SRAM compared to the CFET.

IV. Conclusion

In summary, the proposed SSCFET demonstrates significant structural advantages over the CFET. By introducing the bipolar SD and eliminating the SDB, it not only achieves aggressive area scaling for standard cells, but also delivers a 42.3% improvement for SRAM bitcell area. Furthermore, owing to the reduced parasitic RC, the SSCFET significantly improves nearly all critical SRAM performance metrics, including dynamic speed and energy efficiency. These comprehensive device-to-circuit level improvements confirm that the SSCFET exhibits great potential to drive the continued scaling and advancement of high-density logic devices beyond the CFET.

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