A 58.9 µW CMOS Hall Sensor with Asymmetry-Compensated Bipolar HV Duty-Cycled Biasing and SC Offset Cancellation for Low-Power IoT Applications

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***Abstract*— This work presents a magnetic sensor interface using high-voltage (HV) duty-cycled biasing to overcome the noise-power trade-off. To address JFET-induced resistance modulation and common-mode shifts, an asymmetry-compensated bipolar HV converter (ACB-HVC) is proposed, with offset shifting to suppress residual offset. Fabricated in a 180 nm BCD process, the prototype achieves a 10.1× sensitivity gain at 20 V, with a 2.3 µT (3σ) offset and 0.16% nonlinearity. This work demonstrates a 1.4 µT (1σ) resolution and a resolution FoM of 26.4 aJ·T^2 at 58.9 µW, providing a >6.3× resolution FoM improvement and >150× power reduction over the state of the art, enabling low-power IoT applications.**

Keywords—magnetic sensor, Hall plate, JFET effect, high-voltage biasing, duty-cycled, spinning current, offset cancellation, low-power IoT applications

I. Introduction

Magnetic sensing is a versatile modality for energy-constrained IoT nodes, enabling applications such as proximity/position sensing, contactless current monitoring, and e-compasses [1-6]. In CMOS N-well Hall plates, inherent process variation induces tens-of-mT static offsets [1-3] that overwhelm the target µT-level fields. Spinning-current techniques are therefore essential to suppress these offsets and preserve readout dynamic range [7].

Even with spinning, the noise-power trade-off remains a bottleneck for power-constrained IoT nodes. Reducing noise typically demands high bias currents and milliwatt-level power [1-6], which are prohibitive for battery operation. Given these power constraints, improving the inherently low sensitivity of standard CMOS Hall plates is essential to achieve high resolution. High-voltage (HV) biasing is an attractive approach to enhance sensitivity. However, N-well Hall plates suffer from the JFET effect (Fig. 1) [8]. This effect induces bias-dependent resistance modulation and electrical asymmetry [9], which degrade spinning efficiency and result in large residual offsets. Furthermore, the associated common-mode voltage (V_{CM}) shift causes readout saturation and device overstress, restricting the practical application of HV biasing.

This work presents an energy-efficient Hall magnetic sensor interface that achieves a 1.4 µT (1σ) resolution and a 2.3 µT (3σ) residual offset with a power consumption of 58.9 µW. To enable the practical implementation of sensitivity-enhancing HV biasing, the asymmetry-compensated bipolar high-voltage converter (ACB-HVC) generates differential HV± and recenters the Hall plate V_{CM} within the readout input range while compensating for JFET-induced asymmetry. A switched-capacitor offset-cancellation (SCOC) scheme, combined with an offset-shift technique, further suppresses the residual offset. The proposed interface enables high-precision sensing for battery-powered IoT nodes.

This work is supported by the NRF (RS-2025-00562391, RS-2024-00408040 and IITP (IITP-2026-RS-2020-II201821). The EDA tool was supported by

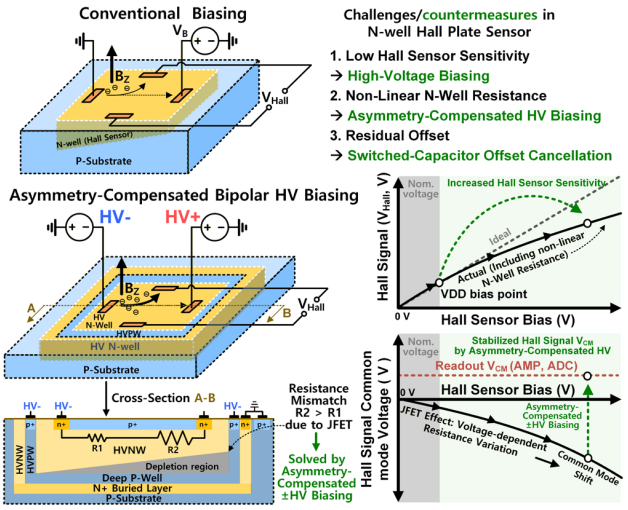

Fig. 1. Conventional N-well Hall plates suffer from JFET nonlinearity, causing offset and V_{CM} shift. HV increases sensitivity, and asymmetry-compensated bipolar HV biasing compensates V_{CM}.

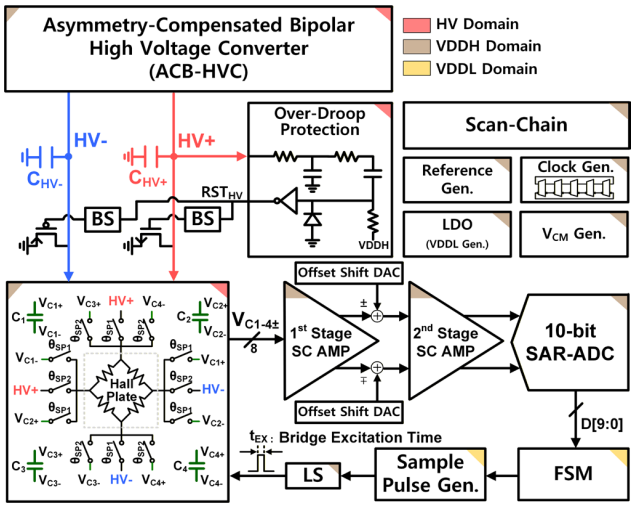

Fig. 2. Top block diagram of the proposed magnetic sensor featuring an ACB-HVC and an SCOC-based readout interface composed of a 2-stage SC amplifier with 6b-offset shift DAC and 10b-SAR-ADC.

II. The Proposed Magnetic Sensor Interface

A. System architecture

Fig. 2 shows the proposed sensor interface comprising an ACB-HVC for HV±, an HV N-well Hall plate, and an SCOC readout interface using a 2-stage SC amplifier with an integrated offset-shifting 6b-DAC [10], and a SAR-ADC. The combination of SCOC and offset-shift further suppresses residual offset caused by process variation and the JFET effect. Peripheral blocks (scan chain, reference, clock, LDO, and V_{CM} generators) provide system configuration, biasing, and timing

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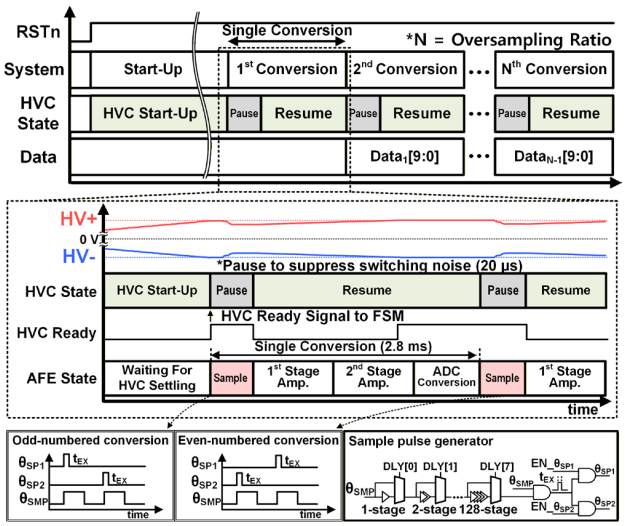

Fig. 3. System timing diagram. The HVC pauses during sampling to minimize switching noise. Duty-cycled excitation (t_{EX}) and interleaved odd/even conversion are used for offset cancellation.

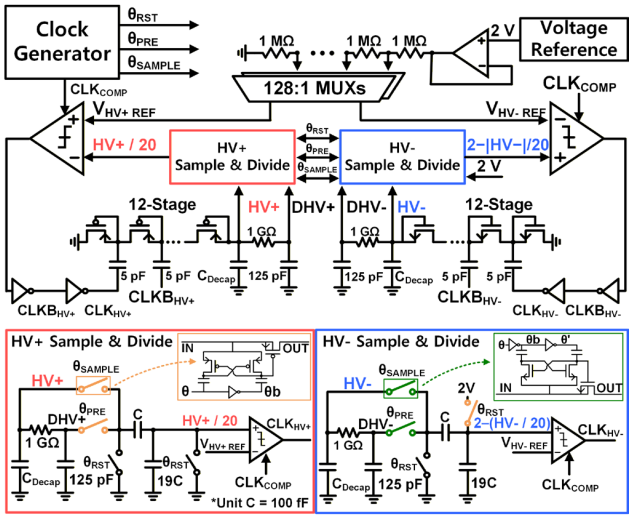

Fig. 4. Schematic Detail of the Asymmetry-Compensated Bipolar High-Voltage Converter (ACB-HVC) including detailed Sample & Divide blocks.

control. Since the Hall plate is driven from an HV domain while the readout operates in a low-voltage domain, over-droop protection monitors the HV rails and asserts RST_{HV} during excessive droop to prevent breakdown.

Fig. 3 shows the overall system operation. After start-up, the ACB-HVC settles HV± and asserts the HVC-ready signal. Each conversion process (2.8 ms) begins with duty-cycled excitation (t_{EX} = 550 ns) that ensures sufficient Hall plate RC settling, followed by sampling, SCOC operation, SC amplification, and SAR-ADC digitization. To minimize switching noise, the HVC pauses (for 20 µs) during the sampling phase. The HV± levels are then fully restored to their target voltage levels during the subsequent resume phase. Odd/even interleaving in the oversampling cycle further reduces the residual offset.

B. Asymmetry-compensated bipolar high-voltage converter

Fig. 4 shows the ACB-HVC with Dickson charge pumps for HV±. In N-well Hall plates, high-voltage biasing exacerbates the JFET effect, causing asymmetric depletion region expansion that nonlinearly shifts the common-mode voltage V_{CM} out of the readout range. To counteract this, the

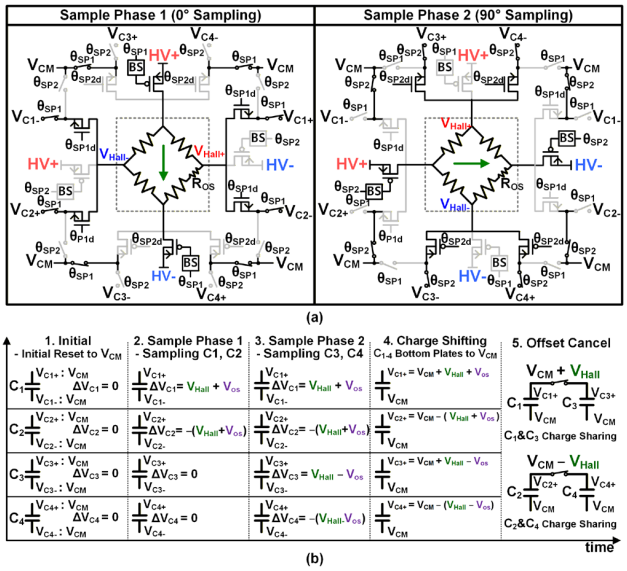

Fig. 5. Proposed switched-capacitor offset cancellation (SCOC) scheme: (a) orthogonal Hall plate biasing configurations for each sampling phase, and (b) SCOC operation sequence for residual offset cancellation.

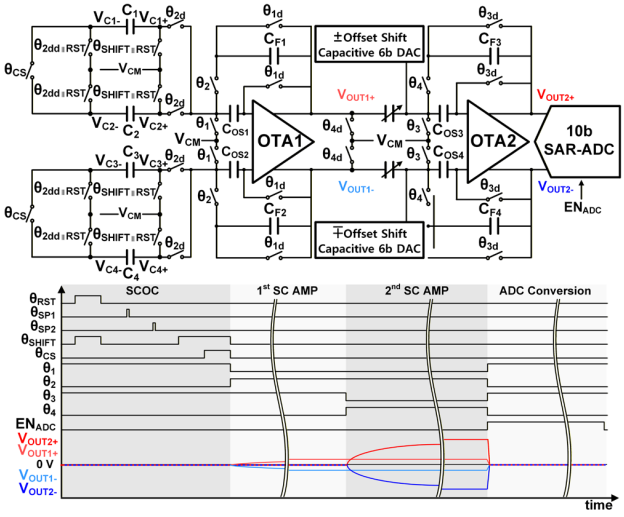

Fig. 6. Schematic and timing diagram of the readout interface: sequence comprises SCOC, two-stage SC amplification, and SAR-ADC conversion.

ACB-HVC employs adjustable references to create an asymmetric bias, realigning the Hall plate V_{CM} within the readout input range. Sample-and-dividers scale HV± to low-voltage levels, specifically HV+/20 and 2-(|HV−|/20), allowing standard low-voltage comparators to monitor the negative rail without headroom issues. Precharged from "dirty" nodes (DHV±) via a large RC path, the sample-and-dividers confine switching ripple to DHV±, keeping HV± clean [11].

C. Switched-capacitor offset cancellation and readout

Fig. 5 shows the SCOC sequence that cancels residual offset via 2-phase spinning with C_1-C_4. Phase 1 biases the Hall plate with HV±, sampling V_{Hall} and offset (V_{OS}) onto C_1 and C_2. In Phase 2, spinning preserves Hall polarity while reversing V_{OS}, which is captured by C_3 and C_4. By returning bottom plates to V_{CM} and connecting C_1/C_3 and C_2/C_4, charge sharing cancels V_{OS}, yielding $V_{CM} \pm V_{Hall}$ at the SC amplifier in Fig. 6.

Fig. 6 shows the readout interface and timing diagram. The offset-cancelled V_{Hall} from the SCOC is amplified by the 1st

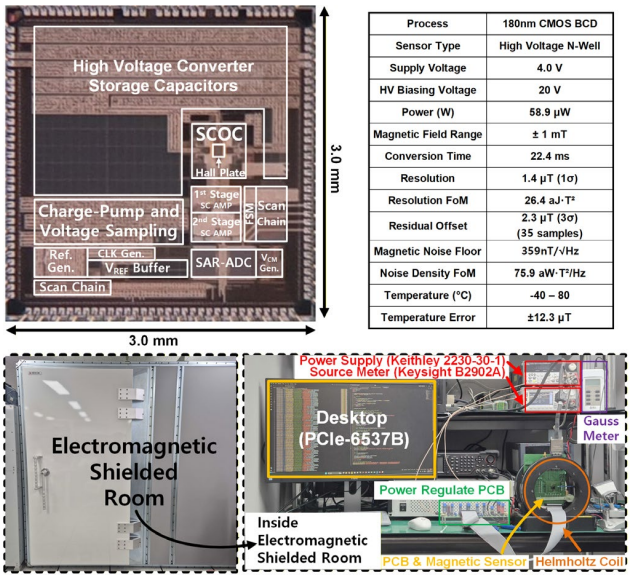

Fig. 7. Die micrograph, performance summary, and measurement setup.

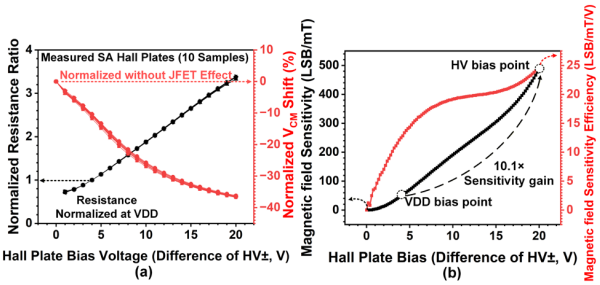

Fig. 8. Measured stand-alone Hall-plate bias dependence and sensor performance: (a) normalized resistance and V_{CM} shift versus bias voltage (10 samples), (b) sensitivity and sensitivity efficiency versus bias voltage.

SC amplifier. The 1st SC amplifier dominates noise performance with kT/C sampling noise from C_1-C_4 of 2.2 pF , which sets the thermal noise floor and balances settling time. The 2nd SC amplifier provides programmable gain (20-83×) to cover Hall plate sensitivity variations. It uses auto-zeroing and an offset-shifting DAC to suppress residual offset, with DAC codes calibrated based on zero-field measurements at room temperature, followed by 10-bit SAR-ADC digitization.

III. Measurement Results and Comparison

The magnetic sensor interface was fabricated in a 180 nm BCD process (Fig. 7) and operated at a 4.0 V supply. The sensor consumes 58.9 μW with the ACB-HVC active (15.1 μW with the ACB-HVC bypassed), achieving a 2.8 ms conversion time over a ±1.0 mT magnetic field range. All magnetic field measurements were performed using a Helmholtz coil, and offset characterization was conducted in an electromagnetic-shielded room as shown in Fig. 7.

Fig. 8(a) presents measurements from 10 stand-alone Hall-plate samples, showing a 3.3× increase in resistance and a 35% V_{CM} shift at 20 V bias due to the JFET effect. These results confirm the significant impact of JFET-induced asymmetry on Hall plate operation and validate the necessity of the proposed ACB-HVC for recentering V_{CM} within the readout input range. Fig. 8(b) demonstrates a 10.1× sensitivity increase at 20 V bias compared to the nominal VDD bias while maintaining voltage-normalized sensitivity efficiency, verifying the effectiveness of high-voltage biasing combined with asymmetry compensation.

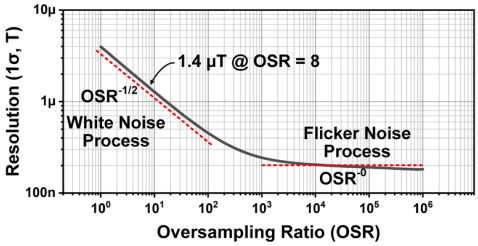

Fig. 9. Measured resolution versus oversampling ratio (OSR).

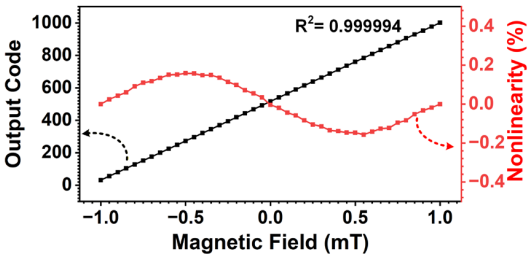

Fig. 10. Measured linearity and nonlinearity across ±1.0 mT range.

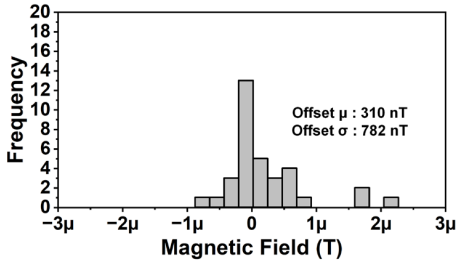

Fig. 11. Measured residual offset distribution (35 samples).

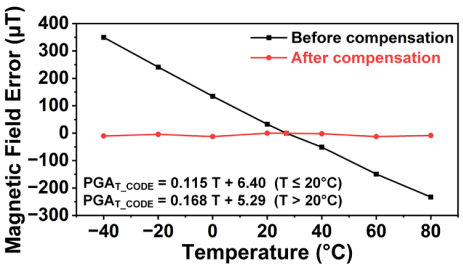

Fig. 12. Measured magnetic field error versus temperature before and after piecewise linear PGA gain compensation (split at 20 °C).

As shown in Fig. 9, the resolution improves with increasing oversampling ratio (OSR), following a thermal-noise-limited trend ($OSR^{-1/2}$) to achieve a nominal resolution of 1.4 μT (1σ) at an OSR of 8. This trend continues until it reaches a flicker-noise-limited floor in the sub-μT range, demonstrating effective low-frequency noise performance of the proposed interface and its potential for higher-precision applications. Fig. 10 shows that the sensor exhibits high linearity with an R^2 of 0.999994 and a nonlinearity of ±0.16% across the ±1.0 mT range. Fig. 11 summarizes the measured residual offset across 35 samples with ACB-HVC, SCOC, and DAC offset-shifting enabled, achieving a mean offset of 0.3 μT and a 3σ residual offset of 2.3 μT.

Fig. 12 shows the measured magnetic field error versus temperature. The temperature error is maintained within ±12.3 μT from -40 to 80 °C using piecewise linear PGA gain compensation split at 20 °C, where the optimal PGA gain codes are determined by piecewise linear fitting to suppress nonlinear temperature-dependent drift. While higher-order compensation could further reduce residual error, piecewise

Table I. Performance summary and comparison with state-of-the-art.

	This Work		TCAS1 2026 Y. Li [6]	ISSCC 2025 F. v. Mourik [5]	JSSC 2019 Y. Li [4]	ISSCC 2012 M. Motz [3]	ISSCC 2007 C. Schott [2]	ISSCC 2005 J. v. d. Meer [1]
	OSR = 1	OSR = 8						
Process	**180 nm BCD**		180 nm BCD	180 nm	350 nm	350 nm	350 nm	180 nm
Hall Sensor Type	**High Voltage N-Well**		N-Well	N-Well	N-Well	N-Well	IMC Hall	N-Well
Supply Voltage	**4 V**		5 V	1.8 V	3.3 V	5 V	3.6 V	5 V
Power	**58.9 µW**		54 mW	9.36 mW	13.2 mW	62.5 mW	18 mW	21 mW
Magnetic Field Range	**± 1.0 mT**		± 96.7 mT	25 mT	± 84.9 mT	± 50 mT	± 0.5 mT	± 10.8 mT
Offset	**2.3 µT (3σ)**		46 µT	1.0 µT (3σ)	237 µT (3σ)	90 µT (3σ)	10 µT	3.65 µT (3σ)
Resolution	**4 µT (1σ)**	**1.4 µT (1σ)**	308 μT_{rms}	0.3 µT[a]	136 μT_{rms}	12.3 µT[a]	0.6 µT[a]	0.67 µT[a]
Nonlinearity	**0.16 %**		—	0.15 %	—	—	1.0%	0.5%
Bandwidth	**178.5 Hz**	**11.2 Hz**	2 MHz	25 Hz	1.7 MHz	10 kHz	100 Hz	5 Hz
Conversion Time	**2.8 ms**	**22.4 ms**	0.25 µs[b]	20 ms[b]	0.3 µs[b]	0.05 ms[b]	5 ms[b]	100 ms[b]
Energy/Conversion	**164.9 nJ**	**1319.4 nJ**	13.5 nJ	187200 nJ	3.9 nJ	3125 nJ	90000 nJ	2100000 nJ
Resolution FoM ($aJ \cdot T^2$)	**26.4**	**25.5**	12806.6	168.5	718.1	4727.8	324.0	9426.9
Temperature Range (°C)	**-40 – 80**		–	–	-40 – 150	-40 – 150	-25 – 100	–
Temperature Error (µT)	**± 12.3 µT[c]**		–	–	339.6 µT[c]	–	–	–

a : calculated based on noise floor **b : calculated based on bandwidth** **- : Not Reported**

c : worst case temperature error *** Resolution FoM = Energy/Conversion × Resolution^2**

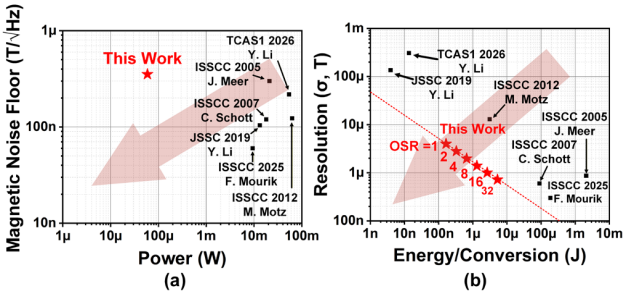

Fig. 13. Benchmark of (a) magnetic noise floor versus power, (b) resolution versus energy per conversion.

linear fitting was selected to minimize hardware complexity and power consumption, which is critical for energy-constrained IoT nodes. Fig. 13(a) and (b) benchmark the proposed design against state-of-the-art Hall magnetic sensors in terms of noise floor versus power and resolution versus energy per conversion, respectively.

Table I summarizes the performance comparison with prior designs [1]-[6]. This work achieves a >150× reduction in power consumption and a >6.3× improvement in resolution FoM compared to the latest integrated Hall sensor [5]. By combining duty-cycled high-voltage biasing with ACB-HVC and SCOC, the design realizes a 10.1× sensitivity gain while effectively suppressing JFET-induced nonlinearity, redefining the noise-power trade-off for Hall magnetic sensors.

IV. Conclusion

This work presented a Hall magnetic sensor interface that overcomes the noise-power trade-off through asymmetry-compensated bipolar high-voltage duty-cycled biasing and switched-capacitor offset cancellation. The ACB-HVC addresses the fundamental JFET-induced challenges of HV biasing, enabling a 10.1× sensitivity gain while maintaining a 2.3 µT (3σ) residual offset. Fabricated in a 180 nm BCD process, the prototype achieves 1.4 µT (1σ) resolution with 58.9 µW power consumption and a resolution FoM of 26.4 $aJ \cdot T^2$, demonstrating the lowest power and best FoM among reported integrated Hall magnetic sensors. These results establish a practical path toward high-precision, low-power magnetic sensing for next-generation IoT applications.

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