

# A $14.6 \mu\text{g}/\sqrt{\text{Hz}}$ , $1.02 \text{ mm}^2/\text{axis}$ MEMS Accelerometer using Energy-Recovery High-Voltage Pulse Excitation with 9.8 pJ Efficiency

Ling Wang<sup>1</sup>, Longjie Zhong<sup>1</sup>, Yi Zhu<sup>1</sup>, Yi Gong<sup>1</sup>, Guangyi Wu<sup>1</sup>, Wenfei Cao<sup>1</sup>,  
Kangkang Cai<sup>2</sup>, Tiegang Hu<sup>2</sup>, Zhangming Zhu<sup>3</sup>

<sup>1</sup>Key Laboratory of Analog Integrated Circuits and Systems (Xidian University), Ministry of Education,  
School of Integrated Circuits, Xidian University, Xi'an, China

<sup>2</sup>Silan Microelectronics, Hangzhou, China

<sup>3</sup>Zhejiang Key Laboratory of Analog Integrated Circuits, Hangzhou Institute of Technology,  
and also with School of Integrated Circuits, Xidian University, Hangzhou, China

Email:ljzhong@xidian.edu.cn, zmyh@263.net

**Abstract**—This work presents an audio MEMS accelerometer using energy-recovery high-voltage pulse excitation (ER-HVPE). The proposed interface circuit is fabricated in  $0.18 \mu\text{m}$  BCD process and measured with a  $1.02 \text{ mm}^2/\text{axis}$  sensor, achieving a low noise floor of  $14.6 \mu\text{g}/\sqrt{\text{Hz}}$  with high efficiency, corresponding to a FoM of 9.8pJ. It also demonstrates high PVT robustness, achieving  $0.016\%/^{\circ}\text{C}$  temperature-induced sensitivity drift and  $3.5\%/V$  supply-induced sensitivity drift.

**Index Terms**—MEMS accelerometer, interface circuit, high efficiency, energy recovery, high-voltage pulse excitation (HVPE), sensitivity drift

## I. INTRODUCTION

MEMS accelerometers for emerging audio applications, including bone-conduction hearables and speech enhancement, require low noise ( $30 \mu\text{g}/\sqrt{\text{Hz}}$ ), wide bandwidth (2kHz), and high linearity ( $\text{THD} < 1\%$ ) while maintaining a small sensor size [1]–[3]. Increasing the excitation voltage is proved to be an effective way to achieve high noise-power efficiency in MEMS accelerometers [4], [5]. A key challenge of high-voltage excitation is the significant nonlinearity introduced by the electrostatic force. To address this issue, high-voltage pulse excitation (HVPE) was reported in [4], where the low-duty-cycle operation alleviates both electrostatic-induced nonlinearity and the pull-in effect. However, as shown in Fig. 1, HVPE-based MEMS accelerometers still suffer from PVT-robustness problem. Firstly, the system power significantly increases with the sensor capacitance increment. Secondly, the sensitivity drifts with the supply and temperature variations. To solve this problem, this work proposes an energy-recovery high-voltage pulse excitation (ER-HVPE) based MEMS accelerometer.

## II. PROPOSED ER-HVPE BASED MEMS ACCELEROMETER

### A. System Architecture

As shown in Fig. 2, a single proof-mass biaxial MEMS sensor is used in the proposed audio MEMS accelerometer to

This work is supported by NSFC (62474132, 62227816).

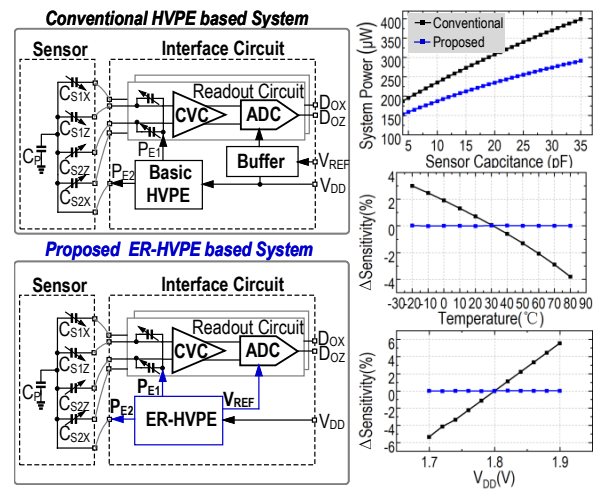


Fig. 1. Comparison of the conventional HVPE and the proposed ER-HVPE MEMS accelerometer.

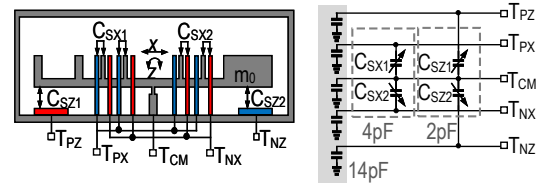


Fig. 2. MEMS sensor of the proposed audio MEMS accelerometer.

achieve low Brownian noise ( $10 \mu\text{g}/\sqrt{\text{Hz}}$ ) with a small sensor size [6], leading to approximately 20-pF sensor capacitance. Fig. 3 shows the block diagram of the ER-HVPE based interface circuit for the proposed audio MEMS accelerometer. The system employs an energy-recovery excitation pulse generator (ER-EPG) to reduce the power consumption and an excitation-voltage reference (EVR) to ensure PVT-robust readout. Driven by two opposite-phase high-voltage excitation pulses ( $P_{E1}$  &  $P_{E2}$ ) generated by the ER-EPG, the capacitor

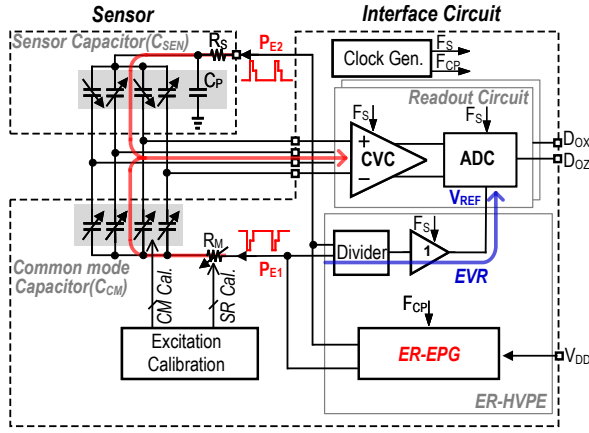


Fig. 3. The block diagram of the proposed ER-HVPE based MEMS accelerometer.

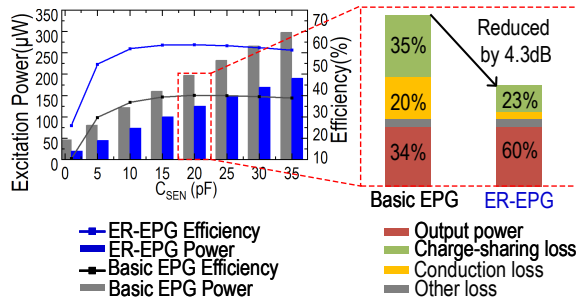


Fig. 4. The power efficiency vs.  $C_{SEN}$  of basic EPG and ER-EPG.

bridge ( $C_{CM}$  &  $C_{SEN}$ ) produces a charge signal, which is converted by a capacitance-to-voltage converter (CVC) and then digitized by an ADC using the EVR.

#### B. Energy-Recovery Excitation Pulse Generator

As shown in Fig. 4, the key idea of the proposed ER-EPG is to reduce the excitation power through efficiency enhancement. The proposed ER-EPG improves the excitation efficiency from 34% to 60%, with  $C_{SEN} = 20\text{pF}$ ,  $C_{E1} = 200\text{pF}$ ,  $C_{E2} = 500\text{pF}$ ,  $C_{CM} = 6\text{pF}$ , and an excitation level of 10.8V. As shown in Fig. 5, there are three designs in the proposed ER-EPG to enhance the excitation efficiency. Firstly, the energy-recovery path (ERP) is employed to reduce the total power consumption by recovering the energy of capacitor  $C_{SEN}$ . Under  $P_{E2}$  excitation, considerable power is consumed during the charging and discharging of  $C_{SEN}$ . During phase  $\Phi_2$ ,  $C_{E1}$  is charged by  $C_{SEN}$  through the ERP, recovering 48% of the energy stored on  $C_{SEN}$ . Secondly, the pre-charge path (PCP) is used to reduce the charge-sharing loss of capacitor  $C_{CM}$  by 47% [7]. During phase  $\Phi_2$ , capacitor  $C_{CM}$  is pre-charged to half of the pulse level (e.g., 5.4V) through the PCP; during phase  $\Phi_3$ , the  $C_{CM}$  is then charged to the full pulse level (e.g., 10.8V). Thirdly, the feedforward energy-storage capacitor  $C_{FF}$  increases the energy-storage capacitance density by  $5\times$  to provide transient

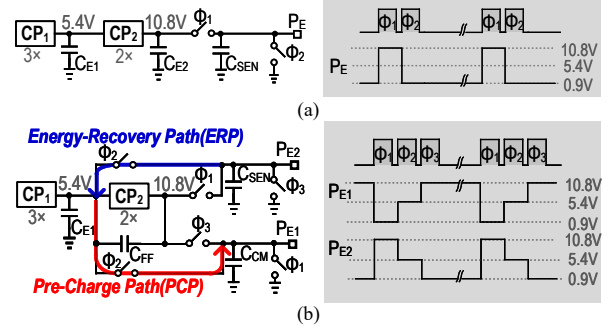


Fig. 5. The topology of (a) the basic EPG and (b) the ER-EPG.

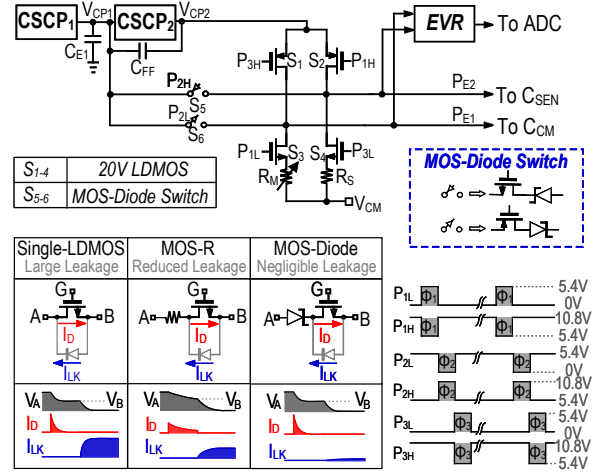


Fig. 6. The switch implementation in the ER-EPG circuit.

energy and minimize the ripple during pulse generation. In the basic EPG, since the  $C_{E2}$  operates at a high voltage (e.g., 10.8V), it can only be implemented by a high breakdown voltage but low capacitance density, such as MIM capacitors with a density of  $1\text{fF}/\mu\text{m}^2$ . To overcome this limitation, the  $C_{FF}$  is used to replace the grounded energy-storage capacitor  $C_{E2}$ , thereby reducing the operating voltage across the energy-storage capacitor by half. As a result, a combination of low-breakdown-voltage high-density capacitors, including MIM capacitors ( $2\text{fF}/\mu\text{m}^2$ ), MOM capacitors ( $0.5\text{fF}/\mu\text{m}^2$ ), and N-well capacitors ( $2.5\text{fF}/\mu\text{m}^2$ ), can be used to achieve an overall capacitance density of  $5\text{fF}/\mu\text{m}^2$ .

As shown in Fig. 6, a key ER-EPG design challenge is the dynamic reverse voltage across  $S_{5,6}$ , formed by the constant voltage  $V_{CP1}$  (e.g., 5.4V) and the pulse voltage  $P_{E1,2}$  (e.g., 0.9–10.8V). A single LDMOS switch suffers from severe leakage ( $I_{LK} > 100\text{mA}$ ) due to body-diode conduction under reverse bias. A MOS-R switch effectively reduces leakage ( $I_{LK} < 0.6\text{mA}$ ), but limits the charge current ( $I_D < 0.9\text{mA}$ ). In this work, a MOS-diode switch is adopted to achieve both low leakage ( $I_{LK} < 2\text{nA}$ ) and large charge current ( $I_D > 2\text{mA}$ ).

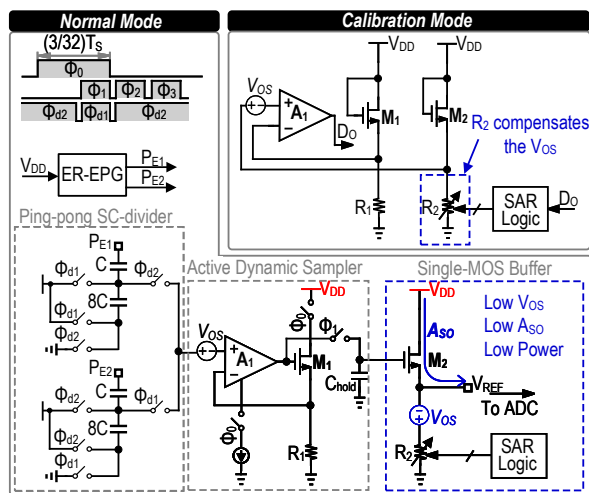
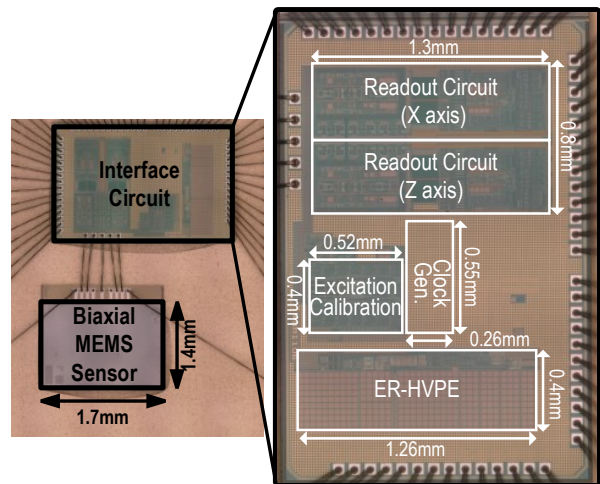
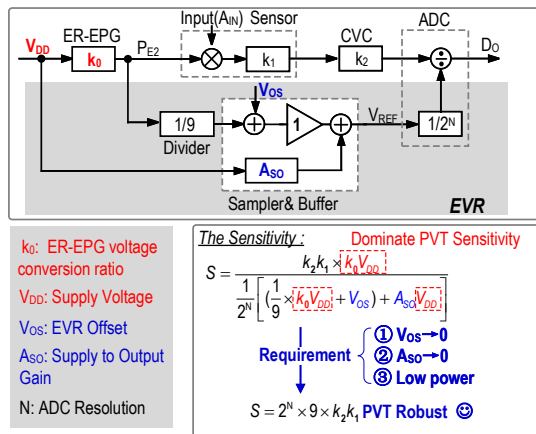


Fig. 8. The circuit implementation of the EVR.

### C. Excitation-Voltage Reference

As shown in Fig. 7, the EVR generates a reference voltage proportional to the excitation voltage for ratiometric readout. In this architecture, PVT variation is embedded in the denominator of the transfer function, which cancels the PVT-induced sensitivity drift in the main signal path. By minimizing EVR offset ( $V_{OS}$ ) and supply-to-output gain ( $A_{SO}$ ), sensitivity variation caused by voltage-conversion-ratio drift and supply fluctuation is effectively suppressed, improving overall PVT robustness.

As shown in Fig. 8, the EVR operates in two modes. In the power-on self-calibration mode,  $V_{OS}$  is compensated by adjusting  $R_2$ . In the normal mode, the excitation pulse  $P_{E2}$  is sampled as the ADC reference through a ping-pong switched-capacitor (SC) divider and an active sampler. In this mode, amplifier  $A_1$  is duty-cycled and pre-biased by a divided pulse  $P_{E1}$ , enabling low-power, fast-response sampling of pulse  $P_{E2}$ . A single-MOS buffer then holds and outputs the sampled pulse voltage with low  $A_{SO}$  and low  $V_{OS}$ .

Fig. 9. Chip micrograph of the MEMS accelerometer.

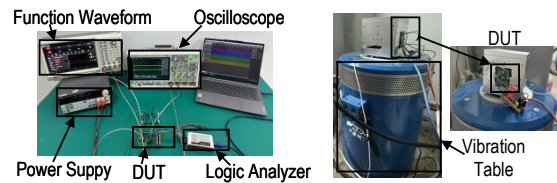


Fig. 10. Test environment.

### III. MEASUREMENT

A prototype of the proposed interface circuit is fabricated in a 0.18 $\mu\text{m}$  BCD process, as shown in Fig. 9. The effective chip area is 1.75mm<sup>2</sup>, and the circuit is measured with a 2.04mm<sup>2</sup> biaxial sensor. The test environment is shown in Fig. 10. As shown in Fig. 11, the optimized system efficiency is achieved with an excitation voltage from 8V to 9.5V. Under typical test conditions (9V excitation voltage and 1g DC input), the MEMS accelerometer achieves a noise floor of 14.6 $\mu\text{g}/\sqrt{\text{Hz}}$ . Owing to energy-recovery and pre-charge operations, the measured transient waveforms of the ER-EPG exhibit a two-step transition. Power breakdown analysis shows that ER-HVPE and CVC dominate the overall noise and power efficiency of the system. Sensitivity-drift measurements are performed on 15 samples, as shown in Fig. 12. With EVR, temperature-induced sensitivity drift over  $-20^{\circ}\text{C}$  to  $80^{\circ}\text{C}$  is suppressed by 16dB. Frequency-dependent supply-induced sensitivity drift is measured by applying a 100mV sinusoidal perturbation to the supply over 10Hz to 10kHz. With EVR and self-calibration enabled, sensitivity drift under a 2kHz supply variation is suppressed by 24dB. The measured root Allan variance shows a bias instability of 6.89 $\mu\text{g}$ . The measured THD versus input acceleration shows THD below 0.3% at 1g input and below 0.5% at 4.5g input. Table I summarizes and compares the proposed design with state-of-the-art MEMS accelerometers. Fig. 13 benchmarks performance in terms of  $FoM_1$ ,  $FoM_2$ , and noise floor. Compared with prior audio MEMS accelerometers [1]–[4], [8], [9], this work achieves both the best noise performance (14.6 $\mu\text{g}/\sqrt{\text{Hz}}$ ) and the best

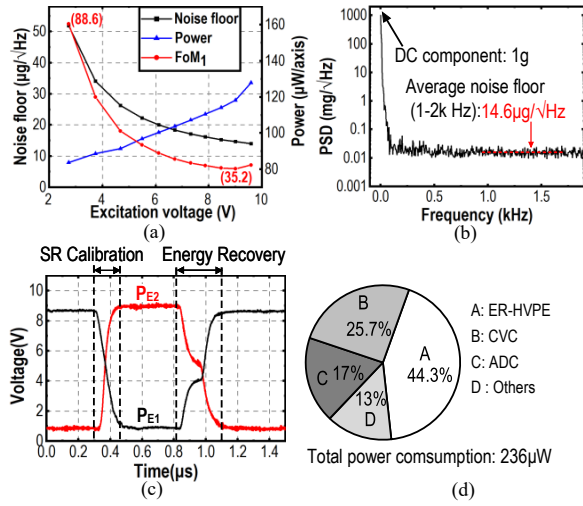


Fig. 11. (a) Measurement results of power efficiency ( $FoM_1$ ) over excitation voltage level; (b) Measured noise performance; (c) Measured transient waveforms of the ER-EPG; (d) Power breakdown.

TABLE I. Comparison with state-of-the-art audio MEMS accelerometers.

|                                      | JSSC '24 [9] | JSSC '24 [8] | TCASI '25 [4] | ADXL 380 [3] | LIS25 BA [2] | BMA 550 [1] | This work |
|--------------------------------------|--------------|--------------|---------------|--------------|--------------|-------------|-----------|
| Process                              | 0.18μm       | 0.18μm       | 0.18μm        | -            | -            | -           | 0.18μm    |
| Supply voltage (V)                   | 1.8          | 1.8          | 1.8           | 2.25-3.6     | 1.8          | 1.7-3.6     | 1.8       |
| Power/ axis (μW)                     | 117000       | 227          | 80            | 374          | 1548         | 261         | 118       |
| Input range (g)                      | ±5000        | ±8           | ±4.5          | ±4           | ±3.85        | ±4.3        | ±4.5      |
| Input bandwidth (Hz)                 | 5700         | 4000         | 2000          | 4000         | 2400         | 2350        | 2400      |
| Sensitivity Temperature drift (%/°C) | -            | -            | -             | 0.02         | 0.08         | 0.02        | 0.016     |
| Noise floor (μg/√Hz)                 | 46.6         | 25           | 32.5          | 20           | 30.6         | 25          | 14.6      |
| Sensor size/axis (mm²)               | 15.6         | 0.93         | 0.64          | 1.08         | 1.33         | 1.2         | 1.02      |
| $FoM_1^2$ (μg·μW/Hz)                 | 72216.2      | 89.7         | 58.1          | 118.3        | 966.9        | 134.6       | 35.2      |
| $FoM_2^3$ (pJ)                       | 18.1         | 14.1         | 16.2          | 37.0         | 314.7        | 39.2        | 9.8       |

<sup>1</sup> Measured by photograph <sup>2</sup>  $FoM_1 = \frac{\text{Power} \times \text{Noise}}{\sqrt{BW}}$  <sup>3</sup>  $FoM_2 = \frac{\text{Power}}{DR \times BW}$

power efficiency ( $FoM_2 = 9.8\text{pJ}$ ).

#### IV. CONCLUSION

The proposed audio MEMS accelerometer achieves a low noise floor of  $14.6\mu\text{g}/\sqrt{\text{Hz}}$  with high efficiency ( $FoM_2 = 9.8\text{pJ}$ ). With ER-HVPE, the excitation efficiency is improved by 26%, and temperature-induced sensitivity drift and supply-induced sensitivity drift are reduced by 16dB and 24dB, respectively.

#### REFERENCES

- [1] Bosch Sensortec, "BMA550 datasheet," Jul. 2023.
- [2] STMicroelectronics, "LIS25BA datasheet," May 2019.
- [3] Analog Devices, "ADXL380 datasheet," Oct. 2024.

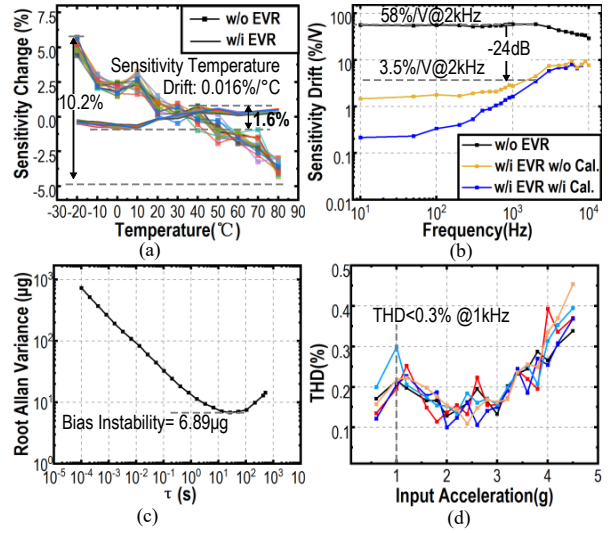


Fig. 12. Measured sensitivity drift induced by (a) temperature and (b) supply variations; (c) Measured root Allan variance; (d) Total harmonic distortion (THD) across input acceleration.

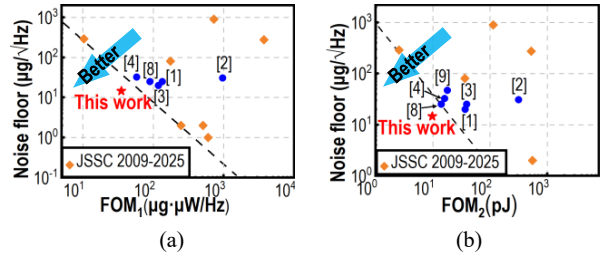


Fig. 13. Performance benchmark.

- [4] L. Zhong, L. Wang, Y. Zhu, W. Cao, P. Shang, and Z. Zhu, "A  $32.5\mu\text{g}/\sqrt{\text{Hz}}$ ,  $0.64\text{mm}^2/\text{axis}$  mems accelerometer using high-voltage pulse excitation and active noise cancellation readout technique," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 73, no. 2, pp. 840–849, 2025.
- [5] Y. Peng, S. Jeong, K. Choo, Y. Kim, L. Y. Chen, R. Rothe, L. Xu, I. Gurin, O. Oliaei, and M. J. Thompson, "An ultralow-power triaxial MEMS accelerometer with high-voltage biasing and electrostatic mismatch compensation," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 7, pp. 2219–2235, Jul. 2024.
- [6] C.-M. Sun, M.-H. Tsai, Y.-C. Liu, and W. Fang, "Implementation of a monolithic single proof-mass tri-axis accelerometer using cmos-mems technique," *IEEE Transactions on Electron devices*, vol. 57, no. 7, pp. 1670–1679, 2010.
- [7] N. Butzen and M. S. J. Steyaert, "Design of soft-charging switched-capacitor DC-DC converters using stage outphasing and multiphase soft-charging," *IEEE Journal of Solid-State Circuits*, vol. 52, no. 12, pp. 3132–3141, Dec. 2017.
- [8] J. Lin, L. Pham, R. Tao, A. Gutmann, S. Guo, A. Cywar, A. Spier, J. Mansson, and K. Nguyen, "A low-power, wide-bandwidth, three-axis MEMS accelerometer ASIC using beyond-resonant-frequency sensing," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 3, pp. 774–783, Mar. 2024.
- [9] X. Li, V. P. Chung, M. G. Guney, T. Mukherjee, G. K. Fedder, and J. Paramesh, "A  $46.6\mu\text{g}/\sqrt{\text{Hz}}$  single-chip accelerometer exploiting a DTC-assisted chopper amplifier," *IEEE Journal of Solid-State Circuits*, vol. 59, no. 2, pp. 502–515, Feb. 2024.