NMOS SOI Source Follower Floating Body Effects Mitigation and Pixel Level Induced Noise Modeling in 3D Sequentially Integrated BSI CIS

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***Abstract*—This paper reports floating body effect (FBE)-induced noise degradation in 3D sequential integration (3DSI) CMOS image sensors (CIS) using SOI source follower (SF) MOSFETs. Statistical measurements on 3DSI pixels show a strong increase in temporal noise when impact ionization-driven FBE is activated, degrading sensor performance. The FBE onset at the pixel operating point is reproduced by TCAD and device-level measurements. Based on these insights, an experimentally validated physics-based transient model is developed to link correlated double sampling (CDS)-dependent noise to floating body charge dynamics. A circuit-friendly calibration and mitigation flow is proposed, including an operating window map for bias and timing optimization, which provides guidelines for robust low-noise CIS design. In our case, a 69% noise reduction is achieved without circuit modification. Additionally, a ground-plane (GP) variant with dynamic back-bias control is demonstrated, enabling FBE mitigation. To the best of our knowledge, this work advances the state of the art as the first to characterize FBE in SOI-based CIS technologies.**

Keywords—FBE, noise, 3DSI, CIS, SOI, ground-plane

I. Introduction

Pixel downscaling targets higher resolution and improved low-light performance, for mobile and automotive imaging applications, but it also degrades certain performance aspects, in particular temporal noise [1]-[4]. This trade-off motivates the transition from 2D to 3D integration, where multiple tiers are vertically stacked [1]. While conventional 3D-stacked CMOS image sensors (CIS) rely on bulk multi-gate or FinFET devices [1]-[4], recent technologies explore the advantages of SOI devices for source follower (SF) transistors, providing improved electrostatic control and reduced parasitic capacitance [5][6]. However, SOI SFs can suffer from floating body effects (FBE), which modify the body potential, degrade noise statistics, and ultimately impact image quality.

The 3D sequential technology presented in this work vertically stacks the photogate (tier-1), the SOI pixel transistors (tier-2), and the digital circuitry (tier-3) using hybrid bonding (Fig.1) [6]. Although FBE is classically associated with partially depleted PD-SOI devices [7][8], the undoped 24 nm SOI film used for the SF transistor in this work can still enable body charging under specific operating conditions, leading to FBE-related phenomena. FBE has been extensively investigated in 3D-DRAM technologies [9], but their impact on CIS remains underreported. This work provides: a quantitative evaluation of FBE-induced noise at pixel level, a physics-based description to characterize FBE, and a calibration flow for FBE detection and mitigation. Table I (Fig.1) benchmarks this contribution against existing work.

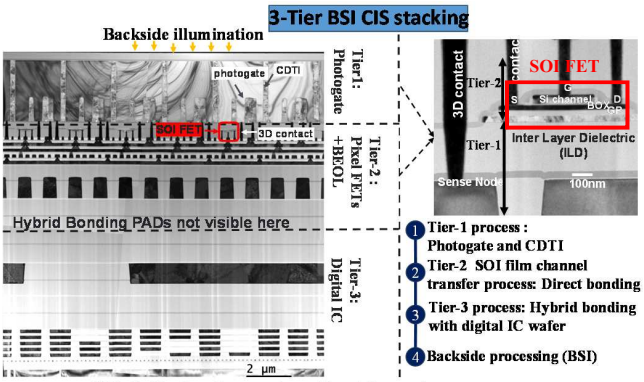


Table I : Benchmark comparison with existing work.

	[1]	[2]–[4]	[5]	This work
Technology	3DSI BSI pixel	1-tier 3D BSI pixel	3DSI BSI pixel	3DSI BSI pixel
SF MOSFET	Bulk	Bulk	SOI	SOI
CIS FB effects	———	———	No	Yes

Fig. 1. 3D sequential integration (3DSI) CIS stack: TEM cross-section of the three-tier architecture, the simplified stacking flow [6], and benchmark comparison with the state of the art.

II. Noise and FBE Investigation

The 1.8 μm 3DSI rolling-shutter pixel under study is summarized in Figs.1 and 2, which show the tier-stack TEM image and a simplified pixel schematic, respectively. The present study focuses on the evaluation of temporal noise performance, measured under dark conditions to suppress photon shot noise. An alternative RESET-ON sequence with a programmable correlated double sampling (CDS) interval T_{CDS} , was implemented to isolate the contribution of the tier-2 SOI SF transistor (Fig.2b). This suppresses reset transistor gate-induced drain leakage and retroactive coupling effects [10]. During readout, the transfer gate (TG) was kept OFF to eliminate its noise contribution. The pixel operates under a constant column current: the SF drain voltage V_D is fixed, the gate voltage V_G is set by the hard reset V_{pix} , and the source voltage V_S follows V_G to maintain the constant drain current. With V_{pix} and T_{CDS} kept constant, sweeping V_D (1000 dark frames per point) reveals a clear noise degradation beyond $V_D =$ 3V (Figs.3a,b). The noise histograms and the complementary cumulative distribution functions (CCDFs) shift toward higher noise levels, which is consistent with an impact-ionization (II)-driven FBE in the SF. In this regime, a high V_{DS} promotes hole accumulation above the buried oxide (BOX), thereby modulating the body potential and the SF threshold voltage, and increasing pixel output fluctuations. Conversely, reducing V_{pix} at fixed V_D also increases V_{DS}, but leads to a weaker degradation in noise statistics, with a lower

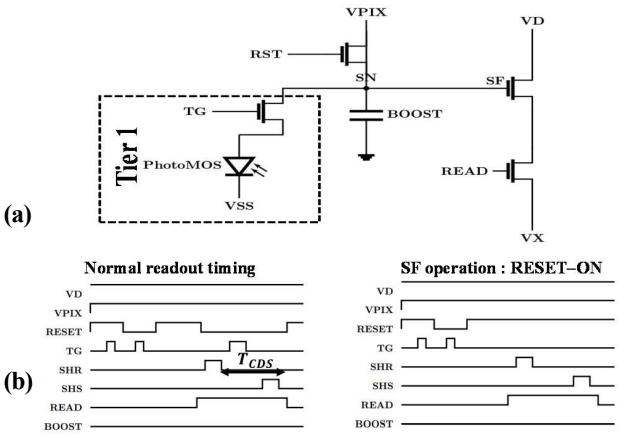


Fig. 2. (a) Simplified schematic of the rolling-shutter pixel with tier-2 SOI SF under constant current bias. (b) Standard readout timing versus the RESET-ON sequence used to isolate the SF noise contribution.

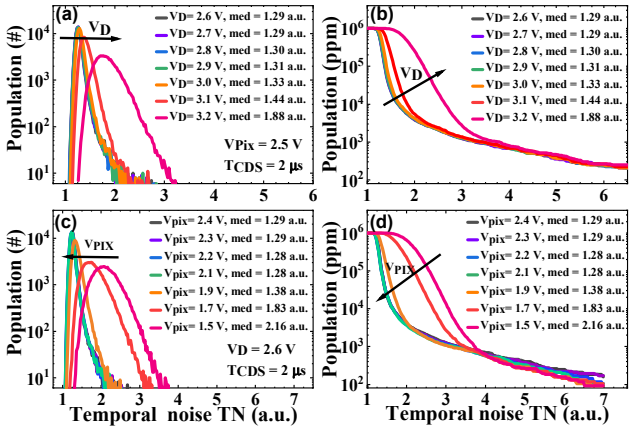


Fig. 3. (a) Noise histograms for a V_D sweep at fixed $V_{pix} = 2.5\,V$, showing progressive degradation beyond 3V. (b) Corresponding complementary cumulative distribution functions. (c) Noise histograms for a V_{pix} sweep at fixed $V_D = 2.6\,V$. (d) Corresponding CCDFs.

onset at $V_{pix} = 1.9\,V$ (Figs.3c,d). This behavior indicates that FBE activation is primarily dominated by the drain bias V_D.

To further investigate this behavior, 2D TCAD simulations were performed on NMOS devices identical to the SF transistors, operated under realistic pixel operating conditions (Fig.4). The resulting hole-density maps clearly reveal the build-up of floating body charge for both biasing strategies, with a more pronounced accumulation when increasing V_D. The onset of this charge build-up is consistent with the system-level behavior observed in Fig.3. For comparable V_{DS}, the extracted floating body charge Q_{FB} is larger for the increasing-V_D strategy (Fig.5). Lowering V_{pix} reduces Vs and increases body-to-source voltage V_{BS}, which enhances hole evacuation through the body-source junction and thus limits the floating-body charge build-up at a constant drain current.

Device-level measurements under pixel conditions confirm that $V_D \geq 3\,V$ corresponds to the FBE activation region. Both the $I_D(V_D)$ characteristic and the output conductance g_{DS} exhibit a kink-like behavior close to this onset (Figs.6a,b). Low-frequency noise power spectral density (PSD) measurements show a dynamic transition: below 2.9 V, the spectrum is strongly dominated by 1/f flicker noise, while above 3 V, a clear Lorentzian excess-noise component, also

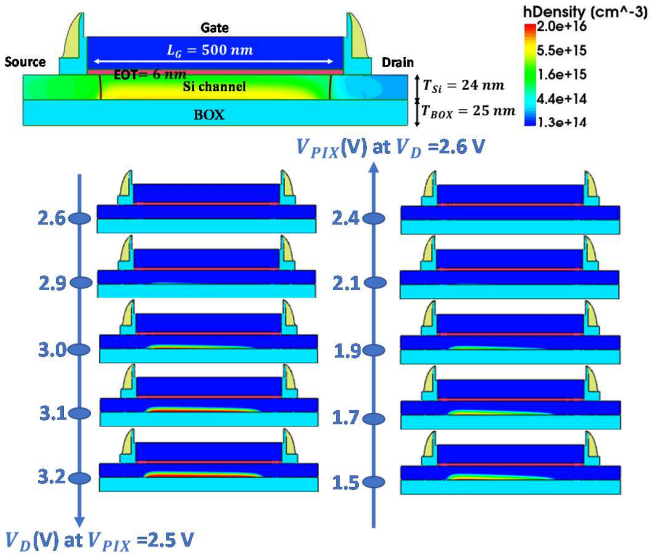


Fig. 4. TCAD-simulated SOI SF device and hole-density maps showing floating body charge build-up for two biasing strategies: increasing V_D and decreasing V_{pix}. FBE appears beyond V_D =3 V and V_{pix} =1.9 V, consistent with pixel noise statistics.

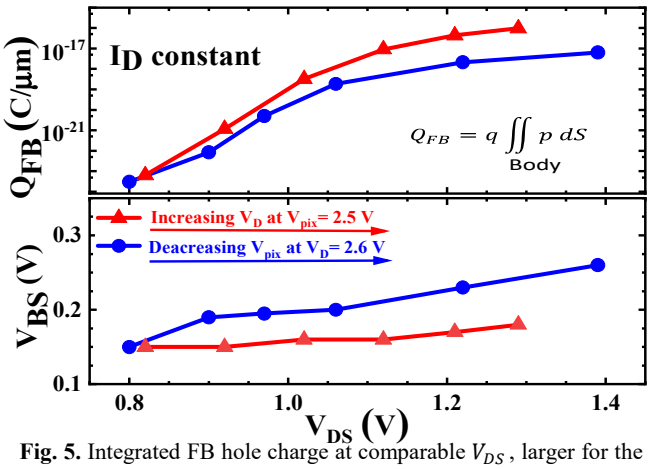


Fig. 5. Integrated FB hole charge at comparable V_{DS}, larger for the increasing-V_D strategy. Extracted body to source voltage V_{BS} shows that decreasing V_{pix} enhances hole evacuation.

characteristic of floating body effect dynamics [11], appears (Fig.6c). This Lorentzian is highlighted as a peak around the corner frequency f_c in the $PSD \times f$ representation (Fig.6d). As V_D increases, f_c shifts toward higher frequencies, indicating faster floating body charging dynamics, consistent with an effective RC-like behavior of the body node.

Based on these static (kink in g_{DS}) and dynamic (Lorentzian PSD) FBE signatures, (V_D, V_{pix})= (2.6, 2.5 V) is selected as the near-safe operating point for subsequent FBE modeling.

III. FBE MODELING THROUGH TRANSIENT BEHAVIOR

Using T_{CDS} as a controlled window enables direct observation of FBE dynamics. at $V_{pix} = 2.5\,V$, noise histograms were measured while sweeping T_{CDS} from 2 to 20 μs in two V_D regimes as shown in Fig.7. In the reference regime (V_D < 3 V, e.g., V_D = 2.6 V), both the histogram median and its shape remain almost invariant with T_{CDS}, which is consistent with a stationary operation, where no FBE is activated within the CDS window. In contrast, in the FBE-active regime (e.g., V_D = 3.2 V), the histograms progressively shift toward higher noise

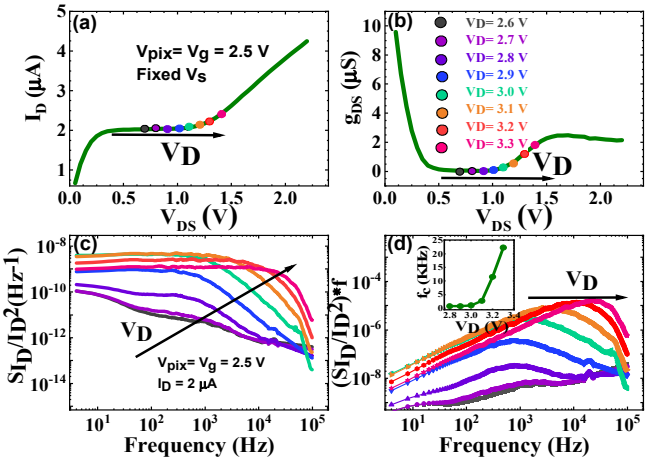


Fig. 6. Device-level electrical measurements under pixel operating conditions. (a) $I_D\,(V_D)$ showing FBE onset near $V_D = 3\,V$. (b) Extracted output conductance g_{DS} exhibiting a kink behavior. (c) Noise PSD revealing a clear Lorentzian noise component in the FBE region. (d) $PSD \times f$ highlighting the Lorentzian peak at corner frequency f_c, which increases with V_D.

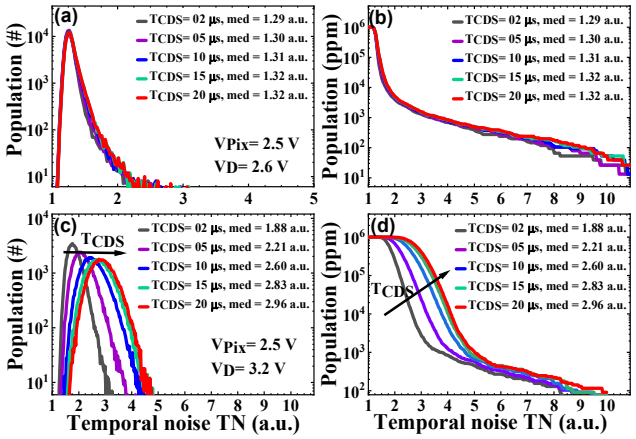
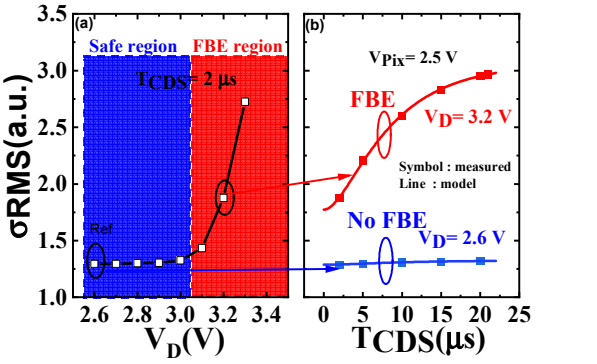


Fig. 7. FBE transient behavior. (a,b) At V_D = 2.6 V (reference), histograms and CCDFs are independent of T_{CDS}, indicating a stationary noise during the sampling window. (c,d) At V_D = 3.2 V (FBE-active), histograms and CCDFs shift to higher levels with T_{CDS}, indicating time dependent FB charge build-up during CDS.

levels and broaden as T_{CDS} increases. This behavior confirms a non-stationary drift between the two CDS samples, caused by II-generated holes continuously accumulating in the floating area during readout. Since V_D and V_{pix} remain applied throughout the acquisition, a longer T_{CDS} allows a larger floating body charge build-up, which in turn increases the temporal noise variance.

Using an RC-like representation of the body node, the array-level temporal noise $\sigma_{RMS}\,(T_{CDS})$ is modeled as the quadratic combination of a stationary term σ_{stat} and a transient FB charging contribution, parameterized by an amplitude A and a charging time constant τ_c ((1) in Fig.8). This model accurately fits σ_{RMS} in the FBE-active regime and collapses to T_{CDS}-independent behavior in the reference regime.

The extracted on-chip FBE parameters in Fig.9 show increasing A and decreasing τ_c with V_D, indicating a stronger body charging, and a shorter time required to fully charge the floating region at higher drain bias. This directly affects the noise behavior and transient response of the pixel circuit.



$$\sigma_{RMS}(T_{CDS}) = \sqrt{\sigma_{stat}^2 + \left(A\left(1 - e^{-\frac{T_{CDS}}{\tau_c}}\right)\right)^2} \quad (1)$$

Fig. 8. Transient model validation of FBE-induced noise. (a) measured σ_{RMS} versus V_D showing a clear FBE onset around 3 V through a rapid increase in σ_{RMS}. (b) Model of $\sigma_{RMS}\,(T_{CDS})$ from equation (1) fitting the FBE-active regime and collapsing to a TCDS-independent behavior in the no-FBE regime.

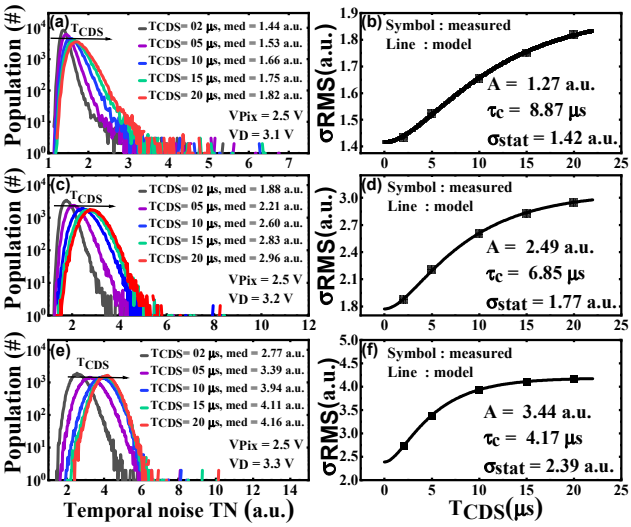
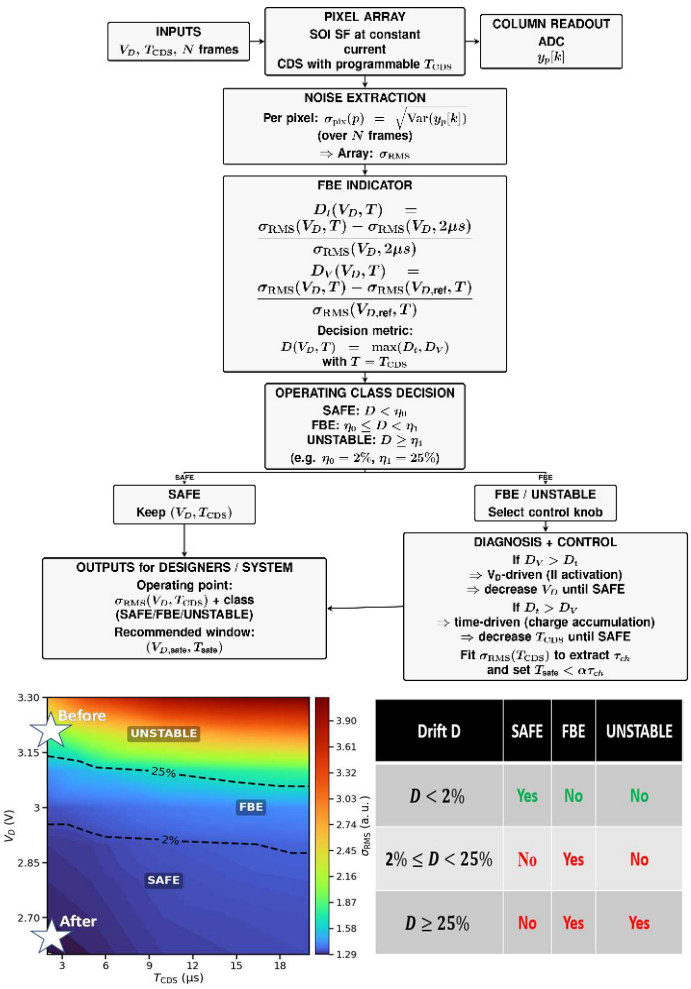


Fig. 9. FBE modeling across drain bias. Noise histograms measured at different V_D values in the FBE-active region show increasing degradation: (a, b) $V_D = 3.1\,V$, (c, d) $V_D = 3.2\,V$, (e, f) $V_D = 3.3\,V$. The transient model accurately fits the data, enabling the extraction of FBE parameters.

IV. Mitigation Flow and Operating Window

The proposed model is translated into a system-oriented bias and timing rules for FBE control (Fig.10). To detect FBE-induced noise degradation, a drift indicator D is defined at array level, quantifying the non-stationary shift of the pixel output between the two CDS samples. Mitigation is then performed by acting on two knobs: the SF drain bias, and the CDS time. First, V_D can be reduced to move the pixel out of the strong FBE region. Alternatively, for a given V_D, the CDS window can be constrained such that $T_{CDS} < \alpha\tau_c$, where τ_c is the extracted FB charging time constant and α is a fixed parameter. This ensures that the floating body charge has insufficient time to significantly change between the two CDS samples, thereby limiting the FBE-induced drift. Starting from an initial operating point, the proposed flow evaluates D, and based on the model, iteratively selects either a bias or timing adjustment until the operating conditions fall into a safe region, where FBE-induced drift remains negligible.



Drift D	SAFE	FBE	UNSTABLE
$D < 2\%$	Yes	No	No
$2\% \le D < 25\%$	No	Yes	No
$D \ge 25\%$	No	Yes	Yes

Figure. 10. Model-guided flow for FBE noise detection and mitigation, and corresponding operating-window map. The heatmap and drift indicator classify operating points into SAFE, FBE, and UNSTABLE regions. Star markers show initial and optimized bias points.

Using this rule, a safe operating area map is generated (Fig.10), providing a direct view of the admissible (V_D , T_{CDS}) combinations and the corresponding actionable decisions compatible with standard CIS bias generation and timing control schemes. In our case, optimizing the SF bias improves noise performance by 69% while preserving the other pixel metrics. The proposed flow can be deployed as a periodic calibration applicable to any SOI-based CIS architecture susceptible to FBE.

V. Additional Design Solution

While recent SOI-based 3D CIS pixels reported in [5] do not include a ground plane (GP), our technology offers a variant with dynamic back-bias through the GP implemented beneath the BOX (Fig.11a). TCAD simulations and device-level measurements in Figs.11a,b show that a positive V_{GP} creates a back-bias field that neutralizes the floating body charge, suppressing hole build-up. As a result, both the static and dynamic FBE signatures observed at $V_{GP} = 0\ V$ disappear when V_{GP} is increased to 2 V, and the associated noise level is significantly reduced. This demonstrates a clear advantage over existing SOI-based CIS implementations without ground-plane [5].

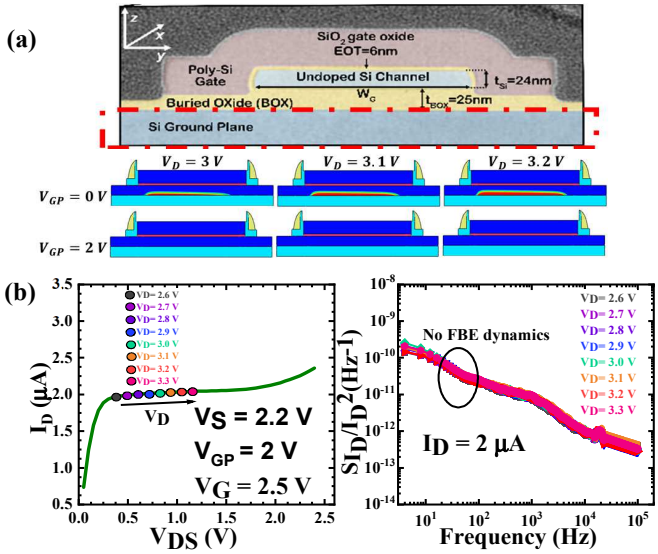


Figure. 11. (a) TEM cross-section of the SOI SF device and TCAD hole density maps showing suppressed hole accumulation under positive GP bias, even at high V_D. (b) Transistor measurements confirming suppression of static (I_D -V_D) and dynamic (noise PSD) FBE signatures, in contrast to V_{GP} = 0 V (Fig.6).

VI. Conclusion

This work provides a complete system-to-device FBE study, combining pixel noise statistics, TCAD simulations, device-level characterizations, and a physics-based model. Impact ionization-driven FBE is identified as the root cause of noise degradation. The proposed transient model extracts FBE characteristics, and enables a mitigation flow and an operating window, achieving 69% noise reduction. In addition, a ground-plane (GP) pixel variant is demonstrated as an effective design solution to mitigate FBE-induced noise.

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