A PVT-robust 500 mV_{PP} 10 kHz-BW Time-domain ExG-to-Digital Frontend Using a Frequency-domain Common-mode Feedback Linearization Technique

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***Abstract*—This paper presents a PVT-robust, high-dynamic-range time-domain continuous-time delta-sigma modulator (CTDSM) for the direct digitization of biopotential (ExG) signals. The design introduces a frequency-domain common-mode feedback (f-CMFB) technique that globally linearizes time-domain CTDSMs by aligning oscillator non-linearity sidebands with the intrinsic anti-aliasing filter (AAF) sinc-nulls of CTDSMs across the PVT spread. Implemented in a 22 nm FDSOI process, the ExG-to-digital frontend supports a maximum input of 500 mV_{PP} and achieves an 80.8 dB SNDR and an 81 dB DR in a 10 kHz BW while consuming 17.1 µW, corresponding to a FoM_S of 168.5 dB. Enabled by the f-CMFB, the measured SNDR drifts by <3 dB across a 0.74–0.86 V supply variation and a -20 to 60 °C temperature range.**

***Index Terms*—ExG readout, direct-digitization, VCO-based ADC, delta-sigma modulator, time-domain, PVT robustness.**

I. Introduction

For neural recording and brain-computer interfaces, direct-digitization frontends (DDFE) for electrophysiological signals (ExG) are required to achieve a wide DR (>80 dB), low input-referred noise (IRN<100 nV/√Hz), and high input impedance (Z_{IN}>10 MΩ). Such DDFEs based on continuous-time delta-sigma modulators (CTDSMs) as shown in Fig. 1 are popular for their intrinsic anti-aliasing filtering (AAF) property [1]. Conventional voltage-domain [1][2] and voltage-time hybrid-domain CTDSM-based DDFEs [3] offer high SNDR, but rely on power-hungry analog blocks which do not scale well with advanced CMOS processes. More recently, DDFEs based on time-domain (TD) CTDSMs [4][5] have gained attention, thanks to their technology scalability, intrinsic noise-shaping, and implicit dynamic element matching (DEM) properties. However, these time-domain solutions face two fundamental limitations:

(i) *Oscillator non-linearity and inter-stage distortion*: As analyzed in [6], the inherent non-linearity of oscillators generates distortion. Moreover, in higher-order designs, this modulates subsequent TD quantizers, limiting the SNDR to <70 dB [7]. Existing TD-CTDSMs with an SNDR >80 dB face significant trade-offs: they rely on counter-based quantizers [4] that sacrifice intrinsic DEM. Furthermore, these architectures are confined to low-BW (<1 kHz) applications. Attempting to scale them to a 10 kHz-BW drastically reduces Z_{IN} to 220 kΩ [5], as optimal chopping frequency necessitates $f_S/2$ [8].

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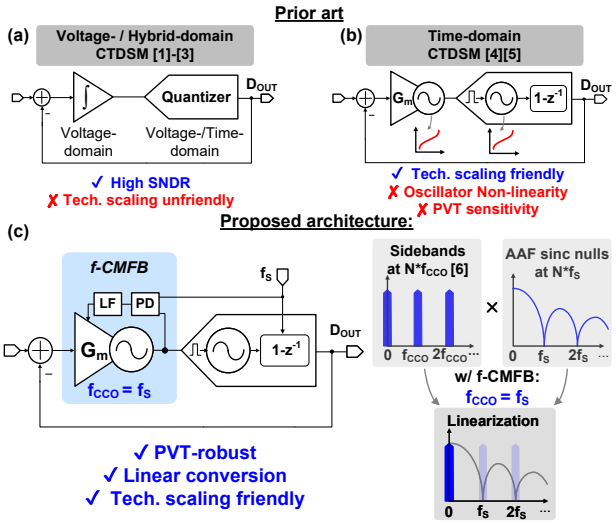

Fig. 1. DDFE architectures: (a) Voltage-/Hybrid-domain CTDSM; (b) Time-domain CTDSM; and (c) Proposed time-domain CTDSM with f-CMFB.

(ii) *PVT sensitivity*: As shown in Fig. 2(a) and analyzed in [7], the SQNR of TD-CTDSMs is highly sensitive to the ratio between the oscillator center frequency (f_{CCO}) and the sampling frequency (f_S), making the system highly vulnerable to PVT variations.

This work addresses the above limitations and trade-offs with a frequency-domain common-mode feedback (f-CMFB) linearization technique as shown in Fig. 1(c). The proposed TD-CTDSM features a PLL-like f-CMFB that locks f_{CCO} to the sampling frequency (f_S), maintaining $f_{CCO} = f_S$ during operation. This ensures:

(i) *Global Linearization*: The inherent non-linearity of oscillators, which appears as sidebands at multiples of f_{CCO} (analysis in [6]), is suppressed by the CTDSM's AAF sinc-nulls at multiples of f_S, since the f-CMFB ensures $f_{CCO} = f_S$. Furthermore, this synchronization drives the subsequent TD quantizer with a frequency-aligned PWM signal, modulating its non-linearity also to multiples of $f_{CCO} = f_S$. This ensures that distortion from the entire signal chain is globally suppressed by the AAF.

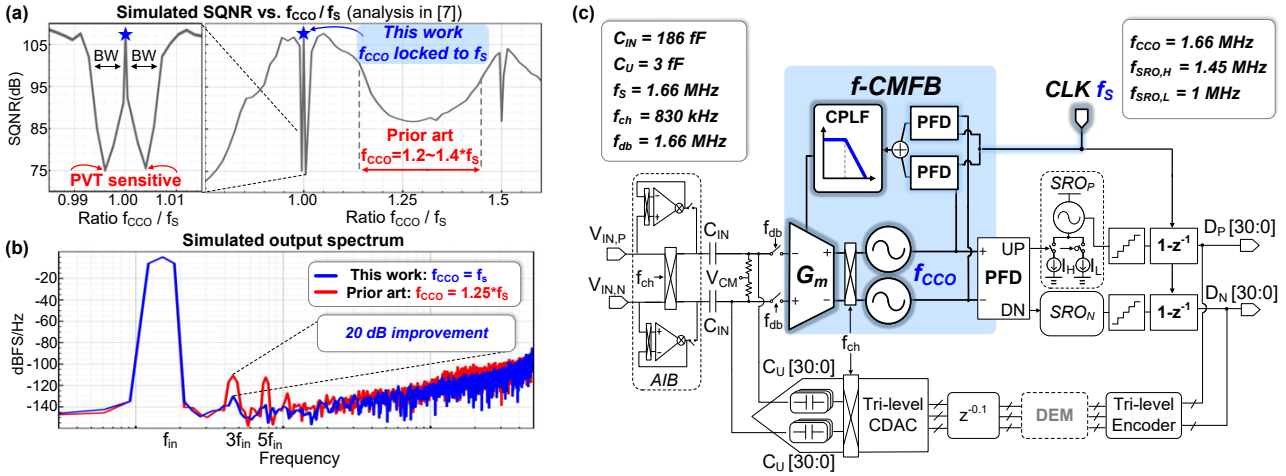

Fig. 2. (a) Simulated SQNR vs. f_{CCO}/f_S of a TD-CTDSM; (b) Simulated output spectra of a TD-CTDSM; (c) System architecture of the proposed DDFE.

(ii) *PVT Robustness*: While prior works trade peak SQNR for uniformity by relying on sub-optimal ratios (f_{CCO}/f_S = 1.2–1.4) and phase-tapping to boost the effective f_{CCO}, the proposed f-CMFB locks f_{CCO} to f_S across all PVT variations, as shown in Fig. 2(a). Operating at this optimal ratio eliminates the need for conservative margins and improves system linearity, as evidenced by the output spectra in Fig. 2(b).

Consequently, the PVT-robust, scaling-friendly TD-DDFE yields an 80.8 dB SNDR in a 10 kHz-BW, and high robustness across a 0.74-0.86 V supply and -20-60 °C temperature range.

II. The Proposed TD-DDFE Architecture

A. System Design

The design details for the DDFE with the proposed f-CMFB architecture are shown in Fig. 2(b). The main signal path begins with an AC-coupled interface driving a Gm-CCO stage, which forms the modulator's core, converting the input voltage into frequency. The CCO's output is then processed by a phase-frequency detector (PFD) resulting in a pulse-width modulated (PWM) signal at the PFD output. The Gm-CCO-PFD chain thus acts as the 1st integrator in the loop filter. The PWM signal drives a pseudo-differential switched-ring-oscillator (SRO) quantizer [9], which provides additional 1st-order noise shaping and intrinsic DEM, leading to an overall 2nd-order noise shaping system. To close the DSM loop, the digital output is fed back to the input through a 6-bit capacitive DAC that employs tri-level switching. To mitigate flicker noise and improve the DAC linearity, system-level chopping is employed around the DSM loop. Several techniques address the non-idealities associated with chopping: (i) bootstrapped switches are used for the input chopper to ensure high linearity; (ii) a deadband technique [1], opening the input of the Gm-stage for 5 ns before chopping instants, converts differential chopping artifacts into common-mode, which are then suppressed by the CMRR of the Gm-stage; and (iii) to counteract the impedance reduction from chopping, an auxiliary impedance boosting (AIB) circuit is employed [1]. Finally, the CCO's linearity is ensured by the key innovation of this work: the f-CMFB loop, implemented as a charge-pump phase-locked loop (CPPLL), which locks f_{CCO} to f_S.

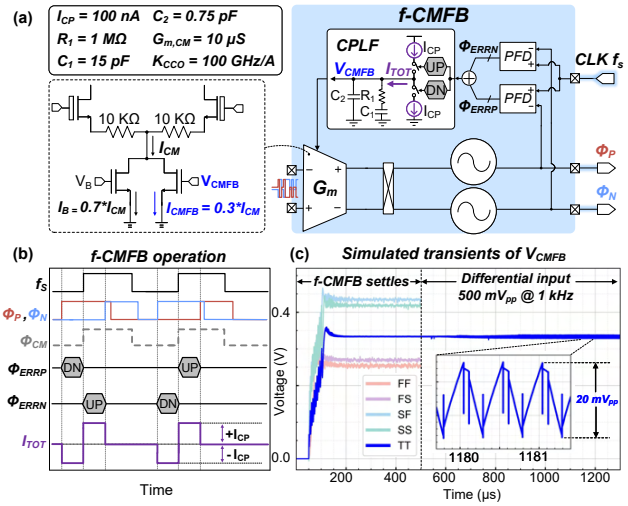

Fig. 3. (a) Detailed implementation of the f-CMFB loop; (b) Operation of the f-CMFB; (c) Transient simulation of the f-CMFB loop.

B. The Proposed f-CMFB

Fig. 3(a) details the implementation of the f-CMFB loop. The positive and negative CCO outputs (Φ_P and Φ_N) are compared respectively against the sampling clock, f_S, using two PFDs built with standard D-flip-flops (DFF) and AND gates. The PFD outputs (Φ_{ERRP} and Φ_{ERRN}) consist of UP and DN pulse signals, where the pulse-width encodes the phase difference between the corresponding CCO output and f_S. The error signals Φ_{ERRP} and Φ_{ERRN} are digitally summed and then drive a charge-pump and loop filter (CPLF). The charge pump (CP) sources current (I_{CP}) in response to UP signals and sinks current for DN signals. The loop filter (LF) then integrates the CP output current (I_{TOT}) to generate the control voltage (V_{CMFB}), which closes the loop by adjusting

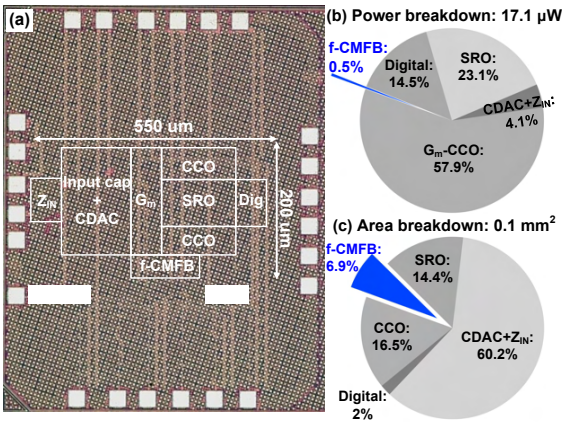

Fig. 4. (a) Chip micrograph; (b) Power breakdown; (c) Area breakdown.

the tail current of the Gm-stage. The Gm-stage is a differential pair degenerated with 10 kΩ resistors for linear V-I conversion and uses thick-oxide input devices for low leakage. To ensure the robust settling of the f-CMFB loop, V_{CMFB} controls a separate tail-current branch carrying up to 30% of the total Gm-stage current, which covers the maximum expected f_{CCO} PVT variations. In the presence of a differential signal, Φ_P and Φ_N become modulated, but as illustrated in Fig. 3(b), their common-mode phase (Φ_{CM}) continues to track f_S. Φ_{ERRP} and Φ_{ERRN}, however, create a ripple on I_{TOT} and consequently on V_{CMFB}. To minimize the V_{CMFB} ripple, the LF main capacitor (C_1) is sized to 15 pF and implemented with an area-efficient MOSCAP, while other loop parameters are chosen to ensure the f-CMFB loop exhibits a phase margin >55° under all process corners, as shown in Fig. 3(c). Under a peak input sinusoid of 500 mV_{PP} at 1 kHz, the resulting ripple on V_{CMFB} is less than 20 mV_{PP} and is further suppressed by the CMRR of the Gm-stage.

III. Measurement Results

Fabricated in a 22 nm FDSOI process, the 0.1 mm^2 design consumes 17.1 µW from a 0.8 V supply. Fig. 4(a) displays the chip micrograph along with the power and area breakdowns (Fig. 4 (b), (c)). The proposed f-CMFB technique introduces a power overhead of 0.5% and an area overhead of 6.9%. To evaluate the effectiveness of this linearization technique, Fig. 5 compares the measured output spectra with and without the f-CMFB active, with a 500 mV_{PP} full-scale sinusoidal input at 1 kHz. When the f-CMFB is disabled and the CCO is manually set to a sub-optimal ratio of f_{CCO}=1.25 f_S, the DDFE exhibits increased harmonic distortion, which degrades the SFDR and SNDR to 80 dB and 74 dB, respectively. In contrast, activating the f-CMFB loop tightly locks f_{CCO} to f_S. This synchronization suppresses the inter-stage distortion, enabling the system to achieve an SFDR, SNDR, and DR of 89 dB, 80.8 dB, and 81 dB, respectively, over a 10 kHz BW.

Fig. 6 highlights the environmental robustness of the proposed architecture by plotting both the measured SNDR and the CCO center frequency (f_{CCO}) across a supply range of 0.74–0.86 V and a temperature range from -20 to 60 °C, with and without the f-CMFB. With the loop enabled, f_{CCO} is

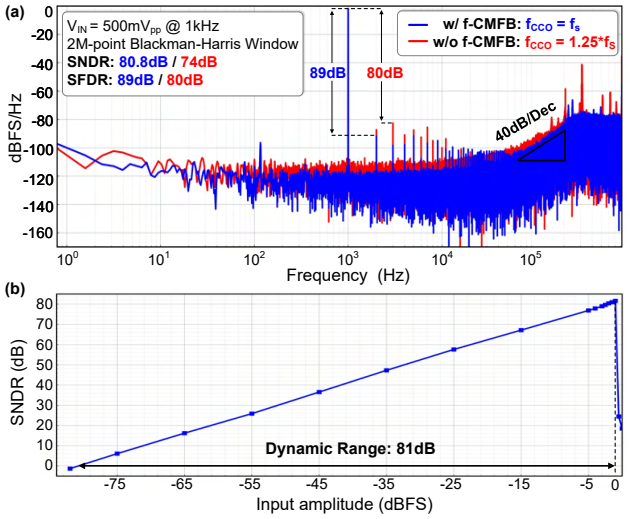

Fig. 5. (a) Measured PSD and SNDR; (b) Measured DR.

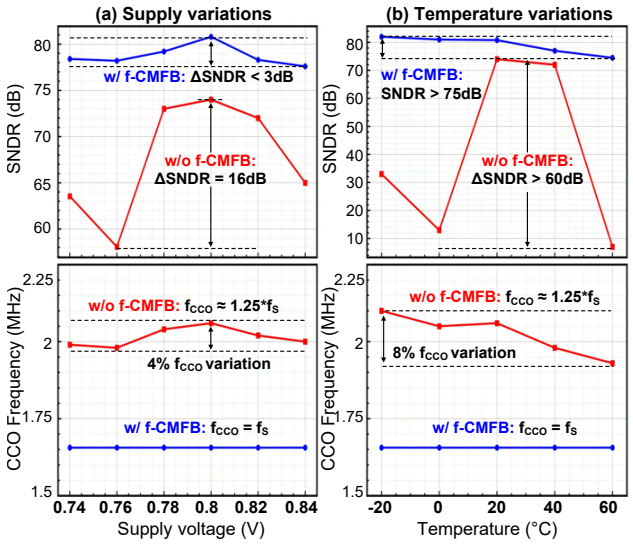

Fig. 6. Measured SNDR and f_{CCO} across (a) supply; and (b) temperature variations .

locked to f_S under all conditions, which directly ensures the robust performance of the DDFE. Consequently, the SNDR is consistently maintained at >75 dB across the entire spread, whereas f_{CCO} drifts and the performance drops significantly when the loop is inactive.

Additional performance characterizations are provided in Fig. 7. The system achieves a measured input-referred noise (IRN) of 84 $nV/\sqrt{Hz}$, which corresponds to an integrated noise of 8.4 μV_{rms} over a 1–10 kHz BW (Fig. 7(a)). Thanks to the AIB circuit, the input impedance (Z_{IN}) is boosted by a factor of 5×, reaching 12 MΩ at DC and 11 MΩ at 1 kHz (Fig. 7(b)). Furthermore, Fig. 7(c) illustrates the intermodulation distortion (IMD) with and without the f-CMFB loop. Activating the f-CMFB loop improves the IMD from 78 dBc to 84.5 dBc.

To validate the practical utility of this design for biomedical applications, Fig. 8 presents measurement results capturing ECG, EMG, and pre-recorded action potentials (APs). The

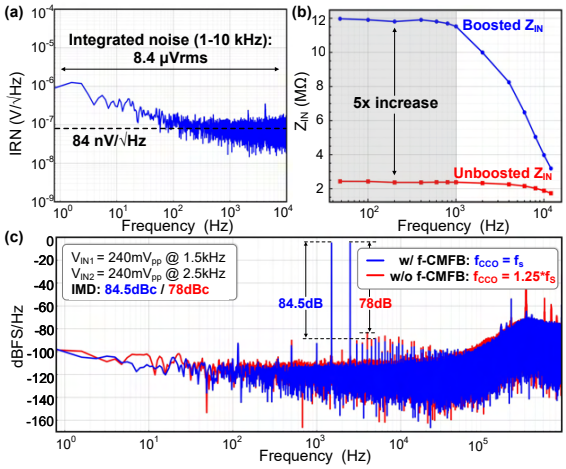

Fig. 7. (a) Measured IRN; (b) Measured Z_{IN}; (c) Measured IMD.

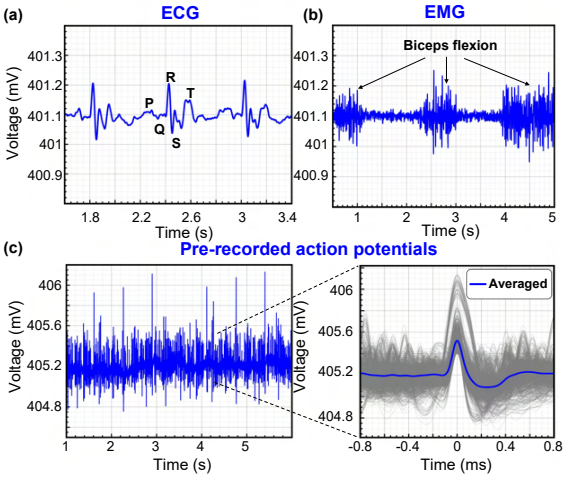

Fig. 8. ExG measurements: (a) ECG; (b) EMG; and (c) pre-recorded APs.

complete electrical measurement setup is detailed in Fig. 9. Finally, Table I compares this work with state-of-the-art DDFEs. Enabled by the f-CMFB, the proposed architecture not only meets stringent DDFE requirements for DR, Z_{IN}, and IRN, but also delivers the highest peak input range and BW alongside a competitive FoM_S of 168.5 dB. As the only inherently PVT-robust design in this comparison, it provides a highly resilient, process-scaling-friendly solution for next-generation ExG readouts.

IV. Conclusion

This work demonstrates a highly resilient time-domain DDFE that overcomes traditional linearity and PVT-sensitivity trade-offs in ExG readouts. Enabled by the f-CMFB technique, the 22 nm FDSOI prototype delivers a 500 mV_{PP} input range, an 80.8 dB SNDR in a 10 kHz bandwidth, and a 168.5 dB FoM_S, while maintaining this linear performance across broad supply and temperature ranges. Importantly, the proposed f-CMFB technique is highly versatile and widely applicable to other TD architectures, offering a low-overhead solution to simultaneously enhance system linearity and PVT robustness.

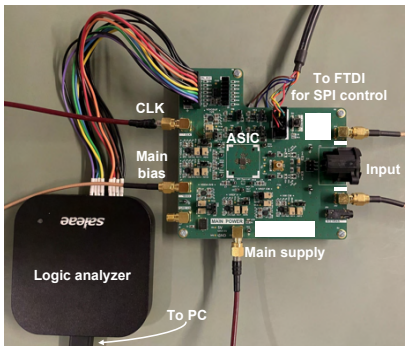

Fig. 9. Electrical measurement setup.

TABLE I
Comparison with State-of-the-Art DDFEs

Parameter	JSSC'18 [1]	ESSERC'24 [2]	JSSC'25 [3]	ISSCC'21 [4]	JSSC'20 [5]	This work
Domain	Voltage	Voltage	Hybrid	Time	Time	**Time**
PVT-robust	No	No	No	No	No	**Yes**
Sampling frequency (Hz)	200k	80k	1.28M	200k	2.5M	**1.66M**
Process (nm)	65	180	180	65	40	**22**
Supply A/D(V)	1.2/1.2	1.2/1.2	0.9/0.7	1.2/0.8	0.8/0.6	**0.8/0.8**
Die area (mm^2)	0.113	0.374	0.073	0.075	0.025	**0.1**
BW (Hz)	5k	2.5k	10k	1k	10k	**10k**
IRN (nV/√Hz)	90	116	60	110	36	**84**
CMRR (dB)	78	>71.5	75	89	83	**77**
Power (µW)	7.3	5.3	11.7	5.8	4.68	**17.1**
Peak input (mV$_{pp}$)	200	180	125	400	100/400	**500**
Peak SNDR (dB)	78	80.8	78.6	92.3	78.5	**80.8**
DR (dB)	81	81.6	78.6	92.3	79/91	**81**
Z_{IN} at DC/1kHz (MΩ)	1520/98	10/10	38/N.A	60/50	0.22/0.22	**12/11**
FoM_S (dB)	166.4	167.5	167	174.7	172	**168.5**

FoM_S = SNDR+ 10*log$_{10}$(BW/Power)

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