Alternating Bit-Line 3D-DRAM Architecture for Reduced Inter-Bit-Line Coupling

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***Abstract*—We propose an alternating Bit-Line (BL) 3D-DRAM architecture that mitigates the BL-BL coupling bottleneck in vertically stacked 3D-DRAM arrays, a promising candidate for future DRAM technology. The proposed structure is validated through a full-flow device-to-circuit evaluation including 3D integration, TCAD calibration, compact modeling, parasitic extraction, and post-layout circuit simulation. We quantified two BL-BL coupling-driven sensing margin degradations, and the proposed structure achieves up to a 2.1× higher sensing margin by mitigating these effects. Under worst-case conditions, 10k HSPICE Monte-Carlo (MC) simulations confirm improved sensing robustness of the proposed architecture, enabling up to a 3.1× higher maximum bit density under BL-pitch scaling.**

***Index Terms*—3D-DRAM, Process Architecture, Compact Modeling, Hybrid Bonding, DTCO**

I. Introduction

As conventional DRAM scaling approaches the sub-10 nm regime, further scaling is constrained by fundamental limitations in patterning challenges and electrical design parameters such as storage capacitance and line resistance. To overcome these limits of planar scaling, 3D-DRAM architectures with vertically stacked memory cells have emerged as a promising candidate for next-generation high-density DRAM technologies [1]–[3]. In conventional 2D-DRAM, WLs and BLs intersect on the horizontal plane, while the storage capacitor is formed vertically above the plane. By contrast, 3D-DRAM employs vertical BLs (VBLs), horizontal WLs (HWLs), and laterally formed capacitors, enabling density scaling through cell stacking rather than continued lateral pitch reduction.

However, this architectural transition introduces a new challenge due to BL coupling. In conventional buried WL cell array transistor (BCAT)-based DRAM, the storage node physically separates adjacent BLs and suppresses direct BL-BL coupling. In VBL-based 3D-DRAM, however, adjacent VBLs directly face each other, which increases BL-BL coupling capacitance. In the worst-case data pattern, where adjacent BLs carry values opposite to that of the victim BL (e.g., 0–1–0), the increased inter-BL coupling degrades the sensing margin and becomes a critical bottleneck for BL-pitch scaling [4].

To address this issue, we propose an alternating BL 3D-DRAM architecture that directly eliminates the BL-BL coupling path. The proposed architecture is validated through a full-flow evaluation spanning process-integration, device calibration and compact modeling, parasitic extraction, and post-layout circuit analysis. Based on this rigorous device-to-circuit assessment, we show that the proposed structure improves sensing robustness and enables higher bit density under pitch scaling by effectively suppressing coupling-induced noise.

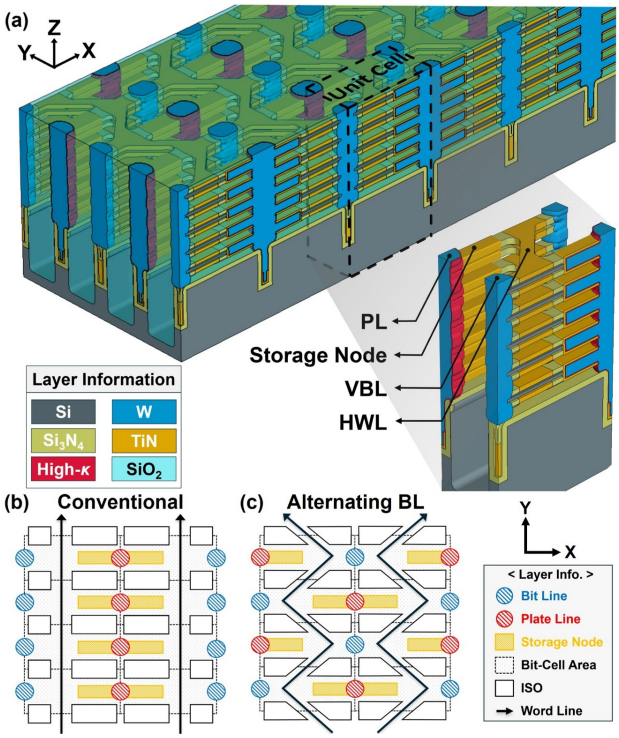

Fig. 1. (a) Overview of the proposed Alternating BL 3D-DRAM architecture. Two-dimensional layout comparison between the (b) conventional structure and (c) proposed Alternating BL structure.

II. Proposed Architecture and Modeling

Fig. 1(a) shows the overall architecture of the proposed Alternating BL structure. The architecture consists of VBLs and zig-zag shaped HWLs, where VBLs and plate-lines (PLs) are alternately placed along the y-direction to prevent adjacent VBLs from directly facing each other. This layout directly removes the BL-BL coupling path that exists in the conventional 3D-DRAM structure. Figs. 1(b) and (c) compare the two-dimensional layouts of the conventional structure and the proposed Alternating BL structure. In the conventional structure, VBLs are positioned on the same side of neighboring cells, leading to increased BL-BL coupling capacitance. By

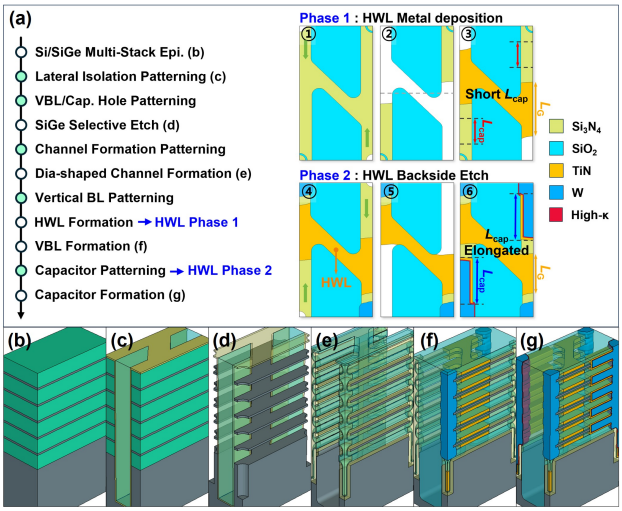

Fig. 2. Process integration scheme: (a) overall fabrication flow highlighting the two-stage HWL formation and (b–g) 3D verification of process steps.

TABLE I
GEOMETRIC PARAMETERS

	Parameters	Unit	Dimension
Unit-Cell	x-Direction Pitch	nm	320
	y-Direction Pitch		160
	WL Vertical Space (S_{WL})		24
Access Tr.	Channel Thickness (T_{CH})	nm	7
	Channel Width (W_{CH})		80 (Max)/22 (Min)
	Gate Oxide Thickness (T_{OX})		4
	Gate Length (L_G)		90
	Gate Height (H_G)		10
Storage Cap.	Storage Cap. Length (L_{cap})	nm	100
	Storage Cap. EOT	Å	4

contrast, the proposed layout alternates the VBL/PL placement and employs a trapezoid-shaped isolation (ISO) layer while maintaining the same two-dimensional bit-cell area as the conventional structure. Detailed geometrical parameters of the proposed structure are summarized in Table I.

To verify the physical feasibility of the proposed layout, the overall process integration flow was simulated using Sentaurus™ Process with careful consideration of process margins at each step, as shown in Figs. 2(b)–(g). One of the key considerations of the proposed structure is the two-stage HWL formation scheme highlighted in Fig. 2(a). In Phase 1, the initial HWL segments are formed to establish the zig-zag routing required by the Alternating BL architecture. In Phase 2, a backside etch process performed after capacitor patterning step defines the gate length (L_G) while simultaneously securing a sufficient storage-capacitor length (L_{cap}). This two-step sequence enables the non-rectilinear HWL routing of the proposed structure without sacrificing bit-cell area.

Based on the integrated 3D structure, Fig. 3(a) summarizes the full modeling flow used in this work, spanning process-architecture implementation, device calibration, and circuit-level modeling. To accurately capture the DRAM access-transistor characteristics, the device parameters were calibrated in technology computer-aided design (TCAD) using fabricated device data [5], as shown in Fig. 3(b). The Inversion Layer

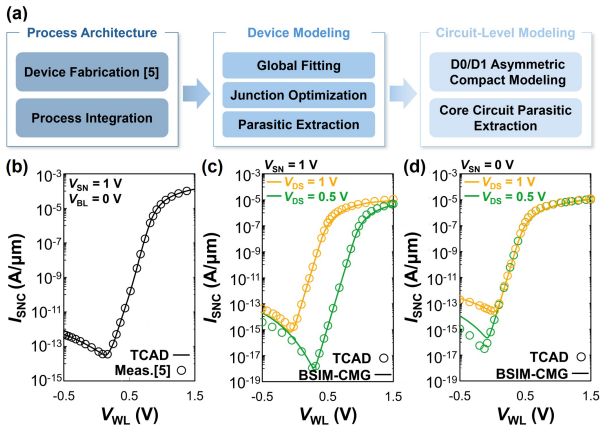

Fig. 3. (a) Overall modeling flow from process architecture to circuit-level modeling. (b) TCAD calibration of transfer characteristics, and BSIM-CMG compact modeling results for the (c) D1 and (d) D0 storage states.

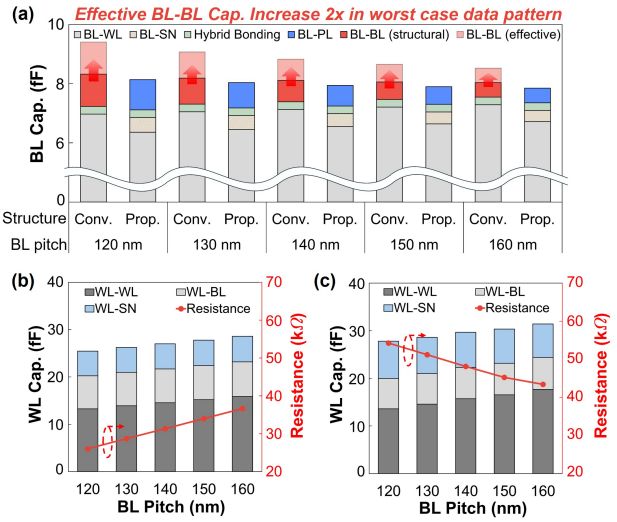

Fig. 4. Parasitic extraction results: (a) BL capacitance at 512 cells per BL and WL RC components of (b) conventional and (c) proposed structure at 512 cells per WL configuration.

Mobility (IALMob) model and the high-field saturation model were employed to reproduce carrier-mobility degradation. In addition, the Shockley-Read-Hall (SRH) recombination model and the Hurkx band-to-band tunneling (BTBT) model were included to fit the subthreshold characteristics. To satisfy the leakage-current requirement of 3D-DRAM cells [6], an asymmetric junction profile was adopted with careful junction optimization. After TCAD calibration and junction optimization, compact modeling was carried out using BSIM-CMG [7] version 110.0.0 under a range of operating conditions, including both D1 and D0 storage states, as shown in Figs. 3(c) and (d). This calibrated device-to-compact-model flow provides the basis for the circuit-level evaluation of the proposed Alternating BL structure.

Fig. 4 reports the parasitic extraction results obtained from the 3D integrated structure. As shown in Fig. 4(a), the proposed structure replaces BL–BL capacitance with BL–PL

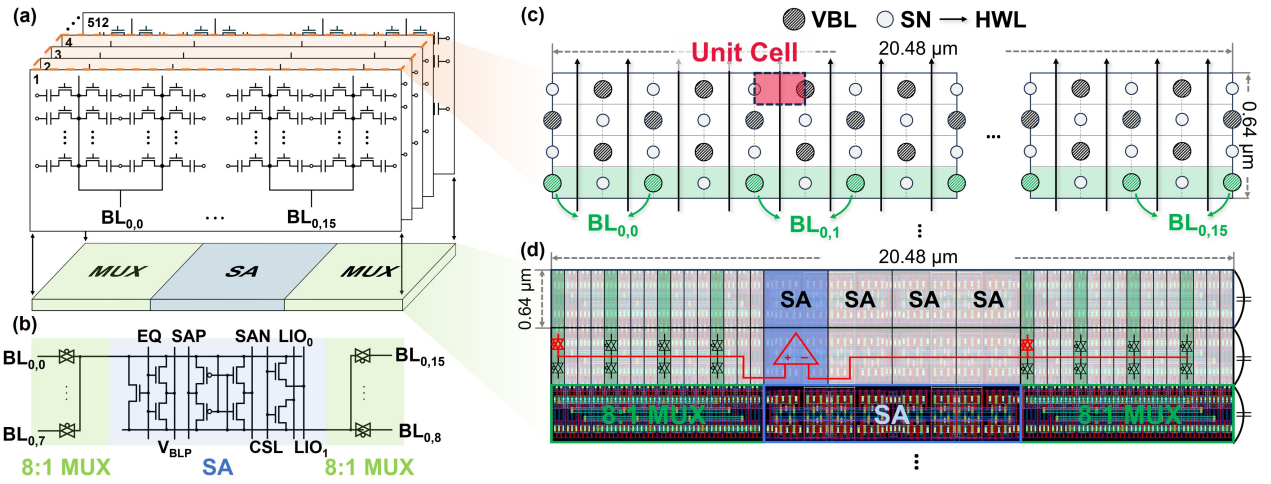

Fig. 5. (a) Schematic of cell MAT at 512×512 MAT size, and 3D CoP scheme with hybrid bonding, (b) schematic of core-circuit, (c) floorplan of proposed 3D-DRAM architecture, and (d) corresponding core-circuit layout verified under 28-nm design rules.

capacitance, thereby reducing the effective BL capacitance increased by adjacent-BL coupling in the conventional structure under worst-case data patterns. This reduction becomes more pronounced as BL pitch shrinks, because the BL–BL coupling component in the conventional structure increases more strongly at tighter pitch. In addition, the zig-zag HWL increases the BL–WL separation, reducing the BL–WL capacitance and leading to a further reduction in total BL capacitance. WL RC parasitic extraction results show that the zig-zag HWL increases WL resistance, reflecting a layout trade-off relative to the conventional structure (Figs. 4(b)–(c)).

III. Core-Circuit Integration and CoP-Aware Floorplanning

Core-circuit design and cell-to-core integration are defined to enable a fair circuit-level evaluation of the proposed Alternating BL architecture. In 3D-DRAM technology based on hybrid bonding, a cell-on-periphery (CoP) organization, in which the cell array is stacked on a separately fabricated core/periphery wafer, is adopted to preserve cell-area efficiency [1], [2]. Consistent with this CoP organization, the core-circuit footprint is constrained to match that of the corresponding cell MAT. Fig. 5(a) illustrates the cell MAT schematic together with the CoP integration concept. Under this MAT-matched footprint constraint, assigning one BL sense amplifier (BLSA) to each BL as in conventional DRAM is difficult in hybrid-bonded 3D-DRAM because direct BL-to-BLSA connection imposes an aggressive bonding pitch requirement and a high BLSA-area requirement within the fixed MAT footprint [8]. Therefore, we adopt an 8:1 MUX with two VBLs tied per MUX input based on the cell dimensions summarized in Table I. By applying a BL multiplexing stage, effective BL loading seen by the BLSA is reduced while preserving the MAT-matched core footprint.

Fig. 5(c) shows the two-dimensional layout organization of the proposed Alternating BL cell MAT. BL groups sharing the same SA are highlighted to clarify the logical mapping between the cell array and the core circuit. Based on this organization, the corresponding core circuit was designed under a 28-nm design-rule constraint with exact area matching to the cell MAT, as shown in Fig. 5(d). The MUX blocks connected to the same SA are color-coded consistently with the associated SA, confirming that the proposed 8:1 MUX + SA organization is layout-feasible within the MAT-matched CoP footprint.

IV. Results and Discussion

3D-DRAM operation of the Alternating BL architecture was verified by post-layout circuit simulations with extracted parasitics, satisfying the JEDEC DDR5 timing specification [9], as shown in Fig. 6(a). Based on this timing-compliant operation, improvements by the proposed scheme are quantified for two coupling-driven sensing degradations.

1) ΔV_{BL} degradation: The proposed Alternating BL architecture improves ΔV_{BL} by eliminating the worst-case BL coupling noise, as shown in Fig. 6(b). The gap between the proposed and conventional schemes increases by up to 10.3% as the BL pitch shrinks.

2) Additional sensing margin ΔV_{min}: Fig. 6(c) shows that ΔV_{min}, defined as the extra margin required to guarantee successful sensing under coupling-induced disturbance [10], is reduced to approximately 0 mV in the proposed structure. In contrast, the conventional structure exhibits a non-zero ΔV_{min} penalty that worsens with scaling.

To summarize the impact of the coupling-driven sensing penalties discussed above, Fig. 6(d) shows the worst-case sensing margin by decomposing the initial ΔV_{BL} at the minimum evaluated BL pitch of 120 nm with V_{core} reduced from its nominal value of 1 V to 0.9 V under a conservative sensing condition. After excluding the coupling-noise and charge leakage components, the proposed structure retains a sensing margin of 52.9 mV in the D0 case, whereas the

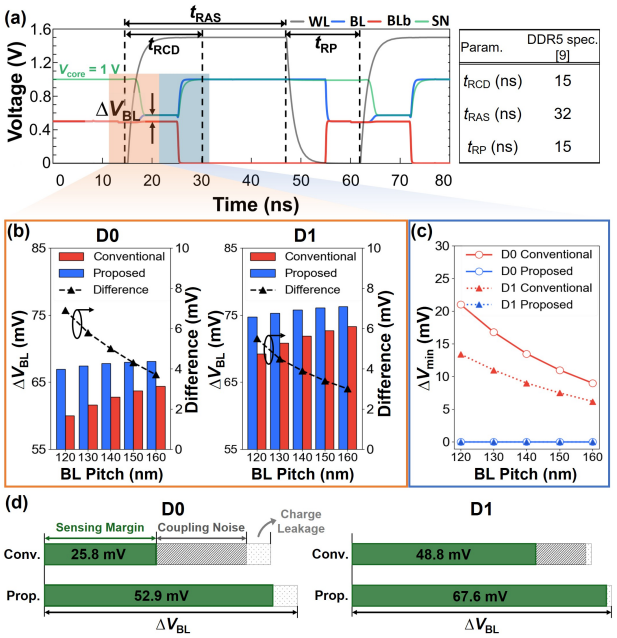

Fig. 6. (a) Post-layout simulation result of 3D-DRAM operation based on JEDEC timing specification, (b) comparison of ΔV_{BL} and (c) ΔV_{min} versus BL pitch, and (d) worst-case sensing margin at D0 and D1 storage states.

conventional structure retains only 25.8 mV, corresponding to up to a 2.1× improvement.

Fig. 7(a) presents post-layout HSPICE MC results from 10k trials for a fixed configuration of 512 cells per BL. Under the conservative sensing conditions discussed above, including reduced core voltage and initial charge-leakage loss, the proposed Alternating BL structure shows zero errors across all evaluated cases, whereas the conventional structure exhibits up to 929 fail bits. Fig. 7(b) summarizes the maximum bit density, where the maximum number of cells per BL is determined using the zero fail bit count (FBC) criterion over 1k MC trials. Due to increased coupling-induced sensing penalty, the conventional structure cannot fully benefit from BL-pitch scaling and therefore exhibits reduced density at tighter pitch. In contrast, the proposed Alternating BL architecture mitigates this coupling penalty and achieves up to a 3.1× higher maximum bit density than the conventional structure.

V. Conclusion

We proposed the Alternating BL 3D-DRAM architecture that eliminates the direct BL-BL coupling path by interleaving VBLs and PLs through a practical integration scheme. The proposed structure was rigorously validated through a full-flow evaluation spanning process integration, device calibration and compact modeling, parasitic extraction, and post-layout circuit simulation. The results show up to a 2.1× higher sensing margin, zero fail bits under worst-case conditions, and up to a 3.1× higher maximum bit density under BL-pitch scaling. These results indicate that the proposed Alternating BL architecture provides a reliable and scalable path toward future high-density 3D-DRAM technologies.

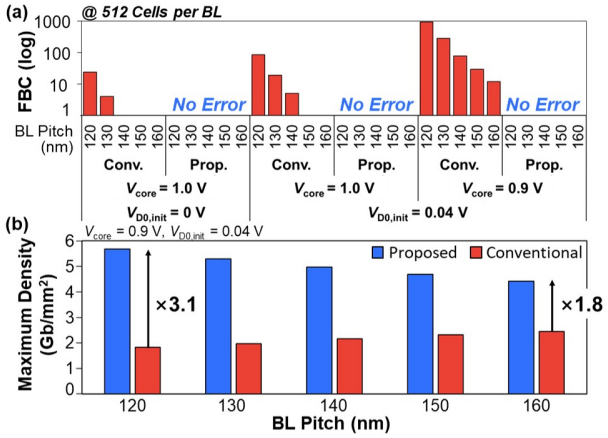

Fig. 7. (a) FBC from 10k MC trials under various sensing conditions, and (b) maximum bit density comparison based on zero-FBC criterion over 1k trials.

Acknowledgment

This work was supported in part by Institute of Information & communications Technology Planning & Evaluation (IITP) grant funded by the Korea government (MSIT) (RS-2023-00256081: artificial intelligence semiconductor support program to nurture the best talents), and BK21 FOUR program and ISRC at Seoul National University. The EDA tool was supported by the IC Design Education Center(IDEC).(Corresponding Author: Jae-Joon Kim).

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