Comments on ESSERC 2025 paper "An Area-Efficient and Low-Power Switched Capacitor Integrator for Discrete-Time Delta Sigma Modulators"

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***Abstract*—A new SC (switched-capacitor) integrator is introduced in [1]: Its sampling capacitor is split, and a discharging phase is added. The authors claim that this reduces the required capacitance while maintaining the same noise performance.**

In this comment, we raise questions about the fundamentals of this technique and present an analysis which shows that it leads to more total capacitance and worse noise performance than using a standard SC integrator with a load capacitor.

I. Overview

In this short note, we compare the authors' SC integrator to the standard parasitic-insensitive SC integrator. The two circuits are very similar, they are described in Fig. 1.

We have analysed track-and-hold and integration independently using the method in [2] and present the noise analysis results with numerical examples using the capacitor values from [1], $C_\mathrm{s} = 2.1\,\mathrm{pF}$, $C_\mathrm{s,aux} = 6.3\,\mathrm{pF}$, and $C_\mathrm{int} = 9.5\,\mathrm{pF}$. For the standard integrator we will use $C_\mathrm{L} = 5.16\,\mathrm{pF}$ such that, using the same g_m, both integrators have the same signal gain and the same noise bandwidth.

II. Track-and-hold (sampling)

SC sampling is done by tracking the input and then holding the value [3]. In phase 1, both capacitors track V_in. In phase 2, C_s continues to track V_in, and $C_\mathrm{s,aux}$ is reset. At the end of phase 2, the charges are held before going to phase 3.

If the switch resistances are low enough for the signals to settle, no information from phase 1 remains on the capacitors by the end of phase 2. Regarding sampled noise (kTC-noise), the theory in [2, Sec. 4 and 5] applies, and the charges on the two capacitors C_s and $C_\mathrm{s,aux}$ at the end of phase 2 become

$$Q_\mathrm{s} = V_\mathrm{in} C_\mathrm{s} + Q_\mathrm{s,e}\,, \quad Q_\mathrm{s,aux} = Q_\mathrm{s,aux,e} \tag{1}$$

where $Q_\mathrm{s,e}$ is a random error with power kTC_s, and $Q_\mathrm{s,aux,e}$ is a random error with power $kTC_\mathrm{s,aux}$. The sum of these charges, $Q_\mathrm{s} + Q_\mathrm{s,aux}$, is transferred to C_int in phase 3.

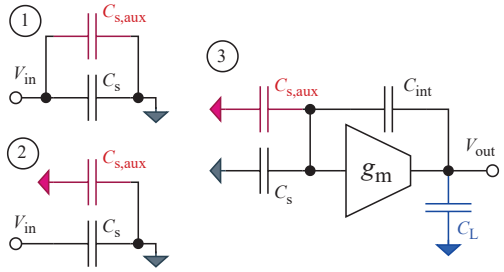

Fig. 1. The authors' SC integrator from [1] and the standard SC integrator are shown here. The phases 1 and 2 track V_in and hold it at the end of phase 2. The charges on C_s and $C_\mathrm{s,aux}$ are transferred to C_int in phase 3. The authors' integrator has a $C_\mathrm{s,aux}$ but no C_L. The standard integrator has a C_L but no $C_\mathrm{s,aux}$, and therefore has only one tracking phase.

The signal charge is $V_\mathrm{in} C_\mathrm{s}$ in both integrators, but the authors' integrator samples more noise. The ratio between the noise powers of the two integrators is

$$\frac{kTC_\mathrm{s,aux} + kTC_\mathrm{s}}{kTC_\mathrm{s}} = \frac{C_\mathrm{s,aux} + C_\mathrm{s}}{C_\mathrm{s}}\,. \tag{2}$$

For the values in Sec. I, this is a factor of 4.0, or 6 dB.

III. Integration (charge transfer)

In phase 3, the presence of $C_\mathrm{s,aux}$ at the input of the OTA in the authors' integrator reduces the noise bandwidth. In the standard SC integrator, the noise bandwidth is reduced by a load capacitor C_load at the output instead. The noise transfer function from the OTA's input-referred noise to V_out for both integrators can be calculated (see, e.g., [2, Sec. 6]). It is

$$T_n(s) = k_n \frac{\omega_p}{s + \omega_p}\,, \quad k_n = \frac{C_\mathrm{int} + C_\mathrm{s} + C_\mathrm{s,aux}}{C_\mathrm{int}} \tag{3}$$

$$\omega_p = \frac{g_m}{C_\mathrm{L}\left(1 + \frac{C_\mathrm{s}+C_\mathrm{s,aux}}{C_\mathrm{int}}\right) + C_\mathrm{s} + C_\mathrm{s,aux}}\,, \tag{4}$$

where k_n is the noise gain and ω_p the pole frequency of the transfer function. The noise bandwidth is $f_n = \omega_p/4$.

For $C_\mathrm{s} = 2.1\,\mathrm{pF}$ and $C_\mathrm{int} = 9.5\,\mathrm{pF}$, the author's integrator with $C_\mathrm{s,aux} = 6.3\,\mathrm{pF}$ and $C_\mathrm{L} = 0$ and the standard integrator with $C_\mathrm{L} = 5.16\,\mathrm{pF}$ and $C_\mathrm{s,aux} = 0$ have the same noise bandwidth f_n and also the same signal gain, $C_\mathrm{s}/C_\mathrm{int} = 0.221$.

Therefore, the ratio between the integrated OTA noise powers in the two integrators only depends on k_n and is

$$\left(\frac{C_\mathrm{int} + C_\mathrm{s} + C_\mathrm{s,aux}}{C_\mathrm{int} + C_\mathrm{s}}\right)^2\,. \tag{5}$$

For the values in Sec. I, this is a factor of 2.38, or 3.77 dB. With the same OTA, signal gain, and bandwidth, the standard integrator has 3.77 dB less integrated OTA noise and uses 1.14 pF less total capacitance than then authors' integrator.

IV. Summary and Conclusion

We have compared the integrator in [1] to the standard integrator having the same OTA, signal gain, and noise bandwidth. The standard integrator needs only two instead of three phases, uses 1.14 pF less total capacitance, and has 6 dB less sampling noise and 3.77 dB less integrated OTA noise. We conclude that the authors' claim of reducing the required capacitance at the same noise level does not hold.

References

[1] Hossein Esmailbeygi et. al., "An Area-Efficient and Low-Power Switched Capacitor Integrator for Discrete-Time Delta Sigma Modulators," *Proc. ESSERC 2025*, München, pp. 229–232.

[2] Hanspeter Schmid et. al., "A tutorial to switched-capacitor noise analysis by hand," *Analog Integr Circ Sig Process*, vol. 89, 2016, pp. 249–261.

[3] Hanspeter Schmid and Alex Huber, "Analysis of switched-capacitor circuits using driving-point signal-flow graphs," *Analog Integr Circ Sig Process*, vol. 96, 2018, pp. 495–507.

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