SiC MOSFET Power Transistor with 32-ns Overcurrent Detection and Self-Powered Protection in a SiP Solution

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***Abstract*—This paper shows an overcurrent-protected Silicon Carbide (SiC) MOSFET with a self-powered Analog Front-End (AFE) integrated circuit in a system-in-package (SiP) arrangement. This solution is completely transparent for the end-user and it is pin-to-pin compatible with a standard SiC MOSFET, achieving overcurrent protection without any dedicated pin and extra component. In normal operation, the SiP behaves electrically as a standard power switch. When a short circuit occurs, the AFE circuit allows extending the short-circuit withstand time of the SiC MOSFET from 1.5 µs to about 4-5 µs, modulating the switch dissipated energy. The proposed 1.8-mm^2 AFE circuit, fabricated in a 400-nm BCD technology, integrates a temperature-compensated current sense circuit and is co-packaged with an 800-V, 80-mΩ SiC MOSFET. Once the short circuit is detected, the AFE circuit features an intervention time of about 140 ns.**

I. Introduction

With respect to Silicon isolated-gate bipolar transistors (Si-IGBTs), Silicon Carbide (SiC) MOSFETs offer better performance in terms of maximum voltage and current. For similar blocking voltage and current ratings, they show higher power density, lower conduction losses and better high-temperature tolerance. On the other hand, because of their smaller active area, SiC MOSFETs show a lower thermal dissipation capability. Therefore, during a short circuit, the junction temperature increases fast and the device is quickly destroyed [1]. This makes, in some applications, the short-circuit withstand time of SiC MOSFETs incompatible with standard short-circuit detection and protection strategies. Desaturation methods, designed originally for Si-IGBTs, sense the voltage across the device to detect the short circuit [2]. However, since in some applications, SiC MOSFETs carry large AC drain current components, to effectively protect the switch desaturation methods require a high threshold voltage or a long filtering time, which are not compatible with the required short-circuit withstand time.

Another possibility to detect short circuits is to sense the drain-source current [3] with a shunt resistor placed in series to the switch, combined with a low-pass filter to prevent false detections due to system noise. Alternatively, it is possible to use a Tunnel Magneto-Resistance (TMR) placed close to the drain-source current path [4]. In any case, current-sense strategies need careful system design and a dedicated circuit to perform detection and protection.

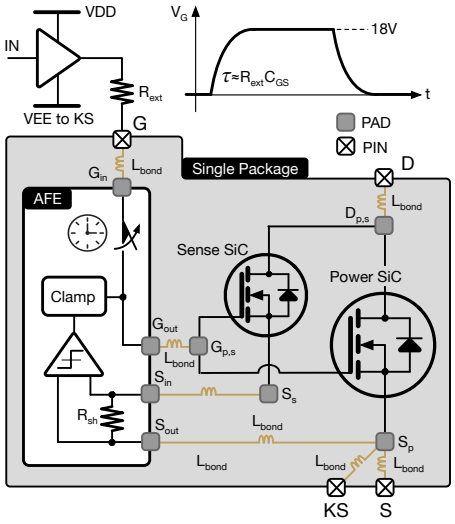

Fig. 1. System level block diagram of the SiP solution.

This paper presents an overcurrent protection method to detect in a fast and reliable way the short-circuit condition of a SiC MOSFET power switch and react in such a way that the perceived short-circuit withstand time is increased, enabling the use of SiC MOSFET in applications where a sufficient short-circuit withstand time is a must. The proposed short-circuit detection solution, being fully integrated in the power switch package without any extra pin and self-powered, is completely transparent for the end-user and does not affect the behavior of the switch in normal operation, as shown in Fig. 1.

II. Overcurrent Protected SiC MOSFET

The system in package (SiP), whose block diagram is shown in Fig. 1, consists of the switch and an analog front-end (AFE) circuit, whose role is to detect the short-circuit condition and react accordingly. The switch active area is split in two parts: Power SiC and Sense SiC, which have common drain and

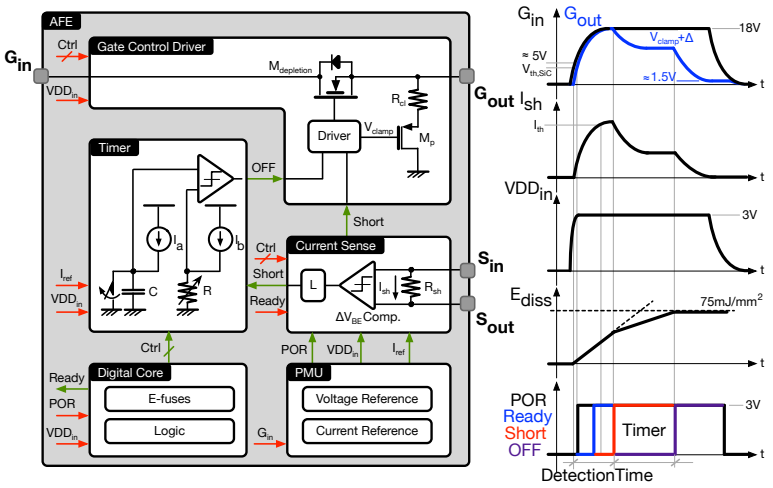

Fig. 2. Circuit block diagram of the AFE and time diagram during a short-circuit event.

gate connections, while the Sense SiC source goes through the AFE circuit before returning to the Power SiC source connection. In the AFE circuit, G_{in} is connected to the SiP gate pin (G), while G_{out} to the actual gate of Power SiC and Sense SiC ($G_{p,s}$). The path between G_{in} and G_{out} is short circuited during normal operation of the switch by a normally-on depletion MOSFET. The Sense SiC current flows through S_{in} and S_{out}, where R_{sh} is placed. No dedicated supply pin is needed for the AFE circuit, since the energy required for its operation is harvested from the 18 V switch gate signal (V_G).

III. Overcurrent Protection Circuit Implementation

The total energy that a SiC MOSFET is able to dissipate during a short circuit before being damaged is about 75 mJ/mm^2. The switch is able to survive for about 2 µs in short-circuit conditions, if it is driven with a gate-source voltage (V_{GS}) of 15 V, but significantly less if it is driven with V_{GS} = 18 V. Fig. 2. shows in detail the AFE circuit architecture together with the timing diagram of the internal signals during a short-circuit event.

The AFE circuit detects the short circuit by sensing the voltage drop across R_{sh}. The detection time, defined as the elapsed time between the wake up of the system (when G_{in} goes above the SiC MOSFET threshold) and the detection of the short circuit, intervention of the protection (intervention time), has has to be as short as possible, since during this phase a lot of energy is dissipated in the SiC MOSFET (V_{GS} is still at 18 V and no current limitation is in place). The energy dissipated during a detection phase of 200 ns is about 25 mJ/mm^2. At the end of the detection phase, the protection phase starts, in which the AFE circuit has to take control of the SiC MOSFET gate voltage to limit the current value and, hence, the energy dissipation. The device isn't turn off immediately to allow system to detect the over current situation.

The Power Management Unit (PMU) block generates voltage (VDD_{in}) and current references (I_{ref}), as well as a power-on-reset (POR) logic signal, which carries the information about the condition of the AFE circuit power supply. The POR signal is asserted when the voltage difference between nodes G_{in} and S_{out} reaches the level required for supplying the AFE circuit and VDD_{in} is stable.

The Digital Core block is an asynchronous digital circuit that, when the POR is asserted, reads the e-fuses, generates the configuration word ($Ctrl$) for the AFE circuit and asserts the $Ready$ signal when successfully finished. The POR and $Ready$ signals, then, enable the comparator output and, hence, the short-circuit protection. The Current Sense block monitors the current in Sense SiC, releasing the $Short$ signal when it crosses a trip threshold (I_{th}). This signal remains latched as long as the POR signal remains high. During normal operation of the SiC MOSFET and in the detection phase, the AFE circuit consumes about 700 µA. The protection phase starts when the $Short$ signal goes high.

The Gate Control Driver block initially disconnects G_{in} from G_{out} (reaction phase) by turning off $M_{depletion}$, allowing the actual gate voltage of the power switch to be easily modulated. Then, the voltage between G_{out} and S_{out} is pulled to the intermediate value $V_{clamp} + \Delta$ (clamp phase) and, finally, it is pulled to a value lower than the power switch threshold (turn-off phase). The clamp phase has the purpose of reducing the short-circuit energy, to allow any other system level protection to detect the abnormal situation and, at the same time, keep the power switch within its short-circuit energy budget. The clamp phase duration is defined by the Timer block, enabled by the $Short$ signal, in which two currents, mirrored from I_{ref}, flow through a capacitor and a resistor, respectively. When the voltage across the capacitor reaches the voltage across the resistor, a comparator asserts the OFF signal that starts the turn-off phase. Voltage V_{clamp} and

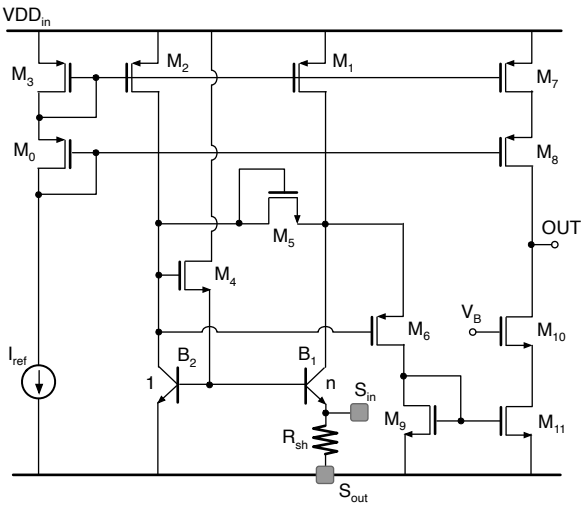

Fig. 3. Schematic diagram of the current sense comparator.

the timer duration can be programmed to fulfill the 75 mJ/mm^2 dissipated energy requirement. During the protection phase the current consumption of the AFE circuit increases to about 8 mA. The current drawn by the AFE circuit decreases the actual voltage at G_{in}, depending on the value of R_{ext}, as shown in Fig. 1.

The comparator used in the Current Sense block exploits an integrated shunt resistor (R_{sh}) to perform the current-to-voltage conversion. This resistor is realized with copper and, therefore, features a temperature coefficient (TC_{Cu}) of about 0.393 %/°C at room temperature. Considering an operating temperature range between –40 °C and 175 °C, the overall resistance variation is 85 %, which is by far too much and has to be compensated for. Moreover, the voltage drop across R_{sh} must be negligible with respect to the voltage between G_{in} and S_{out}, to maximize the matching between Sense SiC and Power SiC. To satisfy all these requirements a ΔV_{BE} based comparator is used, as shown in Fig. 3.

Bipolar transistor B_1 and B_2 feature an emitter-area ratio (n) of 1 to 4, thus leading to a difference between their base-emitter voltages, assuming that they carry the same current, equal to $\Delta V_{BE} = V_T \ln(n)$, which features a temperature coefficient of 0.119 mV/°C (0.34 %/°C), pretty close to TC_{Cu}. Therefore, by using ΔV_{BE} as comparator threshold voltage, TC_{Cu} can be compensated with an acceptable residual error. To better match their actual temperatures, the comparator and the shunt resistor are physically one on top of the other, surrounded by a metal vertical structure to increase the heat spreading.

Transistor M_4 provides the base current for the bipolar transistors, while M_5 clamps the collector voltage of B_1, to prevent it from saturating when the voltage drop across R_{sh} is lower than ΔV_{BE}, minimizing the comparator delay. Transistors B_1 and B_2 are biased by M_1 and M_1 with $I_1 = 2 \times I_2$. When the voltage drop across R_{sh} is equal to

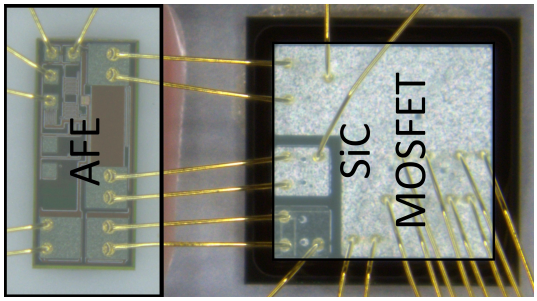

Fig. 4. Micrograph of the SiP, including AFE circuit chip and SiC MOSFET.

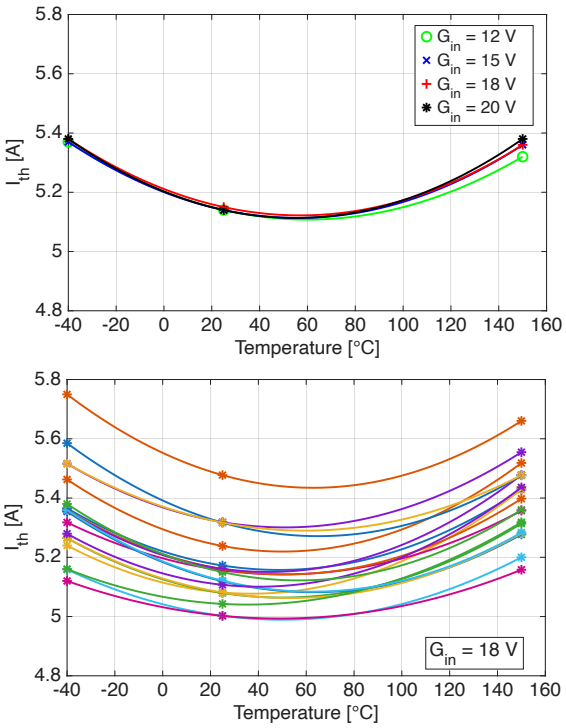

Fig. 5. Measured I_{th} as a function of temperature and G_{in}, and measured I_{th} as a function of temperature for 18 samples

ΔV_{BE}, which represents the trip point of the comparator, B_1 and B_2 carry the same current (I_2) and half of I_1 flows in the output stage ($I_{out} = I_1 - I_2 = I_2$).

IV. Experimental Results

Fig. 4 shows the micrograph of the SiP module, including the 1.8-mm^2 AFE circuit chip, realized in a 130-nm BCD technology, and the SiC MOSFET. Fig. 5 reports the value of the trip threshold current (I_{th}) as a function of temperature for different voltage values at G_{in}, showing acceptable residual voltage and temperature dependency ($< 5\,\%$). The value of I_{th} as a function of temperature for 18 different samples with $G_{in} = 18$ V is also shown in Fig. 5.

Fig. 6 illustrates the transient response of the comparator, showing that the Short signal changes state with a delay of

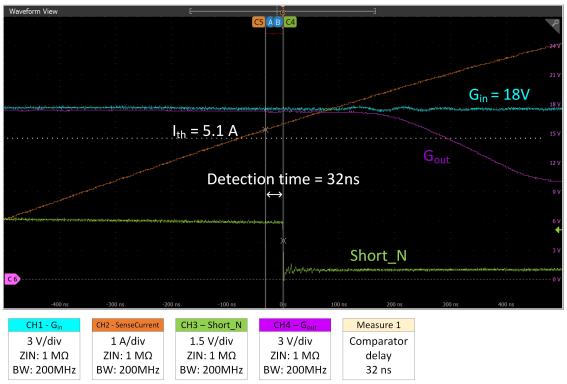

Fig. 6. Measured detection time during a short-circuit event

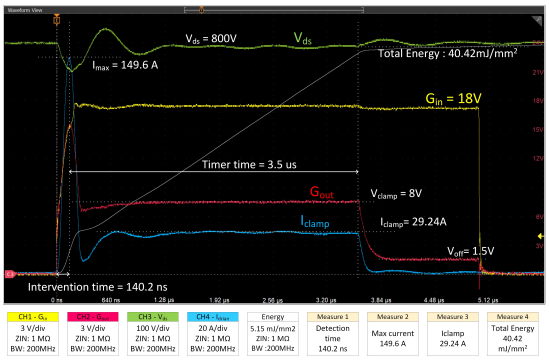

Fig. 7. Behavior of the proposed short-circuit protection, driving an 800-V, 80-mΩ SiC MOSFET with $V_{GS} = 18$ V

about 32 ns when the current in R_{sh} crosses the comparator threshold (detection time).

Fig. 7 shows the behavior of the proposed short-circuit protection, driving an 800-V, 80-mΩ SiC MOSFET with $V_{GS} = 18$ V. The short circuit is detected and the gate voltage is driven to about 8 V after 140.2 ns (intervention time), before turning off the switch after 3.5 µs. The drain current reaches almost 150 A in the detection phase (I_{max}) and it is reduced to about 30 A in the protection phase (I_{clamp}). Without any protection strategy, a short-circuit withstand time of 2 µs can only be achieved by driving the SiC MOSFET with $V_{GS} = 15$ V, at the expense of a larger on-resistance. Driving the SiC MOSFET with $V_{GS} = 18$ V to minimize the on-resistance would lead to a short-circuit withstand time of 1.5 µs, unacceptable in actual applications. With the proposed protection strategy, the overall withstand time with $V_{GS} = 18$ V becomes 4 µs, without any on-resistance derating.

V. Conclusions

Table I summarizes the performance of the proposed short-circuit protection strategy and compares it with the state-of-the-art. With respect to other sense-FET based solutions [2, 6], the proposed SiP achieves more than 10× shorter intervention time, it is more flexible, since it can also be used when a protection strategy at the system level is present, and does not require any additional circuitry nor pins. TMR-based solutions [4] achieve similar performance in terms of detection time, but require an additional isolated operational amplifier to sense the current. Improved desaturation methods [2], originally developed for Si-IGBT, achieve a significantly longer detection time and require a dedicated gate driver as well as high-voltage components. Protections able to achieve similar detection time are present in the literature [5], but they need more time to bring the SiC MOSFET into the safe operating region, as well as additional circuitry. Work in [6] presents a monolithically integrated short circuit protection, including a CMOS power stage to control the SiC MOSFET and an integrated shunt resistor to sense the fault situation. This solution occupies a wider area with respect to the proposed one and requires additional pins to achieve a slower reaction time.

TABLE I
Performance Summary and Comparison with the State-of-the-Art

	Protection method	Isolation	Integration level	Detection time [ns]	Intervention time [µs]
[2]	Desaturation	HV diode	PCB	1250	N/A
[3]	SenseFET/ Shunt	Isolated op-amp	PCB	1000	N/A
[4]	TMR	N/A	PCB	178	0.600
[5]	Gate current sensing	Digital signal isolator	PCB	50	0.352
[6]	SenseFET/ Integrated shunt	Not needed	Monolithic	720	1.890
This Work	SenseFET/ Integrated shunt	Not needed	SiP	32	0.140

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