280/250-GHz Amplifiers Based on Transformer-Embedded Over-Neutralization Technique for High-Speed Communication Application in 65-nm CMOS

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***Abstract*—This article presents a transformer-embedded over-neutralization (TEON) gain-boosting technique to overcome the severe gain and bandwidth limitations of amplifiers operating near transistor f_{max} in CMOS. This approach enables the amplifier to operate at the edge of unconditional stability ($K_f \geq 1$) to achieve the maximum gain, while simultaneously ensuring a conjugate input match and facilitating direct cascadability. To demonstrate the technique, two H-band PAs are implemented in standard 65-nm bulk CMOS. The 8- and 7-stage amplifiers, respectively, achieve peak gains of 28 dB and 22.1 dB, 3-dB bandwidths from 258 to 276 GHz and 213 to 255 GHz, saturated output powers (P_{sat}) of 2.1 dBm and 2.6 dBm, with gain-bandwidth products (GBWs) of 452 GHz and 533 GHz, supporting data rates of 110 Gb/s and 120 Gb/s with relative error vector magnitude (EVM_{rms}) of -21.04 dB and -20.95 dB in 32-QAM modulation measurements. The proposed amplifiers achieve the highest reported GBW among CMOS amplifiers in H-band (220-325 GHz) and demonstrate significant potential for high-speed H-band communication systems in CMOS.**

***Keywords*—amplifier, CMOS, gain-boosting technique, H-band, high gain-bandwidth product, THz.**

I. Introduction

The H-band (220-325 GHz) has emerged as a critical frequency range for next-generation (6G) applications, offering unparalleled advantages in high-speed communications, high-resolution imaging, and advanced radar systems [1]. This band is attractive due to its wide bandwidth, which allows for higher data rates and improved signal resolution. Additionally, the shorter wavelengths in the H-band enable more compact system designs and enhance the precision of imaging and radar technologies, making it a focus for future advancements in these fields.

Despite its potential, leveraging the H-band for these advanced applications presents challenges. CMOS amplifiers operating in this frequency range struggle with low gain and narrow bandwidth due to the limitations of maximum oscillating frequency (f_{max}), as well as increased losses in matching networks and severe parasitic effects at high frequencies. The G_{max}-core topology based on inductive embedding is widely employed in CMOS amplifiers operating above 200 GHz [2], [3], [4], [5], [6], as it enhances the gain at the target frequency. However, this topology requires large feedback inductors, leading to insufficient layout space when integrated into a transmitter. Moreover, the lack of DC-blocking capacitors leads to identical gate and drain voltages, which affects the gain, noise figure (NF), and linearity of the amplifier [5]. In [6], a 237-267-GHz 15-stage amplifier utilizing the dual-peak G_{max}-core topology with added DC-blocking capacitors achieves a 20-dB gain. This design allows for independent bias voltages, albeit at the expense of reduced single-stage gain. Additionally, the saturated output power (P_{sat}) of the single-way amplifier is reported as -3.4 dBm. Furthermore, [7] reports a 206-220-GHz three-stage amplifier using the over-neutralization technique, achieving a 15-dB gain. The amplifier based on neutralization topology with capacitive embedding achieves a wider bandwidth and a more compact structure, compared to the amplifier based on G_{max}-core topology with inductive embedding when embedding is performed at only one frequency point. However, lossy passive components limit the achievable gain of neutralization-based amplifiers at higher frequencies.

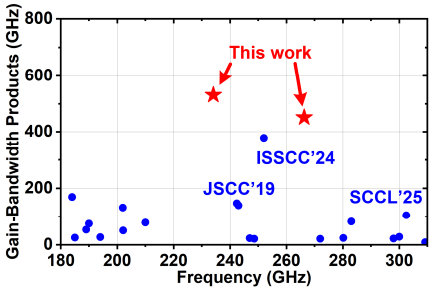


Fig. 1. Comparison of the proposed amplifiers with state-of-the-art CMOS amplifiers in the H-band.

In this work, we propose a transformer-embedded over-neutralization (TEON) gain-boosting technique to address this issue and design 256-281-GHz 8-stage and 213-255-GHz 7-stage amplifiers implemented in standard 65-nm bulk CMOS. The 8-stage amplifier achieves a measured peak gain of 28 dB and a 3-dB bandwidth from 258 to 276 GHz with a P_{sat} of 2.1 dBm, supporting a data rate of 110 Gb/s with a relative error vector magnitude (EVM_{rms}) of -21.04 dB under 32-QAM modulation. The other 7-stage wideband amplifier exhibits a peak gain of 22.1 dB and a 3-dB bandwidth from 213 to 255 GHz with a P_{sat} of 2.6 dBm, supporting a data rate of 120 Gb/s with an EVM_{rms} of -20.95 dB under 32-QAM modulation. The proposed amplifiers exhibit the highest reported gain-bandwidth products (GBWs) among CMOS amplifiers in H-band, as shown in Fig. 1. This work establishes a foundation for the future realization of highly integrated, wideband, and high-power-output CMOS THz front ends.

II. Gain-Boosting Techniques and Transistor Model Optimization

A. Transformer-Embedded Over-Neutralization Gain-Boosting Technique

Fig. 2 (a) illustrates the conventional over-neutralization technique [7]. With neutralization capacitors (C_n) of 6.2 fF and 14 μm transistors, the maximum available gain (MAG) of the amplifier core reaches 7.2 dB with a stability factor (K_f) = 1. However, in the H-band, passive components inevitably introduce high losses. The parasitic resistance (R_{MN}) of 5Ω in

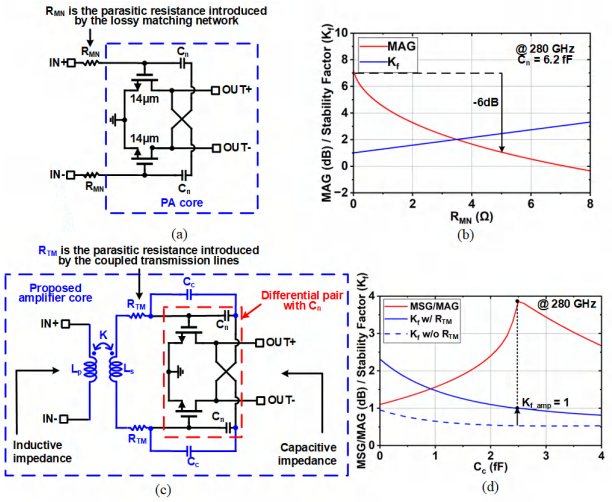


Fig. 2. (a) Conventional over-neutralization schematic and (b) its gain degradation due to R_{MN} at 280 GHz. (c) Proposed TEON technique schematic and (d) simulated gain/stability factor optimization versus C_c.

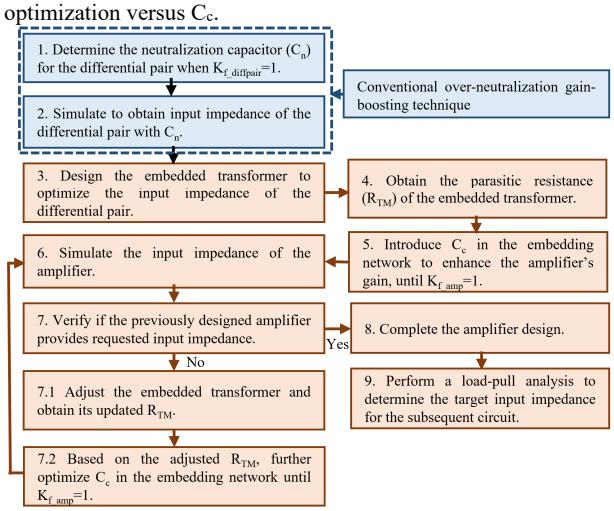


Fig. 3. Iterative design flow of the proposed transformer-embedded over-neutralization technique.

the lossy matching network significantly reduces the gain of each amplifier stage by 6 dB, as shown in Fig. 2 (b). The TEON technique is proposed to address this, as shown in Fig. 2(c). Following the introduction of a transformer for input pre-matching, a compensation capacitor (C_c) is incorporated into the differential pair to enhance positive feedback, thereby compensating for losses due to parasitic resistance (R_{TM}) in the lossy transformer and increasing the gain of each amplifier stage by 2.8 dB. This technique pushes MAG closer to the maximum stable gain (MSG), thereby improving gain while maintaining a wide bandwidth. Given that the transformer enhances both common-mode and differential-mode stability, the transformer is embedded into the amplifier core for co-design to achieve a 4-dB gain per stage, while simultaneously optimizing impedance matching for cascading and ensuring unconditional stability. Considering that the introduction of C_c causes variations in the amplifier's impedance, Fig. 3 illustrates the iterative optimization process for the embedded transformer and the C_c. To distinguish it from the conventional over-neutralization approach, steps corresponding to the traditional technique are marked with blue boxes. Furthermore, the common-mode and differential-mode

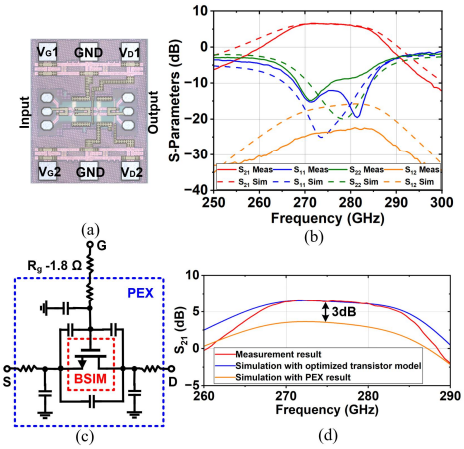


Fig. 4. (a) Die micrograph and (b) S-parameters of the two-stage test amplifier. (c) Proposed transistor model optimization and (d) comparison of S_{21} between measurements and simulations.

impedances at both the gate and drain terminals of each transistor are verified to ensure that their real parts remain positive across the entire frequency range, thereby guaranteeing unconditional stability of the amplifier. Besides, the proposed design allows independent biasing of the transistor's gate and drain, enabling the device to achieve optimal performance in a compact area.

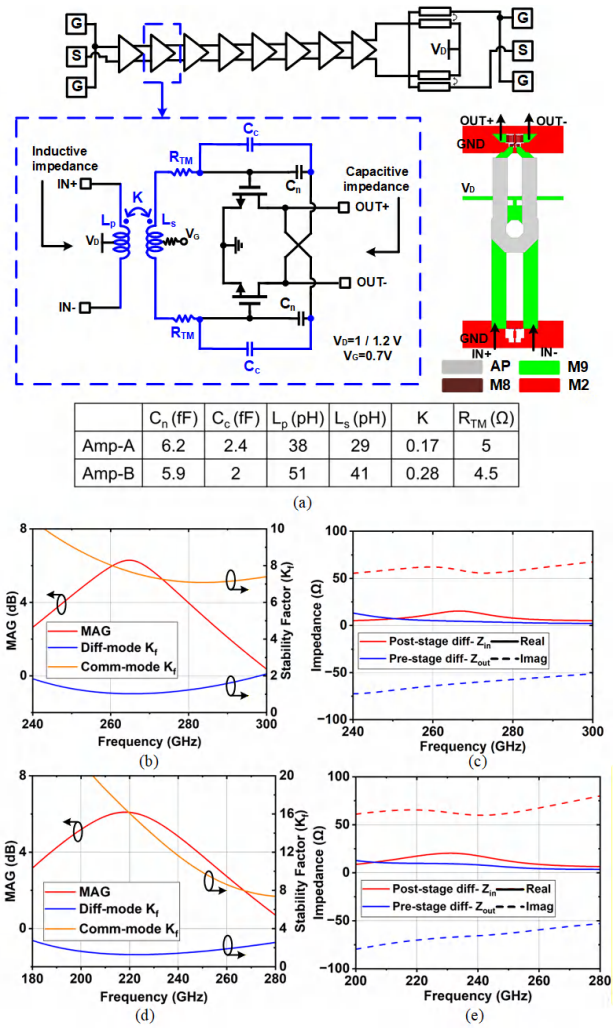
B. Transistor model optimization

A 262-286-GHz two-stage amplifier in 65-nm CMOS is designed and measured to optimize the transistor model in the H-band and validate the feasibility of the TEON technique. Figs. 4(a) and (b) show the chip and measured small-signal performance of the amplifier. A small-signal gain of 6.1 dB is achieved at 280 GHz, with unconditional stability across the entire frequency range. Based on these measurements, Fig. 4(c) displays the optimized transistor model. According to the parasitic extraction (PEX) results, the simulated small-signal gain is 3 dB lower than the measured results, with a discrepancy of 1.5 dB per stage. Consequently, in the optimized transistor model, the parasitic resistance at the gate is reduced by 1.8 Ω, aligning the simulated gain with the measured results across the bandwidth. This optimization helps prevent oscillations and frequency deviations in subsequent cascaded amplifier designs. The accuracy of the simulation with the optimized transistor model is further confirmed through small-signal measurements of the two subsequent amplifiers, demonstrating improved simulation accuracy for CMOS circuits operating in the H-band.

III. Design and Measurements of H-band Amplifiers

A. Design of H-band Amplifiers

Fig. 5(a) details the schematics and parameters of the proposed TEON-based Class-A amplifiers. The 256-281-GHz 8-stage amplifier (Amp-A) is designed for high gain, while the 213-255-GHz 7-stage amplifier (Amp-B) is optimized for wide bandwidth. The design parameters for the amplifier cores are detailed in Fig. 5(a). The simulated stage-level performance of the two designs is detailed in Fig. 5(b)–(e). As illustrated in Fig. 5(b) and (d), co-designing the amplifier stages with inter-stage transformers achieves 3-dB MAG bandwidths of 240–288 GHz for Amp-A and 180–260



	C_n (fF)	C_c (fF)	L_p (pH)	L_s (pH)	K	R_{TM} (Ω)
Amp-A	6.2	2.4	38	29	0.17	5
Amp-B	5.9	2	51	41	0.28	4.5

Fig. 5. (a) Schematics, transformer layout, and design parameters of the proposed 8-stage Amp-A and 7-stage Amp-B. Simulated stage-level MAG, stability factors, and differential impedances for (b)-(c) Amp-A and (d)-(e) Amp-B.

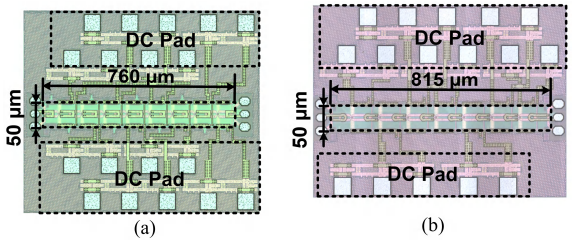


Fig. 6. Die micrographs of the prototype (a) 8-stage Amp-A and (b) 7-stage Amp-B, with active area dimensions indicated.

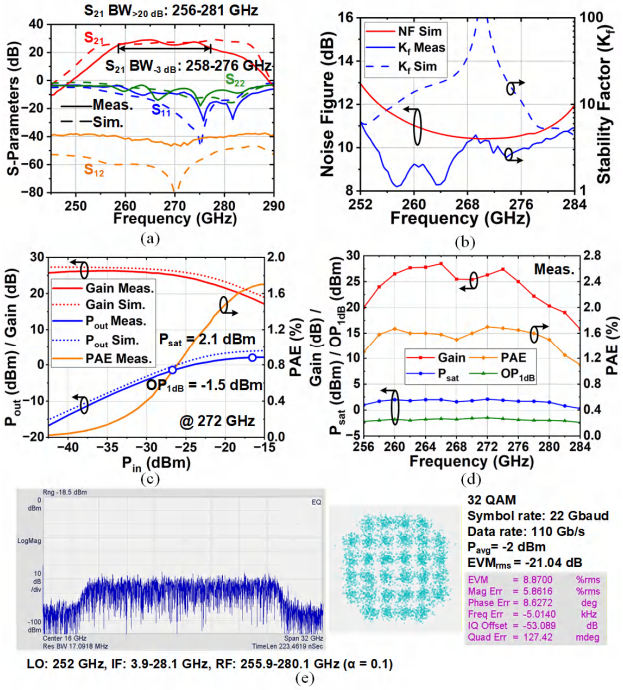


Fig. 7. Measured performance of Amp-A: (a) S-parameters, (b) K_f and simulated NF, (c) large-signal performance at 272 GHz, (d) P_{sat}, OP_{1dB}, and PAE versus frequency, (e) modulation performance with a 22-Gbaud 32-QAM signal.

GHz for Amp-B, respectively. Within these operational bands, unconditional stability is maintained for both common-mode and differential-mode configurations. Meanwhile, it features an inductive differential input impedance and a capacitive differential output impedance, shown in Fig. 5(c) and (e). As a result, it achieves conjugate matching within a wide frequency range and can be cascaded to enhance gain. The Metal 9 and AP layers are used to achieve low transformer inductances. The virtual ground point of the transformer provides access to the drain DC voltage of the amplifier. Fig. 6 presents the chip micrographs of Amp-A and Amp-B, and the respective active areas are 0.05 mm × 0.76 mm and 0.05 mm × 0.82 mm.

B. Measurement Results of the 256-281-GHz Amplifier

Fig. 7(a) presents the small-signal measurement results of the Amp-A, which exhibits a 3-dB gain (S_{21}) bandwidth of 258-276 GHz, with a peak gain of 28 dB and a GBW of 452 GHz. The bandwidth with a gain higher than 20 dB spans from 256 to 281 GHz. The amplifier is unconditionally stable across all frequencies, with a simulated NF of approximately 11 dB, as shown in Fig. 7(b). The discrepancy between the measured and simulated K_f is primarily attributed to degradation in measured S_{12}. This difference is caused by signal leakage between the input and output probes via spatial radiation and substrate coupling during on-wafer measurements, which reduces the port-to-port isolation compared to the ideal simulation environment.

In large-signal measurements, the amplifier achieves a P_{sat} of 2.1 dBm, a 1-dB compression of the output power (OP_{1dB}) of -1.5 dBm, and a power-added efficiency (PAE) of 1.7% at 272 GHz, shown in Fig. 7(c). Fig. 7(d) illustrates the measured P_{sat}, OP_{1dB}, and PAE versus frequency. To characterize the modulation performance, Fig. 7(e) presents the measurement results of the proposed amplifier using a single-carrier 32-QAM signal. At a symbol rate of 22 Gbaud, the amplifier achieves an average output power (P_{avg}) of -2 dBm and an EVM of -21.04 dB, supporting a data rate of 110 Gb/s.

C. Measurement Results of the 213-255-GHz Amplifier

Fig. 8(a) showcases the small-signal measurement results of the Amp-B. The peak S_{21} reaches 22.1 dB, with a 3-dB bandwidth spanning 213-255 GHz, yielding a GBW of 533 GHz. The amplifier maintains unconditional stability across the operating band, with a simulated NF of approximately 10.5 dB, as shown in Fig. 8(b). In large-signal measurements shown in Fig. 8(c) and (d), the amplifier achieves a P_{sat} of 2.6 dBm, an OP_{1dB} of -0.8 dBm, and a PAE of 1.9%. The

TABLE I PERFORMANCE COMPARISON WITH STATE-OF-THE-ART H-BAND AMPLIFIERS IN CMOS

	This work		[6] ISSCC'24	[2] JSSC'19	[3] JSSC'21		[8] JSSC'23	[5] MWTL'19	[9] MWTL'21	[4] TMTT'25		[10] JSSC'17
Technology	65-nm CMOS											
Topology	TEON		G_{max}-core									
Supply (V)	1.2	1.2	1	0.85	1	1	1	1	1.2	0.75	0.75	1
Gain (dB)	28	22.1	22*	13.9	18	15	26	21	12.6	18.2	9.3	9.2
Frequency (GHz)	258-276	213-255	237-267	227.5-257.2	247	272	243	298	248.6	280.2	309.2	257
3-dB BW (GHz)	18	42	30*	29.7	2.9	3.7	7	2*	5*	3*	3*	12.2
GBW(GHz)	452	533	378	147	23	21	140	22	21	24	9	35
Stage	8	7	15	4	2	2	6	16	3	3	3	4
P_{sat} (dBm)	2.1	2.6	-3.4	-3.3	0.09	-2.36	10.5 (4-way)	N/A	3.8	-10.4	-8.1	-3.9
OP_{1dB} (dBm)	-1.5	-0.8	-11.2	-5.1	-9.52	-10.18	7.7	-13	2.3	N/A	N/A	-8
PAE (%)	1.7	1.9	N/A	1.6	4.44	2.37	2.7	N/A	3.2	0.4	1.9	0.8
P_{dc} (mW)	92	85	38	23.8	21.5	21.5	407	35.4	62.4	12.3	6.6	27.6
Power Density (mW/mm^2) ***	42.63	44.39	0.95	8.68	7.5	5.23	10.79	N/A	12.83	0.42	2.35	2.9
Core Area (mm^2)	0.038	0.041	0.48	0.053	0.136**	0.111**	1.04**	0.39	0.187**	0.212**	0.066**	0.14

*Estimated from the figures. **Core area estimated according to chip photos, excluding RF and DC pads. *** Power Density = P_{sat} (mW)/Core Area(mm^2)

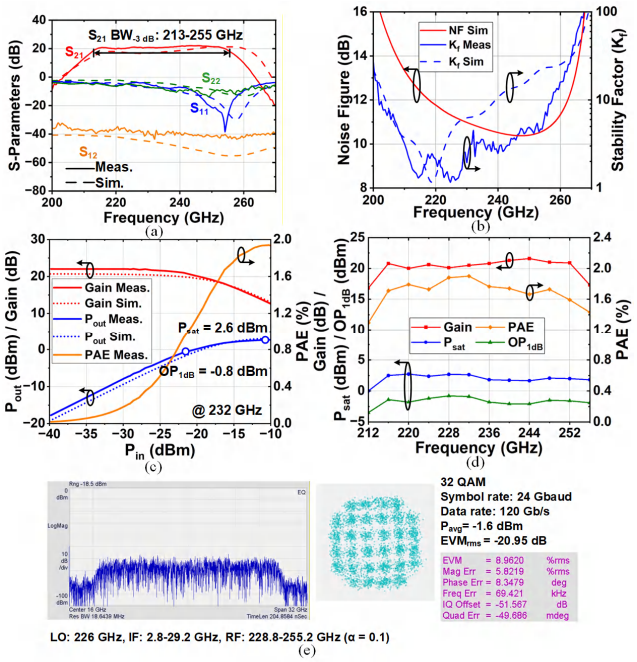


Fig. 8. Measured performance of Amp-B: (a) S-parameters, (b) K_f and simulated NF, (c) large-signal performance at 232 GHz, (d) P_{sat}, OP_{1dB}, and PAE versus frequency, (e) modulation performance with a 24-Gbaud 32-QAM signal.

proposed amplifier is characterized using a single-carrier 32-QAM modulation signal. At a symbol rate of 24 Gbaud, the amplifier achieves a P_{avg} of -1.6 dBm and an EVM of -20.95 dB, supporting a data rate of 120 Gb/s. These results demonstrate that the proposed amplifiers are well-suited for high-data-rate communication systems in the H-band.

IV. CONCLUSION

Table I summarizes the performance of state-of-the-art CMOS amplifiers in the H-band. The proposed amplifiers with the TEON technique demonstrate superior gain and bandwidth, the largest GBW, and competitive P_{sat} and OP_{1dB}, while occupying the most compact area and achieving the highest power density. Furthermore, both amplifiers are capable of supporting high-speed communication applications with data rates exceeding 100 Gb/s. These attributes underscore their considerable potential for high-speed communications, imaging, and radar applications in the H-band.

ACKNOWLEDGMENT

This work was supported by the Hong Kong Research Grants Council Collaborative Research Fund under Grant C1009-22G. Corresponding author: Zhicheng Lin.

REFERENCES

[1] S. Lee, S. Hara, T. Yoshida, S. Amakawa, R. Dong, A. Kasamatsu, J. Sato, and M. Fujishima, "An 80-Gb/s 300 GHz-band single-chip CMOS transceiver," *IEEE J. Solid-State Circuits,* vol. 54, no. 12, pp. 3577–3588, Dec. 2019.

[2] D. -W. Park, D. R. Utomo, B. H. Lam, S. -G. Lee and J. -P. Hong, "A 230–260-GHz Wideband and High-Gain Amplifier in 65-nm CMOS Based on Dual-Peak G_{max}-Core," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1613-1623, June 2019.

[3] D. -W. Park, D. R. Utomo, B. Yun, H. U. Mahmood, J. -P. Hong and S. -G. Lee, "Design of High-Gain Sub-THz Regenerative Amplifiers Based on Double-G_{max} Gain Boosting Technique," *IEEE J. Solid-State Circuits*, vol. 56, no. 11, pp. 3388-3398, Nov. 2021.

[4] B. Yun, D.-W. Park, and S.-G. Lee, "Design of sub-THz low-power and high-gain amplifiers based on double-embedded technique," *IEEE Trans. Microw. Theory Techn.*, vol. 73, no. 10, pp. 7558–7571, Oct. 2025.

[5] K. K. Tokgoz et al., "A 273–301-GHz Amplifier With 21-dB Peak Gain in 65-nm Standard Bulk CMOS," *IEEE Microw. Wireless Technol. Lett.*, vol. 29, no. 5, pp. 342-344, May 2019.

[6] C. Wang et al., "24.3 A 236-to-266GHz 4-Element Amplifier-Last Phased-Array Transmitter in 65nm CMOS," *in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2024, pp. 415-417.

[7] Z. Wang, P. -Y. Chiang, P. Nazari, C. -C. Wang, Z. Chen and P. Heydari, "A CMOS 210-GHz Fundamental Transceiver With OOK Modulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 564-580, March 2014.

[8] B. Yun, D.-W. Park, W.-J. Choi, H. U. Mahmood, and S.-G. Lee, "A 250-GHz 12.6-dB gain and 3.8-dBm Psat power amplifier in 65-nm CMOS adopting dual-shunt elements based Gmax-core," *IEEE Microw. Wireless Compon. Lett.*, vol. 31, no. 3, pp. 292–295, Mar. 2021.

[9] B. Yun, D.-W. Park, and S.-G. Lee, "H-band power amplifiers in 65-nm CMOS by adopting output power maximized Gmax-core and transmission line-based zero-degree power combining networks," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3089–3102, Nov. 2023.

[10] H. Bameri and O. Momeni, "A high-gain mm-wave amplifier design: An analytical approach to power gain boosting," *IEEE J. Solid-State Circuits*, vol. 52, no. 2, pp. 357–370, Feb. 2017.