A 92.3%-Efficiency 12V-to-1V HOT-12 Converter: Reframing Hybrid Design via the Dual-Output SC-Driven Parameterized HOT-X Framework

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***Abstract*—This paper presents a hybrid DC-DC converter optimized for 12V-to-1V conversion, synthesized from the proposed HOT-X design framework. Based on a parameterized dual-output SC model, the framework systematically derives the best-fit topology for a target inductor-current fraction and voltage conversion ratio (VCR = 1/X), enabling both high efficiency and power density. Fabricated in 180nm BCD, the HOT-12 converter chip achieves 92.3% peak efficiency with a 5.5mm^3 passive volume and maintains 82.8% at a current density of 0.55A/mm^3.**

***Keywords*—DC-DC converter, dual-output switched-capacitor (DO-SC), HOT-X framework, hybrid design model, inductor current reduction, point-of-load (PoL), voltage conversion ratio (VCR)**

I. Introduction

Efficiency and power density are two of the most critical figures of merit for modern DC-DC converters. However, the purely inductive buck converter struggles to maximize both metrics simultaneously; shrinking the inductor volume inevitably raises its DC resistance (DCR), degrading efficiency. Hybrid converters—inductive buck stages augmented by a switched-capacitor (SC) network forming a parallel current path—circumvent this trade-off [1]–[7]. By sharing the load current (I_{Load}) between the inductor and the flying capacitors, the inductor carries only a fraction of I_{Load}. This allows for inductor miniaturization (and higher DCR) with minimal efficiency penalty. While many hybrid converters [1]–[11] have achieved strong results, their design rationale often relies on topology-specific heuristics, making it difficult to distill systematic guidelines when re-targeting new specifications. A prior study [2] attempted to systematize hybrid design but was limited by solely targeting a desired duty ratio (D) for a given voltage-conversion ratio (VCR).

This paper presents **HOT-X** (**H**ybrid converter **O**ptimal at a **T**arget VCR of 1/**X**), a parameterized design framework that synthesizes hybrid topologies by formalizing SC charge distribution parameters (α and β). The proposed HOT-X design methodology is validated via a HOT-12 converter chip aimed at high-power-density 12V-to-1V point-of-load (PoL) applications.

II. HOT-X Framework via DO-SC-driven Hybrid Model

A. Dual-Output (DO)-SC-driven Hybrid Model

Fig. 1 shows the proposed generic hybrid-design model that

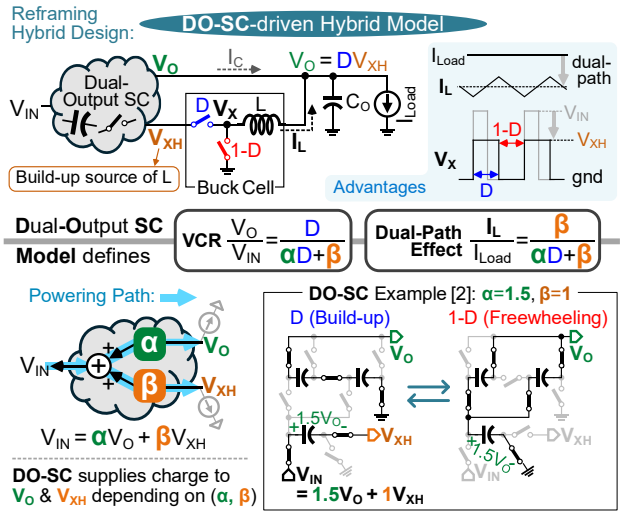


Fig. 1. Dual-output (DO)-SC-driven generic hybrid-design model.

underpins HOT-X. A dual-output SC (DO-SC) stage converts the input (V_{IN}) into two outputs, V_O and V_{XH}, governed by the weighted-sum relation:

$$V_{IN} = \alpha V_O + \beta V_{XH} \tag{1}$$

An inductive buck cell, controlled by the duty-cycle ratio (D), is interposed between V_{XH} and V_O, resulting in:

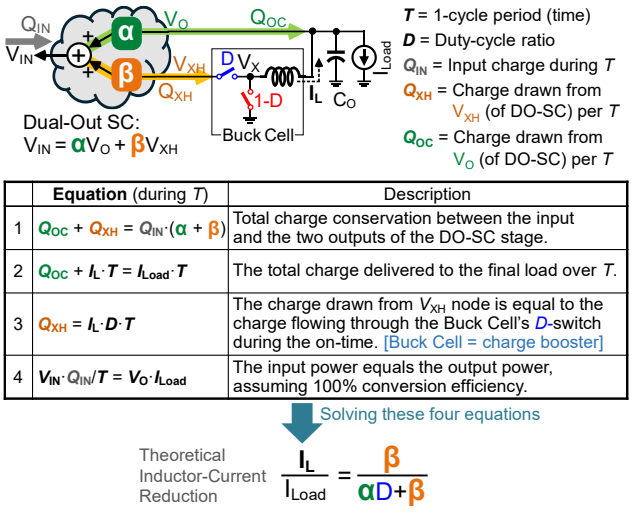
$$V_O = D \cdot V_{XH} \tag{2}$$

Combining (1) and (2) yields the VCR formular:

$$\mathrm{VCR} = V_O/V_{IN} = D/(\alpha D + \beta) \tag{3}$$

Magnetizing the inductor with a reduced $V_{XH} = (V_{IN} - \alpha V_O)/\beta$ (versus full V_{IN} in a classical buck) lowers the required inductance. Also, the DO-SC defines the node voltages and sources charge to both V_{XH} and V_O. Charge supplied to V_{XH} is multiplied by $1/D$ via the buck cell, appearing at V_O as the inductive current I_L, while direct charge delivery to V_O forms the capacitive current I_C. This load-sharing reduces I_L demand, relaxing DCR constraints and shrinking the inductor volume.

Fig. 2 presents the core insight of the DO-SC-oriented model: abstracting the hybrid converter into a unified charge-flow network. This model simplifies complex switching operations

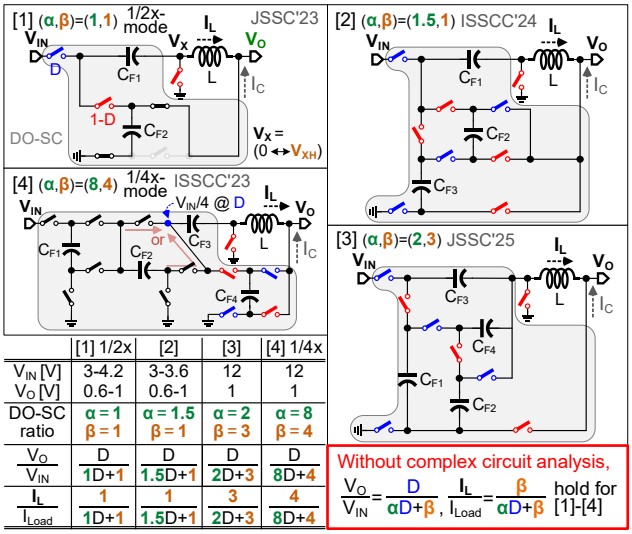


	Equation (during T)	Description
1	$Q_{OC} + Q_{XH} = Q_{IN}\cdot(\alpha + \beta)$	Total charge conservation between the input and the two outputs of the DO-SC stage.
2	$Q_{OC} + I_L\cdot T = I_{Load}\cdot T$	The total charge delivered to the final load over T.
3	$Q_{XH} = I_L\cdot D\cdot T$	The charge drawn from V_{XH} node is equal to the charge flowing through the Buck Cell's D-switch during the on-time. [Buck Cell = charge booster]
4	$V_{IN}\cdot Q_{IN}/T = V_O\cdot I_{Load}$	The input power equals the output power, assuming 100% conversion efficiency.

Solving these four equations

Theoretical Inductor-Current Reduction $\frac{I_L}{I_{Load}} = \frac{\beta}{\alpha D+\beta}$

Fig. 2. Charge-flow abstraction of the hybrid converter via the DO-SC-oriented model and derivation of the inductor-current fraction (I_L/I_{Load}).



	[1] 1/2x	[2]	[3]	[4] 1/4x
V_{IN} [V]	3-4.2	3-3.6	12	12
V_O [V]	0.6-1	0.6-1	1	1
DO-SC ratio	α = 1 β = 1	α = 1.5 β = 1	α = 2 β = 3	α = 8 β = 4
$\frac{V_O}{V_{IN}}$	$\frac{D}{1D+1}$	$\frac{D}{1.5D+1}$	$\frac{D}{2D+3}$	$\frac{D}{8D+4}$
$\frac{I_L}{I_{Load}}$	$\frac{1}{1D+1}$	$\frac{1}{1.5D+1}$	$\frac{3}{2D+3}$	$\frac{4}{8D+4}$

Fig. 3. Re-interpretation of existing dual-path hybrid converters via the lens of the proposed DO-SC-driven hybrid model.

into a charge-conservation problem. Here, the inductive buck cell acts as a charge booster (gain: $1/D$) integrated into the DO-SC's nodal charge distribution. By solving charge (Q)-relations, the inductor-current fraction is derived as:

$$I_L/I_{Load} = \beta/(\alpha D + \beta) \quad (4)$$

Since VCR (3) and I_L-reduction (4) are governed by (α, β), the design process is streamlined to parameter selection and DO-SC synthesis. Elevating (α, β) to first-class variables replaces ad-hoc intuition with a systematic methodology. As the DO-SC deterministically hard-charges its network to set V_O and V_{XH}, the flying capacitors (CFs) do not rely on I_L, eliminating the charge-balance constraint of I_L-cycled hybrid converters [9]–[11].

Fig. 3 reinterprets existing dual-path-structured hybrids [1]–[4] via the lens of the DO-SC-oriented model; appropriate (α, β)

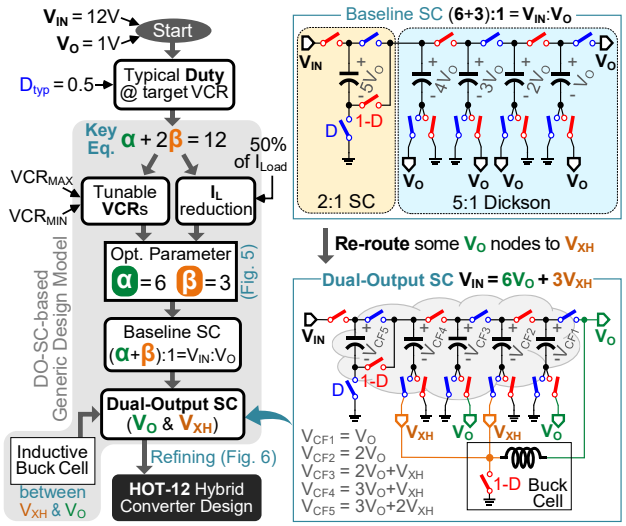


Fig. 4. Parameterized HOT-X design framework for deriving a DO-SC-based hybrid converter topology optimized at VCR = 1/X.

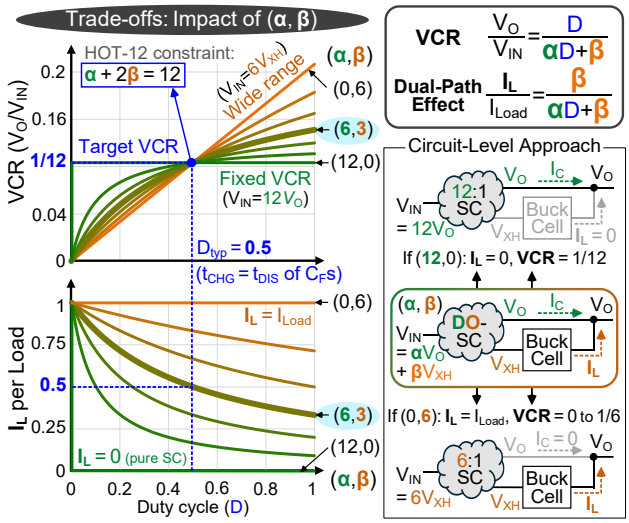


Fig. 5. Trade-off analysis: Impact of (α, β) parameters on tunable VCR range and I_L-reduction, subject to HOT-12 design constraint.

parameterization recovers their theoretical VCR and I_L-reduction, offering a unified view of these successful designs.

B. HOT-X Design Framework

Fig. 4 shows the HOT-X framework, demonstrated for a 12V-to-1V converter (HOT-12). The design process begins by establishing the nominal operating point: a VCR of 1/12 at D_{typ} = 0.5. Centering D_{typ} at 0.5 offers two benefits: symmetric D headroom for rapid load-step recovery and equalized CF charge/discharge intervals that minimize capacitive RMS current [2], [7], [8]. Applying the VCR formula (3) with these target values yields the central constraint: $\alpha + 2\beta = 12$, defining a family of (α, β) pairs with distinct trade-offs (Fig. 5). Selecting (α, β) = (12, 0) collapses the model into a fixed-ratio 12:1 SC converter ($V_{IN} = 12V_O$). Conversely, (α, β) = (0, 6) configures a

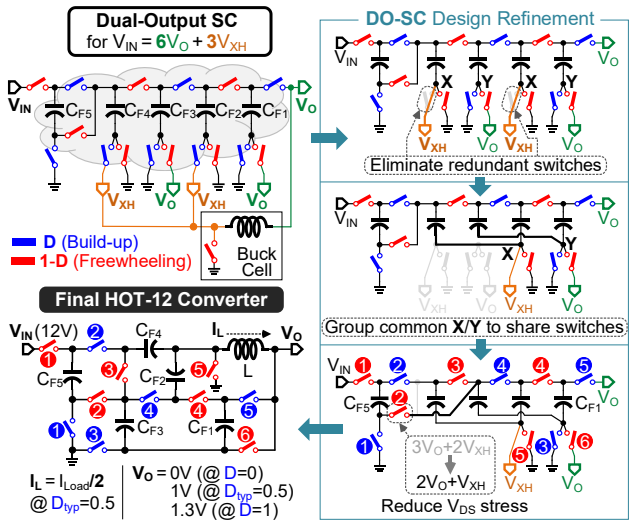


Fig. 6. Design refinement flow for the HOT-12 hybrid converter.

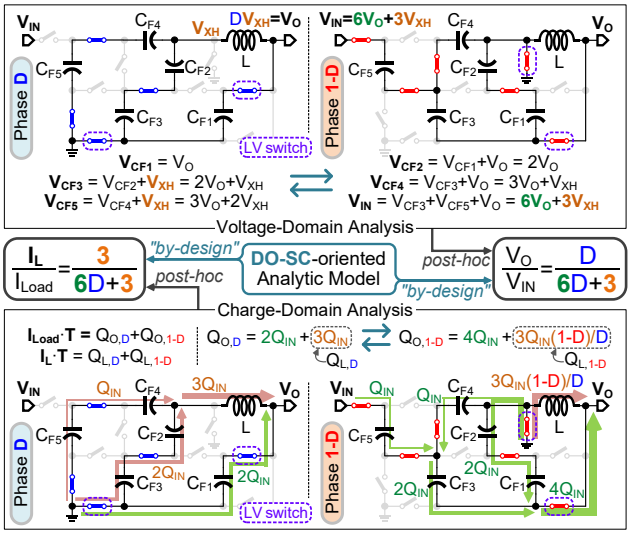


Fig. 7. Operation and analysis of the HOT-12 hybrid converter.

cascaded 6:1 SC → buck stage (i.e., $V_{IN} = 6V_{XH} = 6V_O/D$), which maximizes the VCR range but negates the I_L-reduction benefit ($I_C = 0$). For this HOT-12 design, we select $\alpha = 6$ and $\beta = 3$ to strike a deliberate balance; this ensures a practical VCR-tunable range ($V_O = 0$ to 1.3V) while achieving significant I_L-reduction at the target VCR ($I_L = 50\%$ of I_{Load} at $D_{typ} = 0.5$).

Following (α, β) selection, the DO-SC stage for $\alpha = 6$ and $\beta = 3$ is synthesized by transforming a baseline 9:1 [$= (\alpha+\beta):1 = V_{IN}:V_O$] single-output SC (Fig. 4, top-right). This baseline—efficiently realized as a 2:1 and 5:1 Dickson cascade—is converted into a dual-output SC by re-assigning selected V_O nodes to the V_{XH} rail to satisfy "$V_{IN} = 6V_O + 3V_{XH}$" (Fig. 4, bottom-right). Finally, an inductive buck cell is interposed between the DO-SC's V_{XH} and V_O nodes.

Fig. 6 shows the refinement flow of the synthesized DO-SC. First, redundant switches are removed by shorting the X-node to the inductor's left terminal, as both remain at ground during the (1–D) phase. Next, grouping switches at common X and Y nodes lowers both the switch count and gate-drive complexity. Finally, the V_{DS} stress on a switch is reduced by reconfiguring the C_{F5} bottom-plate connection without impacting operation. These refinements yield the final HOT-12 converter design.

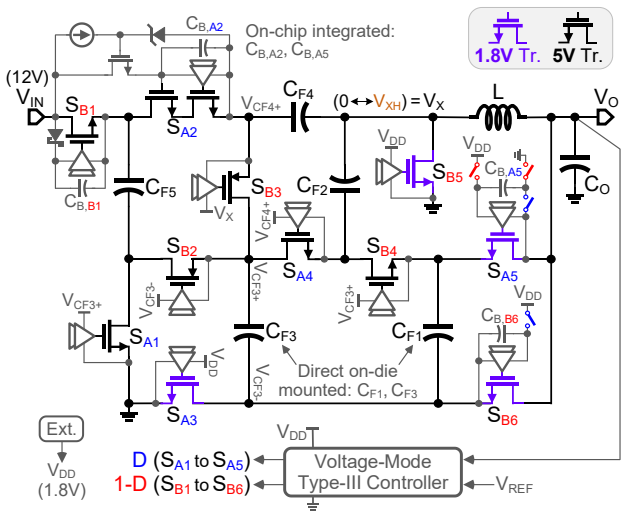
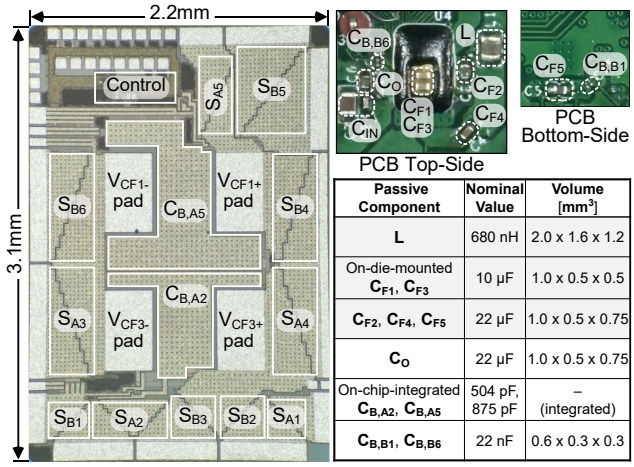


Fig. 8. Circuit-level implementation of the HOT-12 hybrid converter.



Passive Component	Nominal Value	Volume [mm³]
L	680 nH	2.0 x 1.6 x 1.2
On-die-mounted C_{F1}, C_{F3}	10 µF	1.0 x 0.5 x 0.5
C_{F2}, C_{F4}, C_{F5}	22 µF	1.0 x 0.5 x 0.75
C_O	22 µF	1.0 x 0.5 x 0.75
On-chip-integrated $C_{B,A2}$, $C_{B,A5}$	504 pF, 875 pF	– (integrated)
$C_{B,B1}$, $C_{B,B6}$	22 nF	0.6 x 0.3 x 0.3

Fig. 9. Die micrograph, test PCB, and details of the components used.

III. Operation & Implementation of HOT-12 Converter

Fig. 7 shows the HOT-12 converter operation. In the voltage-domain analysis (top), the CF voltages are established during the D and (1–D) phases to satisfy the steady-state condition. The resulting VCR formula (3) confirms that the converter achieves a 12:1 step-down ratio at $D_{typ} = 0.5$. Consistent with the DO-SC-based model, the charge-domain analysis (bottom) demonstrates that the total charge supplied to V_O is composed of $3Q_{IN}/D$ (via L-path) and $6Q_{IN}$ (via C-path); consequently, at $D_{typ} = 0.5$, the inductor is only required to carry 50% of the total I_{Load}, validating the I_L-reduction formula (4).

Table I. Performance Summary in Comparison with Prior Works

	ISSCC'23 [4]	ISSCC'24[e] [6]	JSSC'25 [3]	ISSCC'25[d] [9]	ISSCC'25 [10]	This Work
Process	0.18μm BCD	0.18μm BCD	0.18μm BCD	0.18μm BCD	0.18μm BCD	**0.18μm BCD**
Topology	ReSC-PL	CCP-HB	DPSC	HOOP	SI	**HOT-12**
Input Voltage (V_{IN})	12V	12V	9–16V	12V	12V	**12V**
Output Voltage (V_O)	0.6–1.2V	1–1.8V	0.6–1.6V	1–1.2V	1–1.8V	**0.6–1V**
Max. Load Current	5A	5A	5A	5A	6A	**4A**
SW Freq. (f_{SW})	0.8MHz	1MHz	1MHz	1MHz	2MHz	**1MHz**
Components	1L 4C 12SW[b]	1L 4C 8SW	1L 4C 8SW	2L 2C 7SW	3L 6C 15SW	**1L 5C 11SW**
Inductor (DCR)	1μH (N.R.)	1μH (57mΩ)	0.68μH (N.R.)	2 x 1μH (48mΩ)	3 x 0.6μH (29mΩ)	**0.68μH (33mΩ)**
I_L-Reduction[g] @VCR=1/12	50%	54%	17%	0% (N = 2)	0% (N = 3)	**50%**
Flying Capacitor	2 x 22μF, 2 x 10μF	3 x 10μF, 1 x 22μF	2 x 20μF, 2 x 10μF	2 x 10μF	6 x 1μF[f]	**2 x 10μF, 3 x 22μF**
Output Capacitor	100μF	22μF	22μF	2 x 10μF	10μF	**22μF**
Peak Efficiency @ V_{IN}=12V	91.8% @ V_O=1V	94.7% @ V_O=1.6V	94.5% @ V_O=1.2V	90.2% @ V_O=1.2V	92.9% @ V_O=1.8V	**92.3% @ V_O=1V**
Peak Efficiency @ V_{IN}=12V & VCR=1/12	91.8% @ I_{Load}=1A	91.1% @ I_{Load}=1.2A[c]	93.4% @ I_{Load}=0.8A	89%[c] @ I_{Load}=1A	91.7% @ I_{Load}=2A	**92.3% @ I_{Load}=0.7A**
Die Area	8.88mm^2	5mm^2	3.86mm^2	4.6mm^2	6mm^2	**6.82mm^2**
Total Passive Volume[a]	14.3mm^3	7.3mm^3	29.8mm^3	8.2mm^3	7.4mm^3	**5.5mm^3**

[a] Counts flying-capacitors & inductors, [b] Excluding parasitic inductor, [c] Estimated from figure, [d] 1-chip version, [e] Plan B (compact), [f] Effective value, [g] Theoretical I_L reduction = (I_{Load}/N – I_L)/(I_{Load}/N) [%] (N = # of inductors)

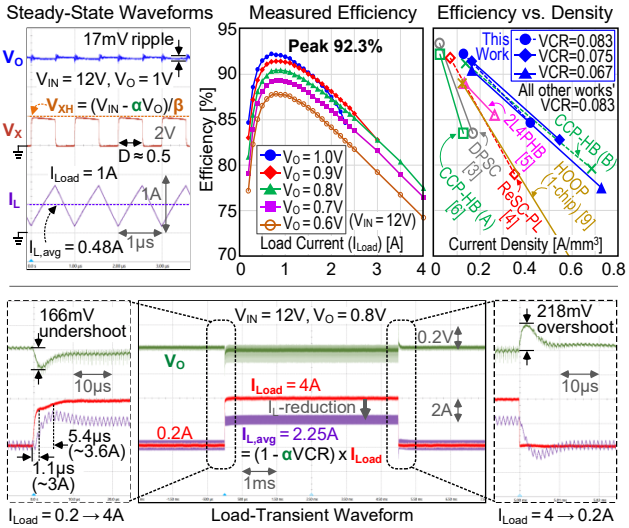


Fig. 10. Measurement results with a total passive volume of 5.5mm^3.

Fig. 8 details the circuit implementation. All switches utilize transistors rated below 5V for V_{IN} = 12V; specifically, high-current switches use low-R_{ON} 1.8V devices. C_{F1} and C_{F3}, which deliver charge directly to V_O, are vertical on-die-mounted capacitors. CF plate voltages are reused as bootstrap sources for gate drivers. This strategy minimizes complexity, requiring only 4 bootstrap capacitors (2 internal, 2 external) for all 11 switches.

IV. Measurement Results

The HOT-12 chip was fabricated in a 180nm BCD and tested with a 680nH inductor (33mΩ DCR) and flying capacitors, occupying a total passive volume of 5.5mm^3 (Fig. 9). Fig. 10 presents the measurement results. Steady-state waveforms were captured at V_{IN} = 12V, V_O = 1V, and I_{Load} = 1A. The V_X node toggles between 0V and V_{XH}, where the measured V_{XH} (≈ 2V) closely follows V_{XH} = (V_{IN} – αV_O)/β. The average inductor current ($I_{L,avg}$) was measured at 0.48A—roughly 50% of I_{Load}. A peak efficiency of 92.3% is achieved at I_{Load} = 0.7A. Moreover, the HOT-12 chip maintains 82.8% efficiency at a current density of 0.55A/mm^3 and 77.5% at 0.73A/mm^3. During load transients (0.2A ↔ 4A) with C_O = 22μF, V_O exhibits an under/overshoot of –166/+218mV. Table I provides a performance comparison, highlighting this work's leading efficiency (92.3% at VCR = 1/12) and its smallest total passive volume (5.5mm^3).

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