A 10-bit 200 MS/s SAR ADC with an Embedded 3–6 GHz RF Switching Mixer and Filter

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***Abstract*—This paper presents a 10-bit 200 MS/s two-times time-interleaved SAR ADC with a 3–6 GHz RF switching mixer and FIR filter embedded in its sampling operation, acting as the front-end for a RISC-V processor system. The architecture samples using both reference clock edges to achieve a 6–12 GHz sampling frequency from a 3–6 GHz LO reference clock signal. The duty cycle dependency of the sampling operation is alleviated by sample averaging. This forms a decimating low-pass FIR filter that reduces noise and interference. The filter is designed to be reconfigurable with 16–32 taps in order to maintain ADC sampling rate of 200 MS/s across the LO frequency range. The ADC is fabricated in 22 nm FDSOI process, and achieves more than 7.1 effective number of bits while consuming 8.01–12.6 mW of power downconverting from 3–6 GHz carrier frequencies.**

***Index Terms*—analog-to-digital converter, downconversion, embedded filter, embedded mixer, successive approximation register**

I. Introduction

TO REDUCE the area consumption and improve system energy efficiency, multiple analog functions can be performed by sharing the common circuit structures. Such circuit re-use has been applied in successive approximation register (SAR) analog-to-digital converters (ADCs), where the signal is sampled directly to the capacitive digital-to-analog converter (CDAC), eliminating the need for a separate sampling capacitor [1]. To further extend the re-use of the sampling capacitor, it has been used to embed filtering function to SAR ADCs [2]–[7], alleviating receiver front-end filter requirements.

As depicted in Fig. 1a, a FIR filter can be embedded by performing selective sampling to different capacitors using multiple parallel reconfigurable switches [2]. This reduces the capacitive load of the buffer amplifier driving the sampling capacitors and alleviates the pre-ADC filtering specification with minimal area overhead. Fig. 1b depicts an alternative sampling structure, where the filter response is improved at the cost of effective signal bandwidth using an additional capacitor to implement an IIR filter after the FIR filter [3]–[6]. A SAR ADC with embedded FIR filtering and downconversion has also been studied [7]. In the architecture, the input signal is subsampled to an intermediate frequency (IF), and then downconverted using a variable reference voltage [8].

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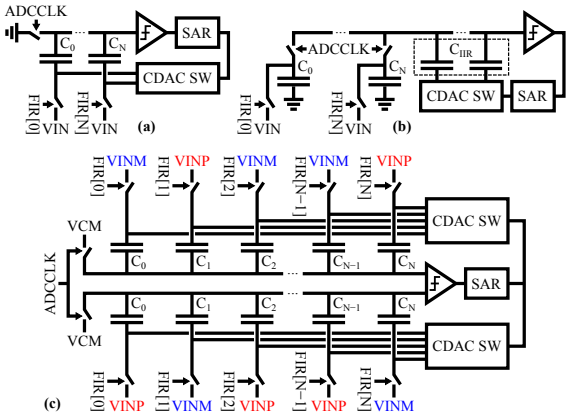

Fig. 1: SAR ADCs with embedded (a) FIR (b) FIR and IIR (c) switching mixer and FIR filter (this work).

This work presents a 10-bit two-times time-interleaved 200 MS/s SAR ADC with an embedded 3–6 GHz RF switching mixer and a decimating FIR filter, which further alleviates frequency selectivity requirements of a receiver front-end. The converter is designed as an A/D front-end for a RISC-V processor system. As shown in Fig. 1c, the downconversion is performed by alternating the input polarity and sampling to different capacitors with 6–12 GHz frequency.

In order to reduce system power consumption, both edges of LO clock signal are used for sampling, making the sampling prone to duty cycle errors that may cause spectral degradation [9]. In this work, the embedded FIR filtering operation also alleviates these errors by sample averaging. The decimating FIR filter is designed to be reconfigurable to maintain ADC output sample rate of 200 MS/s.

The downconverting and filtering ADC is fabricated in 22 nm FDSOI process and measured to achieve SNDR of over 44.6 dB across the carrier frequency range of 3–6 GHz with ADC output sample rate of 200 MS/s. The downconverting ADC system consumes 8.01 and 12.6 mW at 3 GHz and 6 GHz carrier frequencies respectively. To the authors' knowledge, the ADC is the first SAR with embedded zero-IF downconversion, and operates with the highest filter sampling

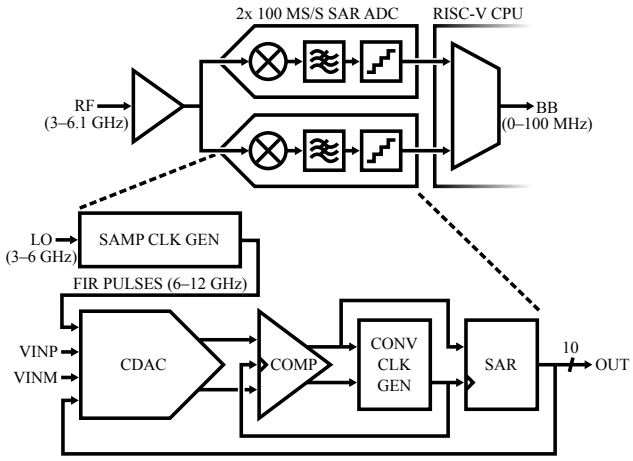

Fig. 2: Block diagram of the downconverting and filtering two-times time-interleaved SAR ADC.

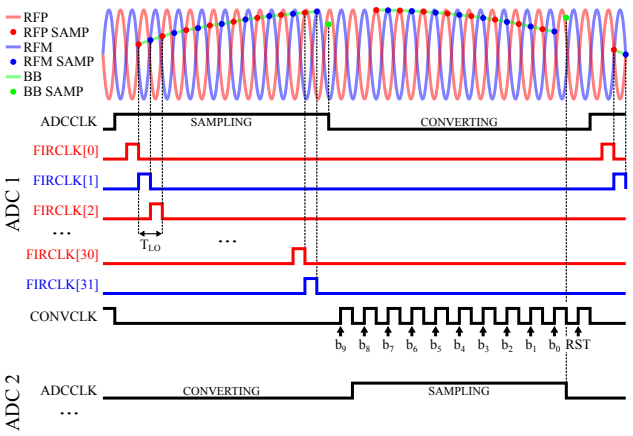

Fig. 3: Timing of the time-interleaved downconverting and filtering SAR ADC.

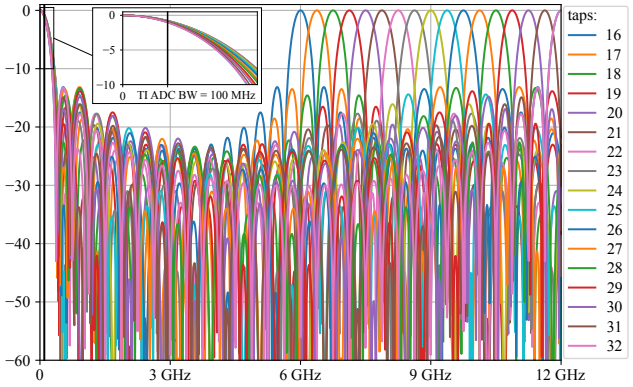

Fig. 4: Theoretical responses of the embedded FIR filter in different configurations.

rate of all of the published filtering SAR ADCs.

The paper is structured as follows. Section II introduces the SAR ADC with filtering and downconversion embedded in the sampling operation. Section III presents the measurement results of the fabricated prototype. Finally, Section IV concludes the paper.

II. The Downconverting and Filtering ADC

Fig. 2 shows the block diagram of the implemented downconverting and filtering two-times time-interleaved SAR ADC. It has a common input buffer, two unit ADCs that both perform the filtering and downconversion individually, and a RISC-V microprocessor system that captures and processes the ADC data. The input buffer is common for the unit ADCs to minimize system power consumption, to reduce inter-channel mismatches, and to provide a consistent load as the ADCs operate in opposite phases.

The downconversion and filtering are performed simultaneously in the sampler, as depicted in Fig. 1c. There is no separate mixer or filter circuitry inside the ADC. Splitting the sampling capacitor between the FIR units also alleviates the input buffer power consumption, as it has to drive only a fraction (C_{tot}/N_{taps}) of the total sampling capacitance at the cost of increased parasitics due to more complicated routing and parallel samplers.

Fig. 3 presents the timing of the time-interleaved ADC. The downconversion is performed by taking samples at twice the carrier frequency and inverting every other sample, as in a switching mixer. The ADC performs filtering by weight-averaging RF samples before quantization to form a 16–32 tap reconfigurable analog FIR filter. Furthermore, in order to reduce total power consumption of the system, both edges of the LO are used in the sampling, and therefore the LO and carrier frequencies are the same. In such dual-edge sampling, the duty cycle error may cause non-linearity [9]. In this configuration, the adverse effects are alleviated by averaging samples (FIR filtering), mapping the deviations from the desired duty cycle to gain and phase error [10] that can be calibrated [11].

Fig. 4 depicts the filter responses in different configurations, and the worst-case and average attenuations are listed in Table I. The FIR taps are realized by dividing the CDAC to 32 sample-and-hold units, each comprising a bootstrapped sampling switch and sampling capacitor. The samplers, visualized in Fig. 1c, are controlled using FIRCLK pulses while the ADCCLK is high, after which their samples are combined to form a filtered baseband (BB) sample. The reconfigurability to 16–32 taps is achieved by having digital controls to set whether some samples are taken to two sampler units. The filter order is tuned according to the LO frequency such that the ADC sampling and conversion times remain constant regardless of LO, as long as LO is between 3 and 6 GHz, corresponding to the minimum and maximum number of taps, respectively.

The downconverting and filtering ADC comprises typical SAR ADC components, i.e. clock generators, bootstrapped switches, capacitive DAC, StrongARM comparator, and SAR logic. The SAR conversion clock, CONVCLK, is asynchronous and generated from the comparator output (CONV

TABLE I: FIR filter coefficients and intended LO frequencies.

f_{LO} [GHz]	taps	coefficients	min. [dB]	avg. [dB]
3.0000	16	[2,2,2,2,2,2,2,2,2,2,2,2,2,2,2,2]/32	-13.2	-23.4
3.1875	17	[1,2,2,2,2,2,2,2,2,2,2,2,2,2,2,2,1]/32	-13.5	-26.3
3.3750	18	[1,1,2,2,2,2,2,2,2,2,2,2,2,2,2,1,1]/32	-14.6	-27.5
3.5625	19	[1,1,1,2,2,2,2,2,2,2,2,2,2,2,1,1,1]/32	-16.5	-28.3
3.7500	20	[1,1,1,1,2,2,2,2,2,2,2,2,2,2,1,1,1,1]/32	-19.6	-28.5
3.9375	21	[1,1,1,1,1,2,2,2,2,2,2,2,2,2,1,1,1,1,1]/32	-19.7	-28.8
4.1250	22	[1,1,1,1,1,1,2,2,2,2,2,2,2,2,2,1,1,1,1,1,1]/32	-17.7	-28.4
4.3125	23	[1,1,1,1,1,1,1,2,2,2,2,2,2,2,2,2,1,1,1,1,1,1,1]/32	-17.7	-28.0
4.5000	24	[1,1,1,1,1,1,1,1,2,2,2,2,2,2,2,2,1,1,1,1,1,1,1,1]/32	-16.1	-27.1
4.6875	25	[1,1,1,1,1,1,1,1,1,2,2,2,2,2,2,2,2,1,1,1,1,1,1,1,1]/32	-14.4	-27.1
4.8750	26	[1,1,1,1,1,1,1,1,1,1,2,2,2,2,2,2,2,1,1,1,1,1,1,1,1,1]/32	-13.5	-26.8
5.0625	27	[1,1,1,1,1,1,1,1,1,1,1,2,2,2,2,2,2,2,1,1,1,1,1,1,1,1,1]/32	-13.2	-26.6
5.2500	28	[1,1,1,1,1,1,1,1,1,1,1,1,2,2,2,2,2,1,1,1,1,1,1,1,1,1,1,1]/32	-13.3	-26.4
5.4375	29	[1,1,1,1,1,1,1,1,1,1,1,1,1,2,2,2,2,1,1,1,1,1,1,1,1,1,1,1,1]/32	-13.9	-26.4
5.6250	30	[1,1,1,1,1,1,1,1,1,1,1,1,1,1,2,2,1,1,1,1,1,1,1,1,1,1,1,1,1,1]/32	-14.8	-26.4
5.8125	31	[1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,2,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1]/32	-14.9	-26.6
6.0000	32	[1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1,1]/32	-13.2	-27.7

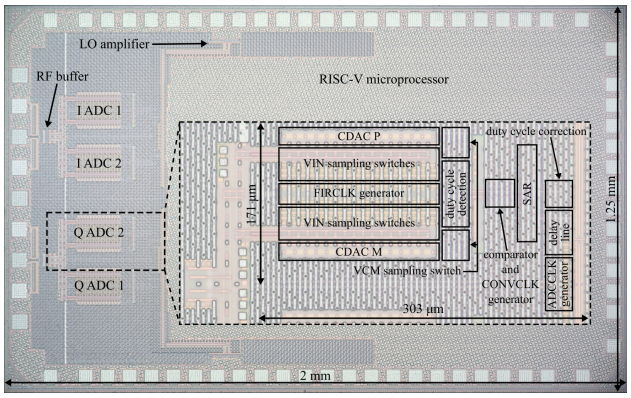

Fig. 5: Chip micrograph.

CLK GEN in Fig. 2) to decouple the conversion frequency from the 3–6 GHz LO. Furthermore, there is no power consumption of additional clock dividers and buffering as the conversion clock is derived from the comparator in a ring-oscillator manner. The comparator, conversion clock generator, bootstrapped switches, and input buffer are implemented using analog layout generators with automated sizing and optimization routines [12], [13].

III. Measurement results

Fig. 5 shows the die micrograph of the downconverting and filtering ADC implemented in 22 nm FDSOI process. Fig. 6 shows the measured FIR filter responses on top of an ideal Python model response with different LO frequencies of 3, 3.75, 5.25 and 6 GHz. As demonstrated in the figures, the filter is reconfigurable and changes depending on the used LO frequency to keep the ADC sampling rate constant.

Fig. 7 shows the time-interleaved ADC performance with downconversion from 3 and 6 GHz carrier frequencies with 2 MHz and 98 MHz baseband signal frequencies. The input power level is kept constant across the measurements, and as can be seen in Fig. 7, the linearity performance degrades at lower frequencies. This can be attributed to two factors. First, the third harmonic that folds to the baseband is attenuated by the FIR filtering. Second, as can be seen from the fullscale ranges, the filtering has some in-band attenuation (Fig. 4) that further improves the linearity at frequencies near Nyquist. In

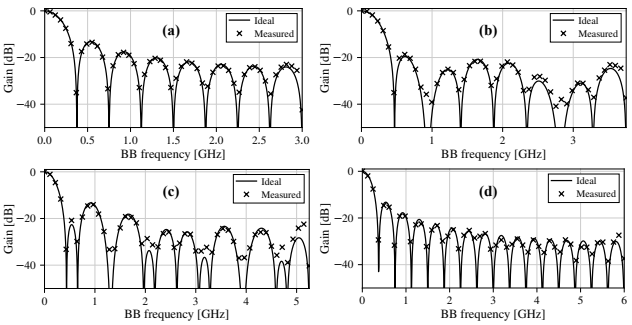

Fig. 6: Measured FIR filter responses with LO signal frequencies of (a) 3 GHz (16 taps) (b) 3.75 GHz (20 taps) (c) 5.25 GHz (28 taps) (d) 6 GHz (32 taps).

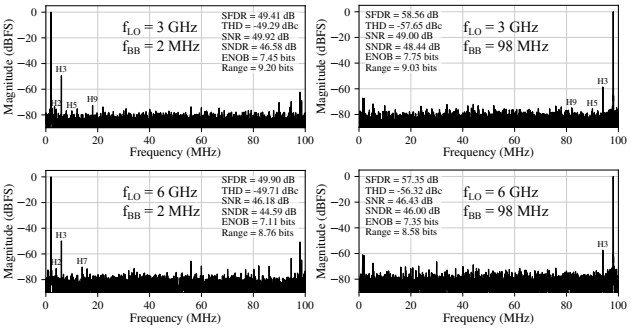

Fig. 7: Measured ADC performance with 3 GHz and 6 GHz carrier frequencies with 2 and 98 MHz baseband signals.

all of the measurements, the timing skew between the time-interleaved branches was foreground calibrated using an on-chip delay line between the unit ADCs. The offset and gain errors were calibrated off-chip in the digital domain.

Fig. 8 shows a carrier frequency sweep with 2 MHz and 98 MHz baseband signal frequencies in Figs. 8a, 8b and Figs. 8c, 8d respectively. The Nyquist performance is noise limited, with the third harmonic limiting the linearity and 2 MHz SNDR is limited by the third harmonic. The core ADC consumes 3.92 mW of power at 3 GHz LO, and 4.17 mW at 6 GHz from a 0.8 V supply. The clock power domain consumes 21.93 mW with 3 GHz LO and 26.24 mW at 6 GHz LO frequency from a 0.8 V supply. The ADC input buffer is consuming 47.6 mW of power when operating at 6 GHz carrier frequency from a supply voltage of 1.275 V. The RISC-V processor system consumes 87.8 mW from a 0.8 V supply. The performance of the proposed downconverting and filtering ADC is compared to other SAR ADCs with embedded downconversion or filtering in Table II.

As can be seen from Fig. 8f, the majority of the clock domain power is consumed statically. This is mainly due to the static power consumption of the self-biased inverters and clock buffers near the I and Q clock pads (Fig. 5). As the static power consumption can not be measured reliably, the dynamic power consumption of the clock domain is estimated using

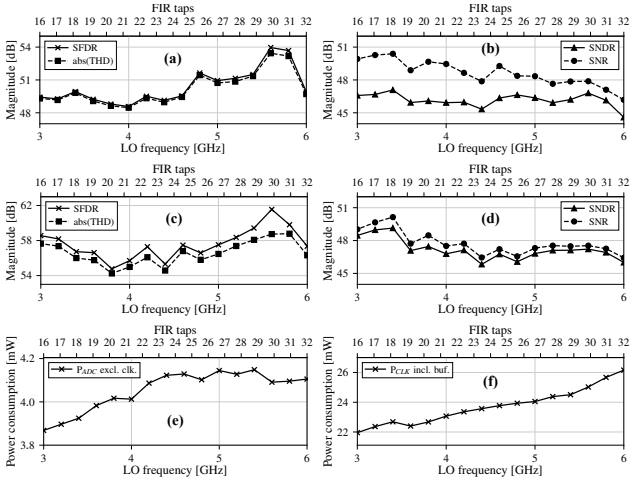

Fig. 8: Measured ADC performance carrier frequency sweep with (a), (b) 2 MHz (c), (d) 98 MHz baseband signal frequency. Power consumption of the (e) ADC (f) clock domain as a function of the carrier and LO frequency.

TABLE II: Performance comparison of SAR ADCs with embedded filtering or downconversion functionality.

	This work	[8]	[2]	[14]	[6]	[3]	[5]
Embedded func.	E1	E2	E3	E4	E5	E6	E7
Process [nm]	22	130	130	130	28	40	28
Supply [V]	0.8	1.2		1.2	1.0	1.1	1.0
Area [mm^2]	0.1035	0.033	0.68	0.04	0.0049	0.067	0.036
Carrier [GHz]	**3–6**	0.2	N/A	N/A	N/A	N/A	N/A
f_s filter [GHz]$^{\downarrow}$	**6–12**	N/A		0.057		0.04	2.8
Min. attn. [dB]‡	>13.2	N/A	>12	>20		>42.2	>40
ADC resolution	10	8	9	8	10	10	5+10
f_s ADC [MS/s]	200	50	5	0.057	132	10	350
BW [MHz]	**100****	25**	2.5**	0.0285**	5	1	80
ENOB	7.45@3G 7.11@6G	7.6*	7.18††	7.8	12.95††	9.42	11.35††
Power [mW]	8.01@3G 12.6@6G†	0.9*	7.32¶	0.0018	0.46	0.0922§	4.87
FoM$_W$ [fJ/c.step]	229.9@3G 453.6@6G	92.8*		140	5.8	13.5	
FoM$_S$ [dB]	147.5@3G 143.6@6G				180.1		172.2

E1: Switching mixer with 16–32 tap FIR filter. E2: Subsampling to IF and variable-reference downconversion. E3: Reconfigurable 4–12 tap FIR filter. E4: Programmable 16-tap digital FIR filter. E5: Noise-shaping and FIR–IIR filter. E6: 13-tap FIR and IIR filter. E7: 8-tap FIR and 3rd-order IIR in a pipelined SAR. *simulated$^{\downarrow}$estimated from figures**ADC Nyquist†excludes estimated static power of clock amplifiers ¶includes internal clock buffer, digital and analog domains§calculated as filter+ADC power††calculated from SNDR

least mean square error fitting to the measured data points and extending the line to 0 Hz. This returns a slope of 1.2475 mW/GHz, and extrapolated to DC a static power consumption of 18.2 mW. As there is some static power consumption in the duty cycle corrector circuit, which is considered ADC power consumption, 0.36 mW of static power is added to the ADC domain according to a post-layout simulated result. By omitting the non-ADC related static power consumption of the clock domain (17.84 mW), the total ADC power consumption is 8.01 mW at 3 GHz and 12.6 mW at 6 GHz LO frequency.

IV. Conclusion

This paper presented a 10-bit 200 MS/s two-times time-interleaved SAR ADC with an embedded 3–6 GHz RF switching mixer and a FIR filter. The mixer was embedded in the ADC sampling operation by sampling at 6–12 GS/s, inverting every other sample to downconvert from a carrier frequency range of 3–6 GHz. In order to reduce the system power consumption, both edges of a 3–6 GHz LO clock were utilized. To mitigate the duty cycle error induced non-linearity, gain and phase errors, the ADC averages the RF samples, which forms a decimating FIR filter. The filter was designed to be reconfigurable with 16–32 taps in order to keep the ADC sampling rate constant at 200 MS/s. The ADC was implemented in 22 nm FDSOI process and measured to achieve over 7.1 effective number of bits, while consuming 8.01–12.6 mW of power at 3–6 GHz LO frequency. The demonstrated ADC is the first SAR with embedded zero-IF downconversion.

References

[1] X. Tang *et al.*, "Low-Power SAR ADC Design: Overview and Survey of State-of-the-Art Techniques," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 69, no. 6, pp. 2249–2262, 2022.

[2] J. Kang, D. T. Lin, L. Li, and M. P. Flynn, "A reconfigurable FIR filter embedded in a 9b successive approximation ADC," in *2008 IEEE Custom Integrated Circuits Conference*, 2008, pp. 711–714.

[3] X. Xin *et al.*, "A Power-Efficient 13-Tap FIR Filter and an IIR Filter Embedded in a 10-Bit SAR ADC," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 70, no. 6, pp. 2293–2305, 2023.

[4] D. T. Lin, L. Li, S. Farahani, and M. P. Flynn, "A Flexible 500 MHz to 3.6 GHz Wireless Receiver with Configurable DT FIR and IIR Filter Embedded in a 7b 21 MS/s SAR ADC," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 59, no. 12, pp. 2846–2857, 2012.

[5] S. Huang, Z. Zhang, X. He, and L. Jie, "A Filter-Embedded Pipe-SAR ADC With Progressive Conversion and Floating Charge Transfer Amplifier," *IEEE J. Solid-State Circuits*, vol. 60, no. 12, pp. 4503–4514, 2025.

[6] C.-C. Liu and M.-C. Huang, "28.1 A 0.46mW 5MHz-BW 79.7dB-SNDR noise-shaping SAR ADC with dynamic-amplifier-based FIR-IIR filter," in *2017 IEEE International Solid-State Circuits Conference (ISSCC)*, 2017, pp. 466–467.

[7] N. Pereira, H. Serra, and J. Goes, "A two-step radio receiver architecture fully embedded into a charge-sharing SAR ADC," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1–4.

[8] N. Pereira and J. Goes, "A charge-sharing analog-to-digital converter with embedded downconversion using a variable reference voltage," *Int. J. Circuit Theory Appl.*, vol. 48, no. 7, pp. 1093–1107, 2020.

[9] M. Waltari and K. Halonen, "Timing skew insensitive switching for double sampled circuits," in *1999 IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 2, 1999, pp. 61–64 vol.2.

[10] M. Tenhunen, V. Lahtinen, and M. Kosunen, "Automatic Reference Clock Duty Cycle Calibration System for Dual Edge Sampling RF Circuits," in *2025 IEEE Nordic Circuits and Systems Conference (NorCAS)*, 2025, pp. 1–5.

[11] G. Manganaro, "An introduction to high sample rate nyquist analog-to-digital converters," *IEEE Open Journal of the Solid-State Circuits Society*, vol. 2, pp. 82–102, 2022.

[12] V. Lahtinen, S. Porrasmaa, A. Heikkinen, M. Tenhunen, J. Ryynänen, and M. Kosunen, "Fully Programmatic Automated Design Procedure of Comparators for Analog-to-Digital Converters," *IEEE Trans. Comput. Aided Des. Integr. Circuits Syst.*, vol. 44, no. 10, pp. 4043–4047, 2025.

[13] V. Lahtinen, A. Heikkinen, S. Porrasmaa, A. Tamminen, and M. Kosunen, "An Efficient Framework for Fully Automated Post-layout Simulation-based Optimization," in *2025 21st International Conference on Synthesis, Modeling, Analysis and Simulation Methods, and Applications to Circuits Design (SMACD)*, 2025, pp. 1–4.

[14] K. Abdelhalim, L. Kokarovtseva, J. L. P. Velazquez, and R. Genov, "915-MHz FSK/OOK Wireless Neural Recording SoC With 64 Mixed-Signal FIR Filters," *IEEE J. Solid-State Circuits*, vol. 48, no. 10, pp. 2478–2493, 2013.