A 97.6% Peak-Efficiency 3–36 V Integrated BCD Gate Driver with Adaptive Dead-Time Control and Open-Loop Gate-Drive Boost

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***Abstract*—An integrated gate driver for high-efficiency BCD synchronous buck converters is presented, focusing on an adaptive dead-time controller (ADTC) and a compact open-loop gate-drive boost (GB) circuit for Dead-time, reverse-recovery charge, and switching-loss reduction. The ADTC directly senses the switching node to minimize both dead-times, achieving near load-independent DT_F of 0–2 ns over 0–4 A while digitally reducing DT_R from ∼6 ns to near 0 ns. At 36 V/5 V, 2 A and 1 MHz, ADTC-R reduces loss by 0.466 W, improving efficiency by 3%. The GB circuit accelerates the LX rising transition without increasing peak dV_{LX}/dt, reducing rise time by 22 ns (47%) and providing an additional 0.375 W loss reduction and 2.5% efficiency improvement. Combined operation yields 5.5% efficiency improvement and 0.81 W loss reduction, corresponding to a junction temperature reduction of up to 40.5°C. Fabricated in 0.11-μm STMicroelectronics BCD technology, the prototype operates from 3 to 36 V up to 4 A and 2.2 MHz, achieving 97.6% peak efficiency and 1.95× higher FoM_{PED} than prior work.**

***Index Terms*—Bipolar-CMOS-DMOS (BCD), gate driver, adaptive dead-time control, gate drive boost, switching loss, dead-time loss, reverse recovery loss, High-Voltage (HV) synchronous buck converter**

I. Introduction

The demand for compact and power-dense DC-DC converters is strongly constrained by achievable efficiency and thermal dissipation limits. At higher switching frequency (f_{SW}), switching, dead-time (DT) associated losses, and gate-drive inefficiencies dominate the efficiency spectrum [1], requiring the need for optimized efficient gate-driver architectures (Fig. 1).

DT-associated losses significantly impact efficiency at high f_{SW}. Excess DT increases Low-side (LS) PowerMOS body-diode conduction and its reverse-recovery charge (Q_{RR}), both strongly dependent on forward current, maximizing efficiency degradation at high load current (I_L) and input voltage (V_{IN}). While insufficient DT risks shoot through [2].

Conventional and fixed DT schemes rely on conservative margins, prioritizing robustness, and do not track I_L-dependent switching node (LX) slew rates [3], [4]. Digital predictive methods reduce average DT [5] but degrade under fast transients, and do not directly sense the LX node, enabling more accurate DT adjustment. Adaptive approaches sense LX directly through an inefficient resistive-divider [1], or Zero

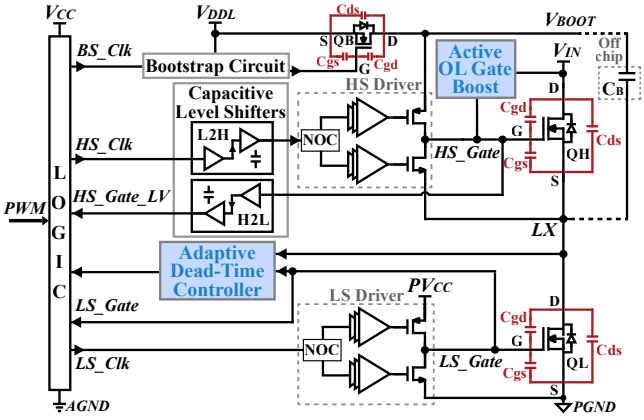

Fig. 1. System Block Diagram of the proposed Integrated Gate Driver for the Synchronous Buck Converter.

Voltage Switching (ZVS) block [6], but the information still needs to propagate through the driver, introducing sub-optimal DT. Bang-bang adaptive DT controllers [7] improve efficiency, but exhibit slow transient response to fast load transients and steady-state oscillations due to the control voltage ripple.

Switching loss is dominated by the finite transition times of LX, where the falling transition is defined by I_L and the rising transition by high-side (HS) gate-drive strength. Increasing drive strength reduces switching loss but increases dV_{LX}/dt, Electromagnetic Interference (EMI), voltage overshoot, and device stress, creating an efficiency and reliability trade-off [3]. Passive gate shaping using a series gate resistor reduces dV_{LX}/dt at the expense of higher switching loss [3], while closed-loop di/dt or dV_{LX}/dt control improves loss but introduces large initial switching stress and bootstrap loading [8]. Open-loop segmented drivers [3] mitigate EMI but lack direct LX sensing for optimal transition control.

The proposed Integrated gate-driver architecture (Fig. 1) combines an adaptive DT controller (ADTC) and a compact open-loop gate drive boost (GB) circuit for improved efficiency. Section II details the design, Section III presents experimental results, and Section IV concludes the paper.

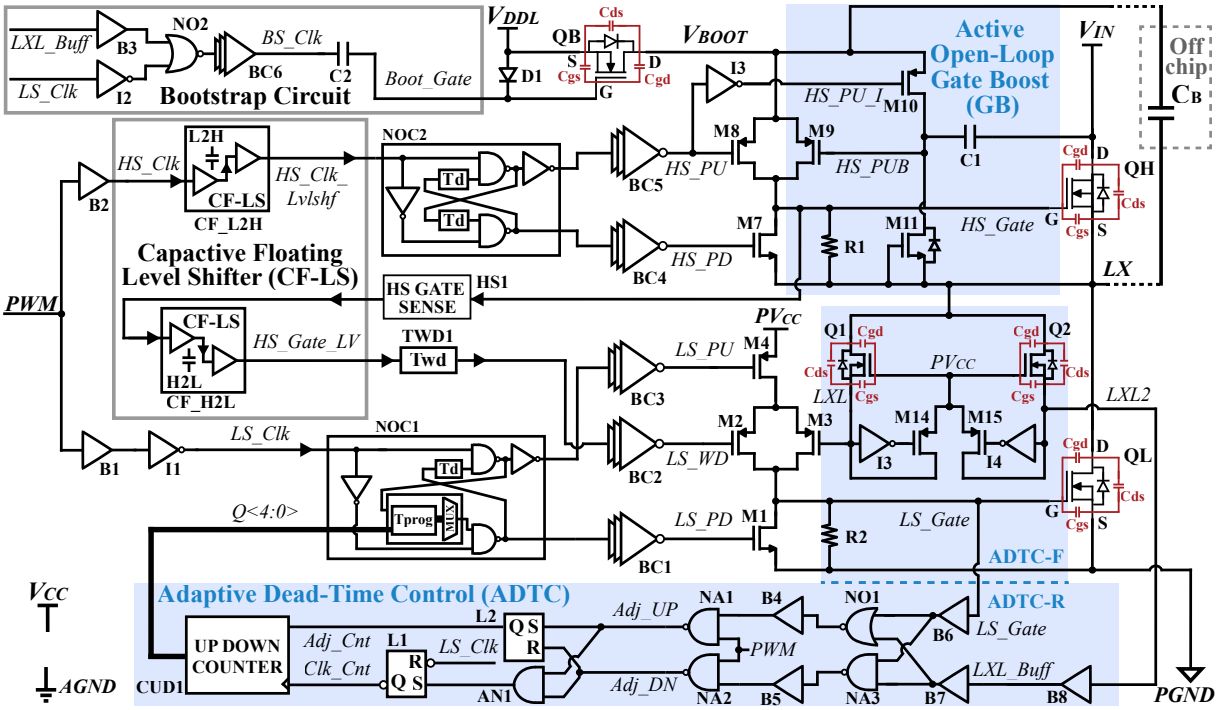

Fig. 2. Proposed Architecture of the Integrated Gate Driver.

II. Design of the Integrated Gate Driver

The integrated gate-driver architecture (Fig. 2) employs several efficiency-driven techniques, including capacitive floating level shifters (CF-LS) for efficient signal translation validated in [9], NMOS bootstrap switch for improved area utilization, and a break-before-make output stage to suppress crowbar current. The proposed ADTC and GB circuit, which enable DT optimization and switching loss reduction, represent the primary contributions of this work and are detailed next.

A. Adaptive Dead-Time Controller (ADTC)

The ADTC consists of two sub-blocks: falling DT controller (ADTC-F) to minimize high-to-low DT (DT_F), and rising DT controller (ADTC-R), which reduces low-to-high DT (DT_R).

The ADTC-F uses a sensing HV PowerMOS (Q1) as a ZVS detector to generate a low-voltage replica (LXL) of LX, which directly controls M3. During the LX rising transition, LXL follows until clamped to PV_{CC} by M14 turn-on. After HS turn-off, LXL initially droops with LX (Fig. 3a), with M14 sized weakly to allow tracking. Once LXL crosses the Q1 threshold, Q1 turns on, forcing LXL to follow LX and disabling M14. As LX nears ground, M3 activates, terminating DT_F. Since triggering depends on absolute LX voltage rather than dV_{LX}/dt, DT_F remains largely I_L-independent.

The DT_R does not depend on I_L, but can vary with slow PVT changes affecting driver delay, making adaptive tuning necessary. A compact digital ADTC-R (125μm $\times$ 85μm) minimizes DT_R from an initial 5–8 ns using a 5-bit up–down counter that detects overlap between LS_Gate and a scaled LX replica ($LXL2$). Non-overlap/overlap generates Adj_UP/Adj_DN pulse to increment/decrement the counter, respectively, allowing cycle-by-cycle convergence through a programmable delay chain (250 ps/step), tuning LS_Gate turn-off via LS_PD (Fig. 3b). The loop converges to $\sim$1 ns residual DT_R, after which a DeadZone freezes the count to avoid oscillation and save power until PVT drift occurs.

B. Gate Drive Boost (GB) Circuit

The GB circuit accelerates the LX rising transition via an auxiliary pull-up (M9) activated through capacitive coupling of HS_PUB via a 130 fF High-Voltage capacitor (C1). M10 resets HS_PUB, M11 limits the voltage stress, and R1 prevents floating. A smaller M8 sets the initial pull-up strength to limit inrush current, di/dt and $(dV_{LX}/dt)_{pre,GB}$. As LX starts to rise, HS_PUB falls per (1) (Fig. 3c), increasing $V_{gs,M9}$ and enabling M9 to boost the pull-up current.

$$\frac{dV_{HS\_PUB}}{dt} = k\left(\frac{dV_{LX}}{dt}\right)_{pre,GB}(t), \quad k = \frac{C_{p,hs\_pub}}{C_1 + C_{p,hs\_pub}} \tag{1}$$

This shortens the LX rise time and Miller plateau interval, with C1 defining activation timing (2) and M9 sizing setting the boost level, with a compromise to maintain dV_{LX}/dt below its initial spike (Fig. 3c).

$$t_{GB,ON} \approx \frac{V_{TH,M9}}{\left(\frac{dV_{HS\_PUB}}{dt}\right)} \tag{2}$$

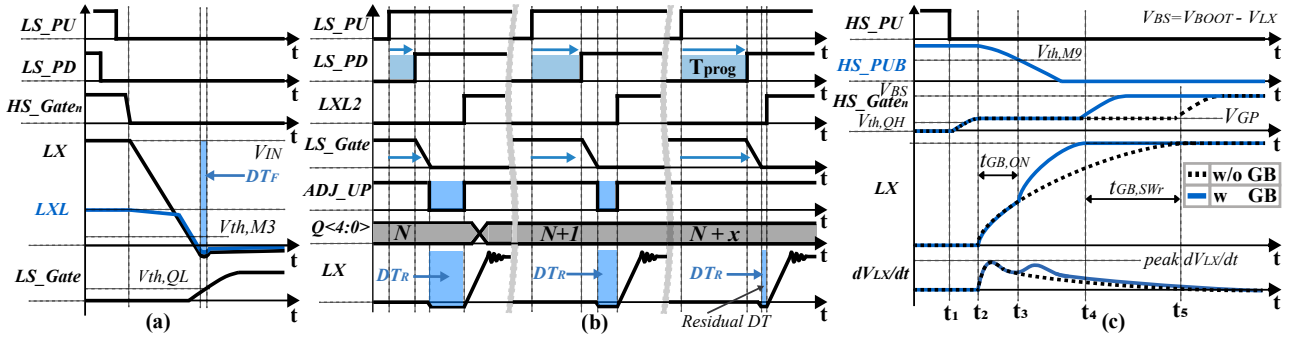

Fig. 3. Signal waveforms associated with (a) ADTC-F and reduction of DT_F; (b) ADTC-R and reduction of DT_R; (c) effect of GB circuit on LX rise time.

III. Results

The proposed Integrated Gate Driver is fabricated in 0.11-μm STMicroelectronics BCD process and packaged in a QFN-24L. The chip micrograph and measurement setup are shown in Fig. 4a–b. The driver core occupies 0.25 mm^2 within a total die area of 2.0 mm × 2.2 mm, largely dominated by the integrated PowerMOS. The design is validated up to V_{IN} = 36 V, I_L = 4 A, and f_{SW} = 2.2 MHz with V_{DDL} = PV_{CC} = 3.3 V and a 10 μH inductor, regulating 5 V/12 V outputs.

ADTC-R and GB can be selectively disabled to quantify their impact on efficiency, whereas ADTC-F remains always active; its benefit is reflected in overall performance.

Measurement results in Fig. 5a show DT_F is nearly load-independent, increasing from 0 ns at no-load to about 2 ns at I_L=4 A. At high load, LS_Gate rise time is the bottleneck of the transition, resulting in a residual DT. At light load, however, a near-zero DT_F does not cause hard switching since LX is already close to 0 V.

Fig. 5b shows ADTC-R reduces DT_R from ~6 ns to near zero, significantly lowering LS body-diode conduction and Q_{RR} losses by 0.466 W and improving efficiency by 3% at 36 V/5 V, I_L=2 A and f_{SW}=1 MHz (Fig. 7). Reduced Q_{RR} also lowers peak dV_{LX}/dt (Fig. 5b), improving robustness and enabling stronger HS pull-up for further switching-loss reduction.

The GB (Fig. 6) reduces LX rise time by 22 ns (47%) without increasing peak dV_{LX}/dt, lowering loss by 0.375 W and improving efficiency by additional 2.5% under the same conditions. Combined ADTC-R and GB operation (Fig. 7)

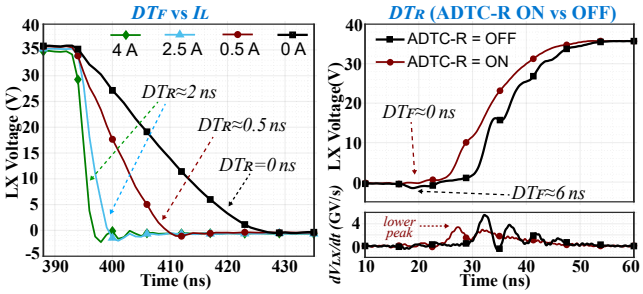

Fig. 5. Measurement result of both DT at $V_{IN} = 36\,V$: (a) DT_F at different I_L conditions; (b) effect of ADCT-R on DT_R.

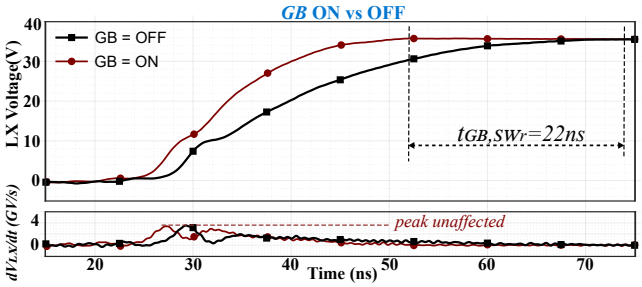

Fig. 6. Measurement result highlighting impact of GB on rising transition of LX node at $V_{IN} = 36\,V$.

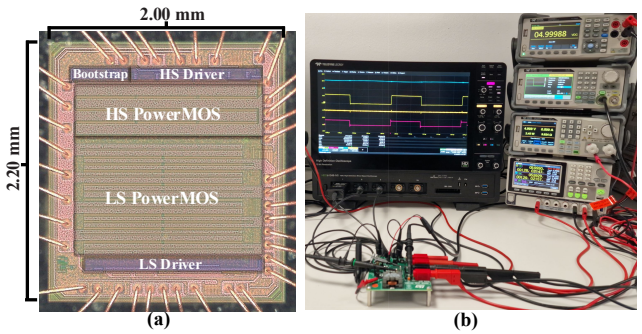

Fig. 4. (a) Micrograph of the proposed gate-driver IC; (b) Measurement Setup.

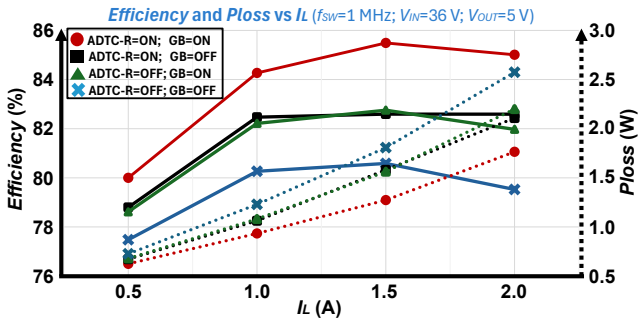

Fig. 7. Measured efficiency and power-loss impact of ADTC-R and GB versus load current at 36 V/5 V conversion and 1 MHz frequency.

TABLE I
Comparison with commercial and literature buck converters

		LMR38020		LM5007	LMR36506		[1]	[10]	[3]	[11]	[12]	[TW]		
Technology							0.5μm	0.18μm	0.18μm	0.18μm	0.35μm	**0.11μm**		
V_{IN} (V)		4.2–80		9–75	3–65		40–100	4.5–60	5–18	4.5–60	3.3–3.6	**3–36**		
f_{SW} (MHz)		0.2–2.2		0.4	0.2–2.2		0.5	0.1–1.2	0.66–1.1	0.1–2.5	1	**0.4–2.2**		
V_{OUT} (V)		5/12		10	3.3/5		24	5	2.5	5	2.5	**5/12**		
Max I_L (A)		2.0		0.5	0.6		0.4	5	2	5	0.6	**4**		
Die Area		3.89mm^2		2.0mm^2	2.00mm^2		7.0mm^2	4.0mm^2	1.4mm^2	4.38mm^2	2.25mm^2	**4.4mm^2**		
Peak η	η (%)	91.0	95.0	93.7	93.5	92.5	94.9*	95.6	92.8*	94	90.0	**97.6***	**95.1***	**97.6***
	V_{IN}/V_{OUT} (V)	24/5	24/12	15/5	12/5	12/5	40/5	7/5	5/2.5	8/5	3.6/2.5	**12/5**	**12/5**	**24/12**
	F_{SW} (MHz)	0.4	0.4	0.38	0.4	1.0	0.5	0.5	0.66	0.4	1.0	**0.4**	**1.0**	**0.4**
	I_L (A)	0.8	0.9	0.3	0.3	0.3	0.25	0.3	0.3	0.8	0.3	**0.6**	**1.0**	**1.0**
	FoM_{ED}[1] (MHz/mm^2)	1.04	1.95	2.826	2.88	6.17	1.33	2.71	6.07	1.42	1.60	**3.69**	**4.41**	**3.69**
	FoM_{PED}[2] (W*MHz/mm^2)	4.16	21.10	4.239	4.32	9.25	1.66	4.07	4.56	5.68	1.2	**11.09**	**22.05**	**44.36**

(*)Open-loop Buck converter; controller LTC3891 reduces efficiency by 0.3% at 0.4 MHz (consumption 10 mW) and 0.2% at 1 MHz (consumption 16 mW)
([1])Efficiency density $FoM(FoM_{ED})=(P_{OUT}\times f_{SW})/(P_{loss}\times Area)=f_{SW}/[Area((1-\eta)/\eta)]$;([2])Power-Efficiency density $FoM(FoM_{PED})=(P_{OUT}\times f_{SW})/[Area((1-\eta)/\eta)]$

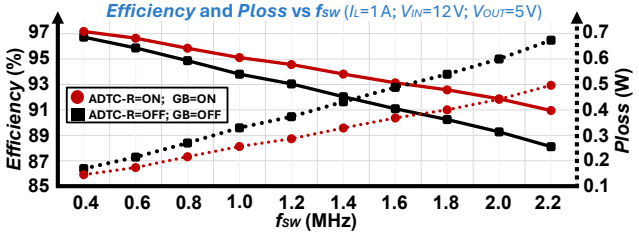

Fig. 8. Measured efficiency gain and power-loss reduction versus f_{SW} with ADTC-R and GB enabled at 12 V/5 V conversion and $I_L = 1$ A.

achieves 5.5% efficiency improvement and 0.81 W loss reduction, corresponding to junction temperature reduction up to 40.5°C, assuming 50°C/W typical system thermal resistance.

Fig. 8 shows increasing benefits at higher f_{SW}, achieving 2.84% efficiency improvement and 0.177 W loss reduction at 12 V/5 V, I_L=1 A and f_{SW}=2.2 MHz; at I_L=2 A the improvement increases to 3.19% and 0.41 W respectively.

Fig. 9 shows peak efficiency of 97.6% at 12 V/5 V (0.6 A) and 24 V/12 V (1 A), a 2% improvement over prior work (Table I). For fair comparison across converters with different power levels, frequency, silicon area, and efficiency, a Power-Efficient Density FoM (FoM_{PED}) is adopted to capture the efficiency–power density trade-off, with the proposed design achieving a 1.95× improvement over prior work at 5V output.

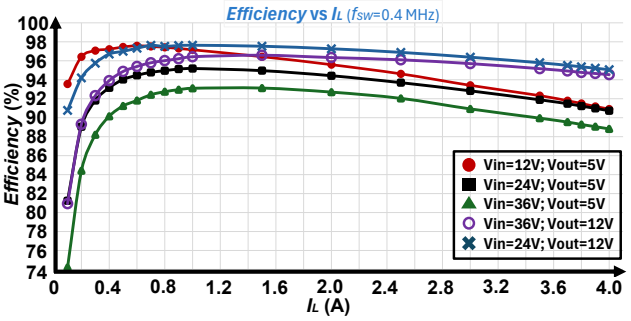

Fig. 9. Measured converter efficiency versus I_L for different conversion ratios at $f_{SW} = 0.4$ MHz.

IV. Conclusion

An LX-sensing ADTC and compact open-loop GB circuit are implemented to reduce DT-, Q_{RR}-, and switching-related losses. Measurements show DT_F of 0–2 ns over 0-4 A and DT_R reduction from ∼6 ns to near 0 ns. At 36 V/5 V, 2 A and 1 MHz, they achieve 5.5% efficiency improvement and 0.81 W loss reduction. Fabricated in 0.11-μm BCD, the prototype operates from 3–36 V up to 4 A and 2.2 MHz, reaching 97.6% peak efficiency and 1.95× higher FoM_{PED} than prior work.

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