A 0.36–mW 500–kHz–BW 182.2–dB–FoMs 3rd–order DNC-Based Sturdy MASH CT DSM

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***Abstract*—This paper presents a 3rd-order single-opamp digital noise coupling (DNC)-based sturdy multi-stage noise-shaping (SMASH) continuous-time (CT) delta-sigma modulator (DSM). The large internal signal swings caused by high-order-shaped quantization error (E_1) in single-loop DSMs and the stringent analog-digital filter matching required in MASH DSMs are alleviated by the proposed M–0 SMASH architecture. The absence of a second-stage analog LF is compensated through a 2nd-order DNC filter. SAR sampling kickback is mitigated by a simple passive RC filter. Fabricated in 28-nm CMOS, the prototype achieves 87.4-dB SNR, 87.0-dB SNDR, and 90.8-dB DR over a 500-kHz BW while consuming only 0.36 mW from a 1.0-V supply, resulting in a state-of-the-art Schreier FoM (FoM_S) of 182.2 dB and a Walden FoM (FoM_W) of 19.7 fJ/conv.-step.**

I. Introduction

In typical DSM architectures, the noise-shaping order is directly proportional to the number of power-consuming analog integrators. To address this, SAR-assisted DNC topologies [1], [2], [3], [4], [5] are utilized to provide aggressive noise shaping without increasing the order of the loop filter (LF) by replacing these analog integrators with simple digital delay cells. However, single-loop DSMs with DNC exhibit a low maximum stable amplitude (MSA) due to high out-of-band gain (OBG) (e.g., −3.6 dBFS in [1]). While solutions such as digital integrators allow for a larger MSA (−1.6 dBFS in [6]), the nature of high-order single-loop DSMs still results in significant LF input swing, necessitating stringent amplifier requirements and high power consumption. These issues can be alleviated using a MASH DSM [7], where E_1 is shaped by its own lower-order loop and removed (ideally) via a digital cancellation filter (DCF) at the output, while the smaller second-stage quantization noise, E_2, is further shaped by DNC on top of the NTF, all in a single SAR ADC.

Nevertheless, MASH architectures (whether utilizing DNC or not) are highly susceptible to noise leakage caused by analog-digital filter mismatch, an issue that is particularly pronounced in CT implementations. As an alternative, [8], [9], [10] proposed utilizing DNC for noise-leakage shaping rather than for additional quantization noise shaping. For example, [9] proposes a digital noise-coupling compensation filter (on top of the standard DCF) to shape the leakage term as $(1 - z^{-1})E_1$ at the output and leaves the desired E_2, which was further shaped by a passive noise-shaping SAR in addition to the analog LF. However, this method requires E_1 to pass through the DNC filter and undergoes additional noise shaping within the main loop, causing the architecture to behave like a high-order single-loop DSM having high OBG, thereby losing the advantages of a MASH structure.

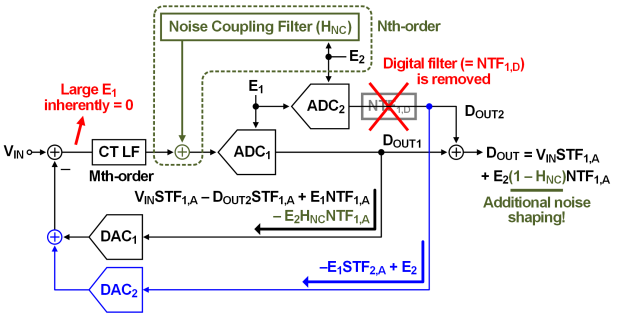

Fig. 1. Conceptual diagram of the proposed NC-based M-N SMASH CT DSM.

To address these challenges, this work proposes a 1–2 SMASH architecture with DNC, utilizing a single SAR ADC, to eliminate the need for analog-digital filter matching. Furthermore, owing to the zeroth-order second stage having an STF = 1, large E_1 is inherently canceled within the main loop (detailed in Section II.A). This achieves significantly smaller internal signal swings, which further relaxes the amplifier design requirements. To compensate for the absence of a second-stage analog LF, a DNC filter is implemented. Additionally, to mitigate the gain mismatch between the first- and second-stage feedback DACs, a mismatch error shaping (MES) technique is adopted [9].

II. Proposed DNC-Based Sturdy MASH CT DSM

A. Derivation, Analysis, and Overall Implementation

Fig. 1 illustrates the conceptual diagram of the proposed two-stage noise-coupling (NC)-based *M–N* SMASH DSM. To construct the SMASH architecture, the digital filter required for typical MASH architectures is removed; instead, both outputs (D_{OUT1} and D_{OUT2}) are fed back to the first-stage loop. In addition, compared to typical SMASH implementations where E_1 is shaped to the same order as E_2, large E_1 is inherently canceled in both the main loop and the final output since $STF_{2,A}$ is inherently unity due to the absence of a second-stage analog LF, which significantly relaxes the requirements for the opamp DC gain and UGBW. Furthermore, to compensate for the lack of second-stage noise-shaping capability, the proposed architecture introduces additional noise shaping to E_2 by applying an NC structure, which effectively transforms the *M*–0 structure into an *M–N* SMASH topology. Consequently, the final output contains V_{IN} and the second-stage quantization noise, E_2, which is shaped by both the NC transfer function $(1 - H_{NC})$ and the first-stage NTF. Notably, this NC filter can be realized in the digital domain (i.e., DNC), and ADC_1 and ADC_2 can be merged in a single SAR ADC.

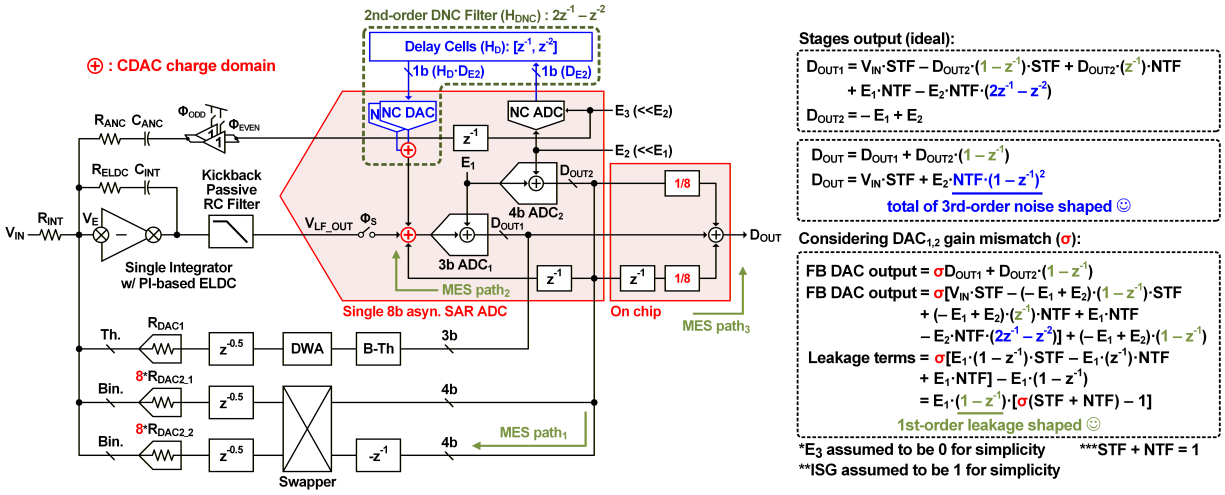

Fig. 2. Overall implementation of the proposed 3rd-order single opamp DNC-based 1-2 SMASH CT DSM with MES (single-ended representation for simplicity).

Fig. 2 shows the overall implementation of the proposed 1–2 DNC-based SMASH CT DSM. The 1st-order CT LF is implemented using an active-*RC* integrator with chopping ($F_c = F_s/2$), while ELD is compensated through R_{ELDC} (= $0.5R_{INT}$) to improve compactness and efficiency. In this architecture, similar to previous DNC works [6], E_1 from ADC_1 (i.e., MSBs of the single SAR) is extracted and injected into ADC_2 (ISBs), after which E_2 is further digitized by the NC ADC (LSBs). The resulting digitized residue (D_{E2}) is then filtered by delay-cell-based logic (H_D) and injected back into the quantizer input through the NC DACs (LSBs) to achieve additional noise shaping for E_2, all within a single 8-bit SAR ADC. Unlike previous single-loop DNC architectures [1], however, where E_1 passes through the DNC path, the proposed approach eliminates large E_1 from the DNC filter; instead, only E_2 goes through the DNC path. Since E_2 in this work results from ISBs, the proposed architecture demonstrates significantly lower noise power compared to prior single-loop DNC. Moreover, unlike previous DNC-based MASH structures [7], both the first- and second-stage outputs (D_{OUT1} and D_{OUT2}) are fed back to the main loop to construct the SMASH architecture. Lastly, as DAC_2 only processes quantization noise, simulation results shows that non-linearity (NL) of DAC_2 results in only a slight increase in the noise floor with no observable tones and negligible performance degradation. Thus, DWA is applied only to DAC_1, enabling a more power-efficient and compact implementation.

Notably, owing to the single SAR ADC implementation, $STF_{2,A}$ is guaranteed to be unity, which inherently cancels E_1 completely as previously discussed. To address the gain mismatch between the two feedback DACs from ADC_1 and ADC_2, an MES technique is adopted [9]. To maintain high hardware efficiency, one of the key building blocks for the MES is also embedded within the same single SAR ADC. As shown in Fig. 2 (top-right), the final output, D_{OUT}, cancels E_1 and leaves only the desired E_2 shaped by both the DNC and the NTF, thereby maintaining the NC-based SMASH characteristic. To achieve the target DR (≥ 90 dB), R_{INT} is set to 5 kΩ, and the unwanted quantization noise from the NC ADC (E_3) is further suppressed by first-order analog noise coupling (ANC) through low-power ping-pong dynamic buffers with C_{ANC} (= C_{INT}) and R_{ANC} (= R_{ELDC}) [6].

Fig. 3 (top) presents a behavioral simulation comparing two prior

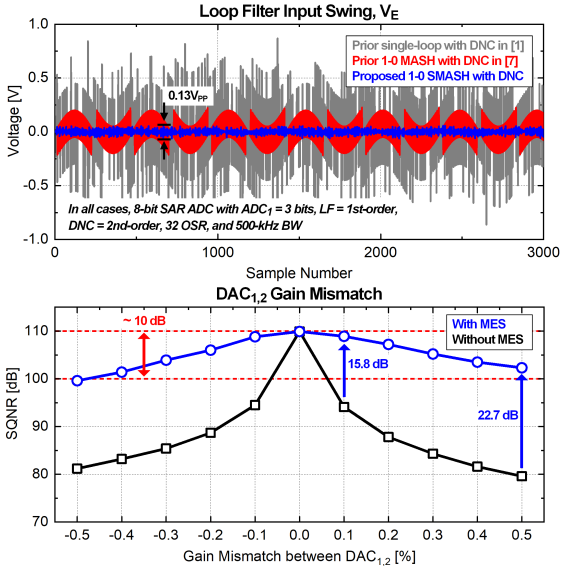

Fig. 3. Behavioral simulation: (top) LF input swing and (bottom) DAC gain mismatch.

DNC works, single-loop DNC-DSM [1] and the DNC-based MASH [7], with the proposed DNC-based SMASH. For a fair comparison, an 8-bit SAR quantizer, 1st-order LF, and 2nd-order DNC filter were used across all three cases. Considering DWA complexity, ADC_1 was set to 3 bits. The remaining 5 bits were allocated to the NC ADC in the single-loop DNC-DSM [1], while both the DNC-based MASH [7] and the proposed DNC-based SMASH divide the 5 bits into 4 bits and 1 bit for ADC_2 and the NC ADC, respectively. As expected, the proposed architecture achieves a significantly smaller swing at the input of the LF of only 0.13 V_{PP}, which is 13.5× and 3.4× lower than [1] and [7], respectively, since E_1 is inherently canceled in the proposed architecture, whereas it remains in the internal nodes of both the prior works. Consequently, this characteristic significantly relaxes the amplifier linearity requirements.

Considering the SAR's subranging property, the ADC_2 output should be scaled by 1/8, which is matched in the analog domain by sizing the resistors in R_{DAC2} (= 8 × R_{DAC1}). However, while the SMASH topology removes the challenge of analog-digital filter matching inherent in MASH architectures, the challenge shifts to the

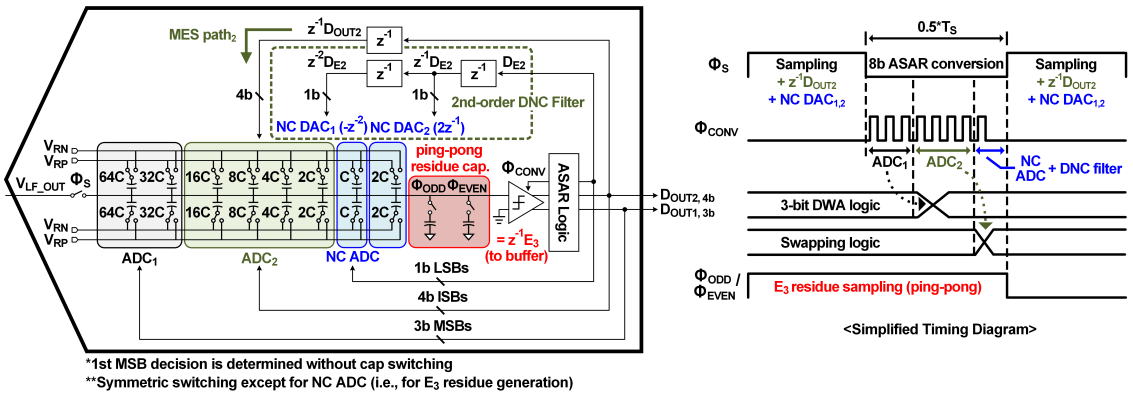

Fig. 4. Detailed implementation of the 8b asynchronous SAR ADC with 2nd-order DNC filter and MES and its corresponding timing diagram.

requirement for precise gain matching between DAC_1 and DAC_2 (i.e., ratio must be exactly 8:1). As shown in Fig. 3 (bottom, black curve), the SMASH architecture suffers a 16-dB SQNR degradation even with only a ±0.1% DAC gain mismatch; this issue is typically addressed through precise layout matching [11] or by combining both stages into a high-resolution single DAC [12]. In this work, a delayed duplicate of DAC_{2_2} (MES $path_1$ in Fig. 2) with element swapping is added to effectively shape the $DAC_{1,2}$ gain mismatch. As described in Fig. 2 (bottom-right), the dominant E_1 leakage term caused by the DAC gain mismatch (σ) is first-order shaped $(E_1 \cdot (1-z^{-1}) \cdot [\sigma(STF+NTF)-1])$, maintaining the SQNR over 100 dB with only 10-dB degradation even at a ±0.5% gain error [Fig. 3]. Since the additional DAC_{2_2} is inserted for MES, this additional term must be eliminated from the final output; this is achieved through MES $path_2$ (within single SAR ADC) and MES $path_3$ (performed on-chip alongside ADC_1 and ADC_2 digital outputs).

Lastly, to address the issue where SAR sampling kickback limits the overall settling behavior and modulator linearity, prior works have employed buffers, either open-loop [13] (to isolate kickback noise) or closed-loop [14] (active only during the first half of the SAR sampling period), which suffer from analog power consumption. In this work, a simpler and more power-efficient alternative is proposed by implementing a passive *RC* filter at the quantizer input. The BW of this kickback filter is designed to be significantly higher than the modulator BW to ensure it does not affect loop stability. With R = 3 kΩ and C = 100 fF, the filter occupies a negligible area of only 40 μm × 10 μm, restoring nearly ideal performance with a 15-dB SQNR improvement.

B. Circuit Implementation with an 8-bit SAR ADC

The detailed implementation of ADC_1, ADC_2, 2nd-order DNC, and MES using a single SAR quantizer, is illustrated in Fig. 4. For simplified clocking, $0.5T_s$ is allocated for sampling, DNC filtering, and MES, while the remaining $0.5T_s$ is utilized for ADC_1, ADC_2, NC ADC, DWA, and swapping logic. By utilizing a split-cap array, the first MSB decision is made without any cap switching, with monotonic switching for LSB (E_3 generation). The residue E_3 is then stored in a ping-pong residue cap for ANC [6]. During the sampling phase, $z^{-1}D_{OUT2}$ for the MES is fed back to the 4-bit ISB portion. Simultaneously, to feedback the $-z^{-2}D_{E2}$ term for the DNC, the 1-bit LSB cap (NC $DAC_1 = C$) is utilized. To achieve the required gain for $2z^{-1}D_{E2}$, an additional NC $DAC_2 (= 2C)$ is added, which eliminates the need for digital adders and allows to perform

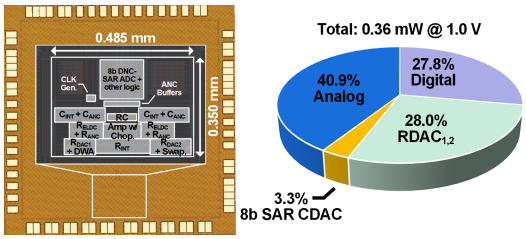

Fig. 5. Chip micrograph and power breakdown.

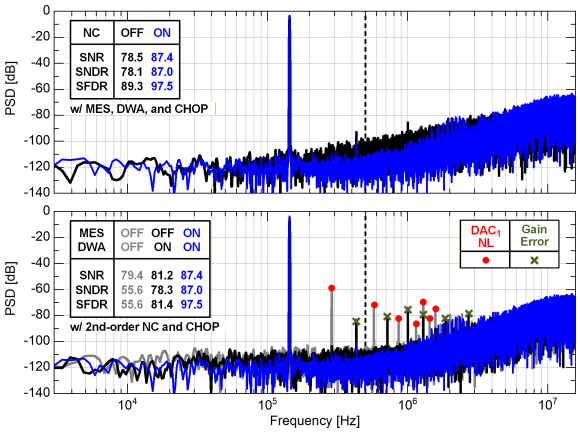

Fig. 6. Measured PSD with and without (top) NC and (bottom) MES and DWA.

both MES and DNC filtering at the same time. For optimized timing, after MSB decision (= D_{OUT1}), the output is fed back to DWA logic while the ISBs are being performed. Similarly, after ISBs (= D_{OUT2}), it goes to the swapping logic while the LSB is being performed.

III. Measurement Results

The proposed 3rd-order DNC-based SMASH CT DSM was fabricated in a 28-nm CMOS process, occupying a core area of 0.17 mm^2 (Fig. 5). Fig. 6 illustrates the measured PSD with a 143.56 kHz, −2.0 dBFS input at room temperature. When the 2nd-order NC is disabled, the performance is limited to a 78.1-dB SNDR, as the noise shaping is provided only by the 1st-order analog LF. Enabling the NC improves the SNDR by 9 dB. Note that, with both DWA and MES inactive (with NC on), the SNDR and SFDR are limited to 55.6 dB. Activating both the DWA and MES yields a significant linearity improvement of 31.4-dB SNDR and 41.9-dB SFDR, reaching a peak SNDR of 87.0 dB and SFDR of 97.5 dB at a 500-kHz BW. Fig. 7 illustrates the measured DR of 90.8 dB. The prototype demonstrates

TABLE I
PERFORMANCE COMPARISON TO STATE-OF-THE-ART CT DSMS REPORTED OVER THE YEARS WITH SIMILAR BANDWIDTH

Parameter	**This work**	VLSI'19 [15]	CICC'22 [16]	VLSI'23 [17]	VLSI'24 [6]	VLSI'25 [18]	OJ-SSCS'26 [12]
Technology [nm]	**28**	180	40	28	28	28	55
Total NTF order	**3**	4	2	3	4	3	3
# of analog integrator	**1**	**4**	1	1	1	**5 (2+3)**	1 **(+1 adder)**
Supply [V]	**1.0**	1.8	1.1	1.8 / 1.2 / 1.0	1.1	1.0	1.2
BW [kHz]	**500**	250	250	1000	200	250	100
OSR	**32**	64	64	50	32	160 / 40	40
F_S [MS/s]	**32**	64	64	50	12.8	80 / 20	8
$SNDR_{PEAK}$ [dB]	**87.0**	103.5	94.8	84.2	89.0	91.2	89.1
DR [dB]	**90.8**	107.5	96.0	86.8	92.1	92.7	95.3
Power [mW]	**0.36**	24.0	4.7	1.62	0.38	0.39	0.46
$FoM_{S,SNDR}$ [dB]	**178.4**	173.7	172.1	172.1	176.2	179.2	172.5
$FoM_{S,DR}$ [dB]	**182.2**	177.7	173.3	174.7	179.3	180.7	178.7
FoM_W [fJ/conv.-step]	**19.7**	392.4	209.3	61.1	41.2	26.4	98.5

*$FoM_{S,SNDR}$ = SNDR + 10·log(BW/Power) **$FoM_{S,DR}$ = DR + 10·log(BW/Power) ***FoM_W = Power / [2^{ENOB}(2*BW)]

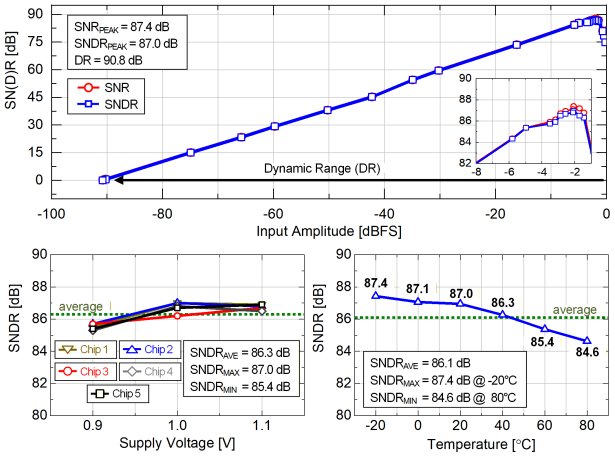

Fig. 7. Measured SN(D)R versus input amplitude (top), supply voltage variation across five samples, and temperature variation (bottom).

excellent robustness, with less than 0.9-dB SNDR variation from the average under ±10% supply voltage variation across five samples, and less than 1.5-dB SNDR variation from the average over a wide temperature range from –20°C to 80°C.

IV. CONCLUSION

This work presents a single-opamp 3rd-order DNC-based SMASH CT DSM with a 2nd-order DNC filter and MES technique, enabling smaller internal signal swings and relaxed opamp requirements compared to prior DNC architectures. The overall architecture integrates most key building blocks into a single SAR ADC. Second-stage DWA is removed and SAR sampling kickback is addressed with a simple passive *RC* filter for improved efficiency. As shown in Table I, due to the relaxed amplifier requirements and additional digital noise shaping provided by the proposed DNC-based SMASH architecture, the prototype consumes only 0.36 mW from a 1.0-V supply, achieving low power consumption while maintaining a relatively wider BW among the compared designs. As a result, this work stands out with the highest $FoM_{S,DR}$ of 182.2 dB, $FoM_{S,SNDR}$ of 178.4 dB, and lowest FoM_W of 19.7 fJ/conv.-step, showing that the combination of SMASH with DNC yields a power-efficient, compact, and robust ADC architecture with a reduced analog burden.

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REFERENCES

[1] I.-H. Jang *et al.*, "A 4.2-mW 10-MHz BW 74.4-dB SNDR continuous-time delta-sigma modulator with SAR-assisted digital-domain noise coupling," *IEEE J. Solid-State Circuits*, vol. 53, no. 4, pp. 1139–1148, Apr. 2018.

[2] Y.-D. Kim *et al.*, "A 4th-order CT I-DSM with digital noise coupling and input pre-conversion method for initialization," in *Proc. IEEE Asian Solid-State Circuits Conf. (A-SSCC)*, 2021, pp. 1–3.

[3] K. E. Lozada *et al.*, "A 4th-order continuous-time delta-sigma modulator with hybrid noise-coupling," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 69, no. 9, pp. 3635–3639, Sep. 2022.

[4] Y.-D. Kim *et al.*, "A 100kHz-BW 99dB-DR continuous-time tracking-zoom incremental ADC with residue-gain switching and digital NC-FF," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, 2024, pp. 1–2.

[5] K. E. Lozada *et al.*, "Continuous-time delta-sigma modulator with SAR-assisted digital noise coupling," in *Proc. IEEE Customs Integ. Circuits Conf. (CICC)*, 2025, pp. 1–8.

[6] K. E. Lozada *et al.*, "A 0.38mW 200kHz-BW 92.1dB-DR single-opamp 4th-order continuous-time delta-sigma modulator with 3rd-order noise coupling," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, 2024, pp. 1–2.

[7] D.-H. Lee *et al.*, "A 25-kHz-BW 97.4-dB-SNDR SAR-assisted continuous-time 1-0 MASH delta–sigma modulator with digital noise coupling," *IEEE J. Solid-State Circuits*, vol. 59, no. 10, pp. 3232–3241, Oct. 2024.

[8] L. He *et al.*, "Digital noise-coupling technique for delta-sigma modulators with segmented quantization," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 6, pp. 403–407, June 2014.

[9] T.-Y. Lo *et al.*, "20.4 An 8×-OSR 25MHz-BW 79.4dB/74dB DR/SNDR CT ΔΣ using 7b linearized segmented DACs with digital noise-coupling-compensation filter in 7nm FinFET CMOS," in *Proc. IEEE Int. Solid-State Circuits Conf. (ISSCC)*, 2019, pp. 334–336.

[10] K. E. Lozada *et al.*, "A SAR-assisted continuous-time M-0 MASH delta-sigma modulator with digital-domain noise leakage shaping," *IEEE Open J. Circuits Syst.*, vol. 7, pp. 69–81, 2026.

[11] N. Maghari *et al.*, "74 dB SNDR multi-loop sturdy-MASH delta-sigma modulator using 35 dB open-loop opamp gain," *IEEE J. Solid-State Circuits*, vol. 44, no. 8, pp. 2212–2221, Aug. 2009.

[12] Z. Lu *et al.*, "Analysis and design of RC-variation-robust continuous-time delta-sigma modulator with boosted MSA," *IEEE Open J. Solid-State Circuits*, early access, Feb. 3, 2026, doi: 10.1109/OJSSCS.2026.3660214.

[13] H. Ghaedrahmati *et al.*, "A 38.6-fJ/conv.-step inverter-based continuous-time bandpass ΔΣ ADC in 28 nm using asynchronous SAR quantizer," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 9, pp. 3113–3117, Sep. 2021.

[14] M. Runge *et al.*, "A 0.9V 45MS/s CT ΔΣ modulator with 94dB SFDR and 25.6fJ/conv. enabled by a digital static and ISI calibration in 22 FDSOI CMOS," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2021, pp. 1–2.

[15] R. Theertham *et al.*, "A 24mW chopped CTDSM achieving 103.5dB SNDR and 107.5dB DR in a 250kHz bandwidth," in *Proc. Symp. VLSI Circuits (VLSI Circuits)*, 2019, pp. C226–C227.

[16] W. Shi *et al.*, "A 0.37mm² 250kHz-BW 95dB-SNDR CTDSM with low-cost 2nd-order vector-quantizer DEM," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, 2022, pp. 1–2.

[17] H.-W. Chen *et al.*, "A 0.024mm² 84.2dB-SNDR 1MHz-BW 3rd-order VCO-based CTDSM with NS-SAR quantizer (NSQ VCO CTDSM)," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, 2023, pp. 1–2.

[18] J. Yoon *et al.*, "A 91.2dB-SNDR 250kHz-BW CT zoom ADC achieving a 6-bit linear zoom-in with interstage LPF and 1.5-bit DAC," in *Proc. IEEE Symp. VLSI Technol. Circuits (VLSI Technol. Circuits)*, 2025, pp. 1–3.