A 5nm 8-phase clock generator based on a feed-forward delay line for 175GSps wireline ADCs

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***Abstract*—This work presents a time-interleaved clock generation circuit implemented in 5nm CMOS for ADCs operating between 170 and 190GSps. The circuit retains random jitter below 50fs and deterministic rms error between the phases below 20fs across the range. Power consumption from a fixed external 0.85V supply is below 45mW. The high operating frequency with CMOS levels is achieved thanks to the addition of feed-forward couplers to a tapped delay-line, optionally disabled to reduce the converter rate. An alternative divider-based low-frequency path enables low-rate operation retaining full supply swings. Calibration and characterization are carried out from data processing of the ADC clocked by the proposed solution.**

I. Introduction

Modern wireline transceivers exceed rates of 100GSps, targeting analog bandwidth in excess of several tens of GHz [1]–[3] to resolve complex modulation schemes [4]. Time-interleaved converters are used both in the Tx and Rx paths, requiring fs-accurate clock generation, both in terms of static (skew) and instantaneous (jitter) rms error. A high-frequency differential clock is delivered to each converter macro, and the multiple phases are generated locally for best performance. Delay lines [5] and injection-locked ring oscillators [6] are the main solutions to minimize power and noise [7]–[10]. PVT variations need to be compensated to reach the stringent sub-degree specifications on skew among the phases. Analog calibrations (fig. 3a) require accurate phase detection, impairing performance of the clocking chain [9], [11]. Digital compensation (fig. 3c) is limited by the power *vs.* accuracy trade-off, thus often complemented by analog tuning [3]. The chosen mixed-signal calibration (fig. 3b) extracts phase error from the ADC data [3], [12], then processed and fed back as correction with analog accuracy.

II. Proposed clocking architecture

The proposed 8-phase clock generator is based on a tunable tapped delay line, as shown in fig. 1. Building on the results of [5], [11], with this architecture the critical path length, and thus power consumption for a given noise, is reduced. Capacitively tuned CMOS inverters are used as delay elements to exploit their superior jitter-power trade-off in the operating region of interest as per [14]. The individual tuning of each inverter allows for coarse correction of deterministic delay mismatch among the taps. The tuning algorithm is based on post-processing of the converter data rather than clock phase detection similarly to [12], for superior accuracy and fewer analog impairments. Fine tuning is embedded in the tap buffers

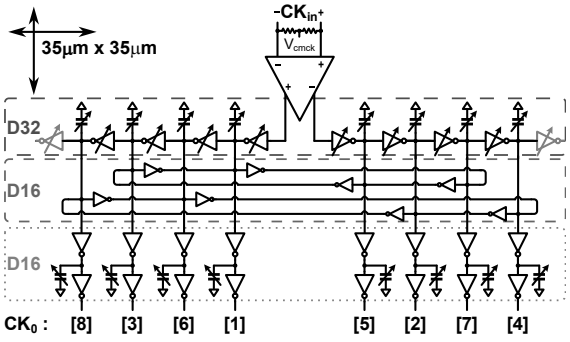


Fig. 1. Proposed 8-phase generator, simplified diagram. Highlighted top to bottom are delay line, couplers and fine-tuning. Input clock buffer as in [13].

to compensate the statistical mismatch due to manufacturing tolerances and process variations. Significant delay reduction is achieved by means of feed-forward ring couplers, which was proven in [11], [15], [16] to increase the speed of ring oscillators. Given the reduced strength needed in the feed-forward network compared to the main delay line, the couplers are implemented as tri-state inverters, allowing an optional extension of the operating range of frequencies while retaining the rail-to-rail swing on each node. The output phases are then

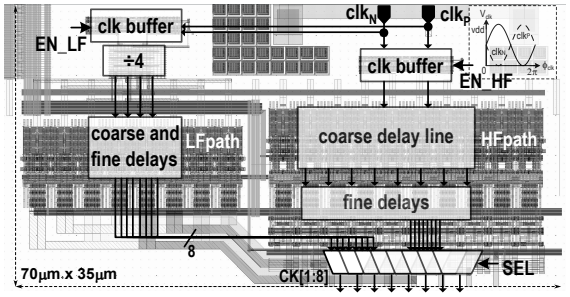
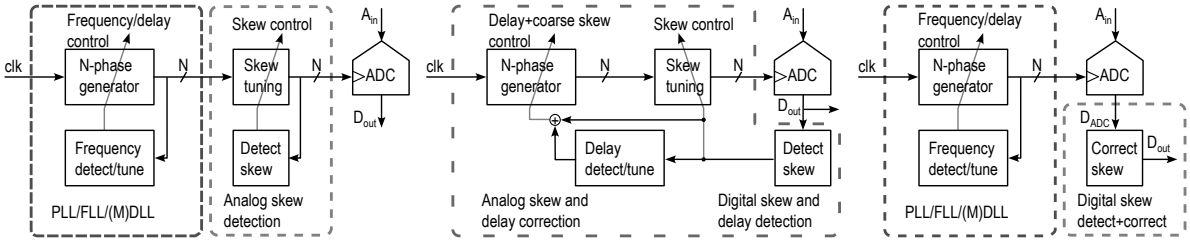


Fig. 2. Diagram and layout. The two paths are mutually exclusive.

delivered to the converter via MUXes, which optionally select a different path from the input clock at lower frequency as in fig. 2. It extends the operating range outside the one allowed by the delay of the inverters, retaining full supply swing on the nodes of interest unlike supply-tuned solutions. The auxiliary path operates with frequency division by 4 in two stages, consecutively duplicating each input into quadrature outputs.



(a) Analog [5], [9] (b) Mixed-signal, proposed and [12] (c) Digital [17]

Fig. 3. Possible clocking strategies for interleaved converters. Both the average and the individual phase delay must be controlled.

A. Main generator

Each stage in the delay line is implemented as the parallel of a CMOS inverter and the tri-state inverters of fig. 4. The selection of the number of parallel inverters allows programming the driving strength of each stage in ultra-coarse steps. A 4-bit bank of binary-scaled coarse capacitors has units selectively connected to the stage output or grounded to mitigate the impact of the bottom-plate parasitic capacitance. The feed-

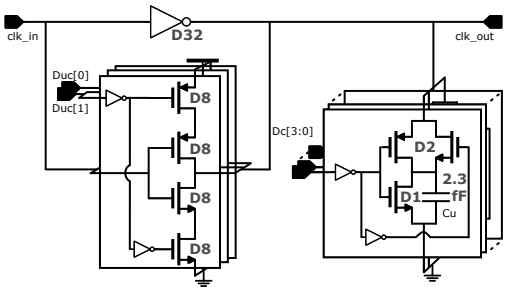
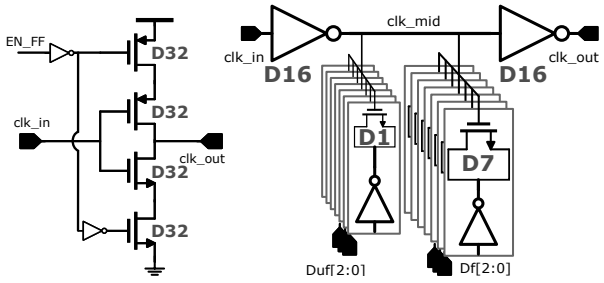


Fig. 4. Coarse and Ultra-Coarse tuning cell with 100fs delay resolution.

forward couplers are implemented as tri-state CMOS inverters like in fig. 5a. The selection switches are sized to reduce the equivalent strength of the couplers to approximately half of that of the main chain. As the output node of the coupler and



(a) Tri-state couplers (b) Fine and ultra-fine cells

Fig. 5. Feed-forward couplers (left) and tunable tap buffer (right).

main delay stages are shorted together, the strength ratio is to first order preserved in the delay tuning range, improving the reliability of the coupling. The tuning via nMOS capacitors of the tap buffers of fig. 5b brings the delay compensation resolution down to 10fs on the sampling edge, needed to achieve the target performance of the converters driven by the 8 phases. The MOS banks are segmented in two 3-bit binary-scaled sections with overlapping characteristic, to ensure good coverage of the delay range and allow for a compact layout of the cell, improving the reliability of the correction strategy.

B. Low-frequency generator

Fig. 6 shows the detailed low-speed path. The clock buffer output is fed first to the "*windmill*" divider of [18] which converts 2-phase inputs to 4-phase outputs E[3:0] while dividing the frequency by 2. The 4 output signals are then gated and buffered to the novel "*watermill*" divider, further dividing the frequency by 2 to generate 8x 25% duty-cycle clock phases F[7:0]. Pair-wise OR combination restores duty-cycle to 50%.

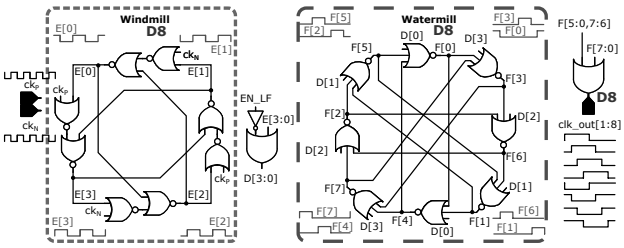


Fig. 6. Low-frequency path schematic, with gating logic to prevent oscillation.

III. Calibration algorithm

The clock skew calibration routine is demonstrated as a foreground feedback loop with a sine wave input signal applied to the ADC, shown in fig. 7. The output decimated data available from the converter is rearranged in 8 streams, one for each of the Rank-1 samplers of the ADC. A sine-wave is fit to each of the data streams to estimate the phase difference among them. The individual tap delay is estimated from the fitted phase. For background operation, skew estimation on a live input using algorithms such as [12] can also be used. An excess delay over the ideal $2\pi/8$ between consecutive channels indicates that the control code for the corresponding delay line should be decremented, and *vice versa*. The sign of the delay error for each channel pair, with one chosen as reference, is sent to a digital accumulator, driving the corresponding delay unit. This scheme implements a sign-LMS loop for each one

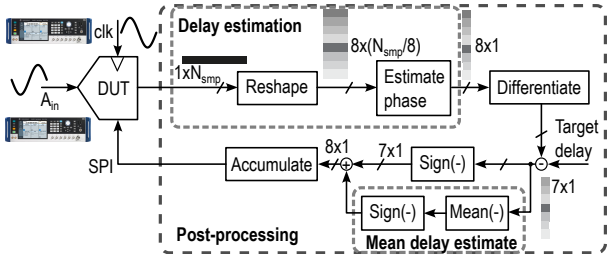


Fig. 7. Proposed calibration diagram and measurement setup.

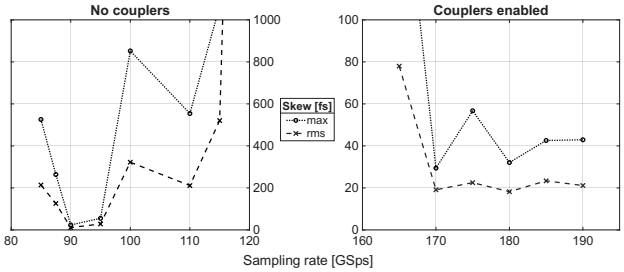


Fig. 9. Residual measured skew *vs.* sampling rate after calibration.

of the channel pairs, attempting to center each channel to its neighbors as in [12]. A second loop acts instead on the average delay of the inverter chain, conditioning all controls simultaneously and acting as a DLL. Although each control word tunes multiple delays, independent control loops can still be used without risk of instability within the correction range due to the cyclic nature of the error definition.

IV. Measurements

The clocking system is implemented in 5nm FinFET technology to clock a 175GSps ADC [2]. The input sinusoidal differential signal and clock come from two reference-locked R&S SMA100B generators. The decimated digital ADC output data is then read out and sent to MATLAB® post-processing scripts.

A. Timing skew calibration

The nominal behavior of the proposed calibration is evaluated from a fresh reset of the chip, starting with all control-words to mid-range. Fig. 8 shows the results of each step of the proposed calibration procedure, plotting estimated skew and spectral purity from a sine-wave input conversion. To speed

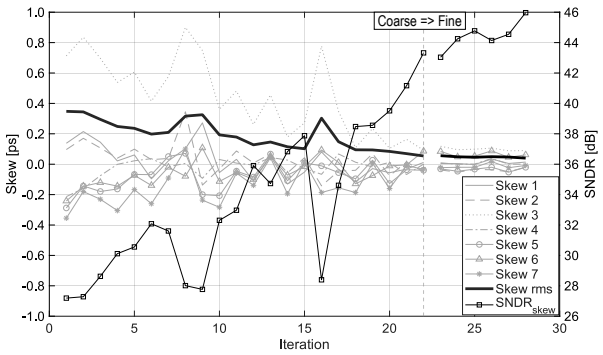


Fig. 8. Skew and spectral purity estimated from measured data. Each iteration is a decimated data capture of a 20GHz sinewave input to the ADC.

up the calibration, the coarse tuning is varied first until the estimated skew falls below 150fs. The fine-tuning is then activated to reach the target <40fs rms error. Fig. 9 shows measurements of the post-calibration residual skew error before (left) or after enabling couplers (right) for the corresponding frequency ranges. Wider tuning ranges are possible by modifying the power supply. The stopping condition in these measurements is set to an estimated 20fs rms error.

B. Jitter estimation

Using ADC data from an input signal frequency sweep it is possible to estimate the total sampling noise. This is useful to estimate the sampling clock jitter, although it is not possible to separate the contributions due to the input source phase noise, to the clock source phase noise, the sampling circuits or to the internal clocking circuitry. The proposed methodology is based on the observation that the SNR of the output data (excluding harmonics and interleaving spurs) has a specific frequency trend due to the sampling jitter. A simplified expression in terms of the power of the individual contributions is:

$$\mathrm{SNR}(f_{\mathrm{sig}}) = \frac{\sigma^2_{\mathrm{sig}}(f_{\mathrm{sig}})}{\sigma^2_v + \sigma^2_q + \sigma^2_{\mathrm{sig}}(f_{\mathrm{sig}}) 4\pi^2 f^2_{\mathrm{sig}} \sigma^2_t} \tag{1}$$

The variances in (1) refer to the signal (σ^2_{sig}), the additive voltage noise (σ^2_v), the quantization error (σ^2_q) and all the sampling time errors (σ^2_t). Assuming data coming from an output power-regulated frequency sweep, the inverse of the SNR can be written as:

$$\begin{aligned} \mathrm{SNR}(f_{\mathrm{sig}})^{-1} &= \mathrm{SNR}(0)^{-1} + (2\pi\sigma_t)^2 f^2_{\mathrm{sig}} \\ &= \begin{bmatrix} (2\pi f_{\mathrm{sig}})^2 & 1 \end{bmatrix} \begin{bmatrix} \sigma^2_t \\ \mathrm{SNR}(0)^{-1} \end{bmatrix} \end{aligned} \tag{2}$$

The regression of (2) can be solved for the timing error power to verify that the clocking jitter is in the expected range, as shown in fig. 10. The results obtained in this way are

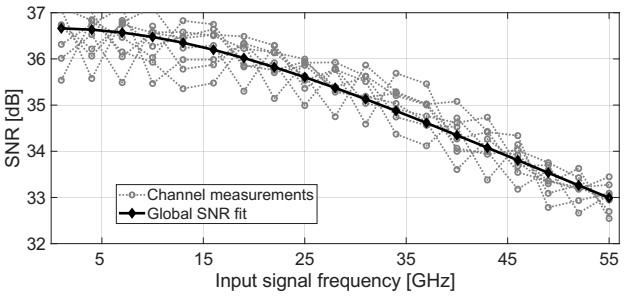


Fig. 10. Rank-1 measured SNR and result of the fitting described in (1).

sensitive to other sources of error not accounted for in (1): for instance, error due to timing skew shows the same trend as the one for jitter, and is as such indistinguishable. To

mitigate the impact of interleaving on the noise estimation, the regression is performed separately per Rank-1 data from the ADC. The residual sources of error thus only affect the frequency-independent part of the regressor. Results of the estimation for each channel across various output signal levels are tabulated in table I. This method is a pessimistic estimation

TABLE I
ESTIMATED JITTER FROM MEASUREMENTS OF VARIOUS SAMPLES.

Sample no.	1	2	3
Power [dBFS]	-2	-4	-2
$\sigma_{t,0}$ [fs]	45.1	45.6	48.7
$\sigma_{t,1}$ [fs]	48.1	47.5	47.1
$\sigma_{t,2}$ [fs]	45.7	49.9	48.5
$\sigma_{t,3}$ [fs]	40.4	47.8	48.8
$\sigma_{t,4}$ [fs]	49.3	46.9	48.2
$\sigma_{t,5}$ [fs]	48.1	45.2	49.0
$\sigma_{t,6}$ [fs]	45.9	48.3	49.2
$\sigma_{t,7}$ [fs]	46.7	46.2	49.9
$\sigma_{t,\text{rms}}$[fs]	46.2	47.2	48.7

of the performance of the clocking, as the contribution of other blocks on the clock chain cannot be isolated in this way. Nonetheless, the measured results match the expected values from simulation, whose breakdown allocates about 30fs rms jitter to the clocking, out of the total 50fs sampling noise.

C. Power consumption

The power consumption at 3 different supply voltages with mid-range settings of all delay controls is shown *vs.* clocking frequency and total sampling rate in fig. 11. The divider path

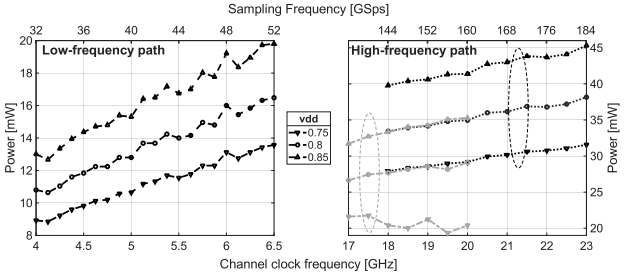


Fig. 11. Measurement of power vs frequency of the different paths. Consumption without enabling the couplers is in gray on the right.

(left) is only shown in a range of frequencies close to its maximum. The main path (right) benefits in speed from the feed-forward coupling, at the price extra power.

V. CONCLUSION

This work demonstrates a multi-phase clocking solution for wireline converters. It achieves $>10\%$ frequency operating range around the nominal differential sinewave input, with $<$20fs rms timing error among the 8 generated phases. Power consumption is <45mW from a 0.85V supply. Either disabling the couplers on the main path, or switching to a path with static frequency dividers enables lower rates. The total area occupation in 5nm FinFET shown in fig. 2 is $70\mu\text{m} \times 35\mu\text{m}$.

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