A Dual-Mode 45-Gb/s NRZ and 58-Gb/s PAM-4 Bandwidth Efficient VCSEL Transmitter with Hybrid Equalization in 28-nm CMOS

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***Abstract*— This paper presents a bandwidth efficient vertical-cavity surface-emitting laser (VCSEL) voltage-mode transmitter (TX) that extends the electro-optical (E–O) bandwidth beyond the limitation of driving the VCSEL using a hybrid equalization technique combining complex-zero shunt peaking (CZ-SP) and a 3-tap asymmetric feed-forward equalizer (FFE). Fabricated in a 28-nm CMOS process, the TX achieves 45-Gb/s NRZ and 58-Gb/s PAM-4 operation with a 14.9-GHz commercial multimode VCSEL. This corresponds to a bandwidth efficiency (data rate / VCSEL bandwidth) of 3.89 bps/Hz, the highest among serializer-integrated VCSEL TXs. The measured energy efficiency is 3.76 pJ/bit for NRZ and 2.31 pJ/bit for PAM-4.**

Keywords—28-nm, CMOS, NRZ, PAM-4, vertical-cavity surface-emitting laser (VCSEL), voltage-mode, complex-zero shunt peaking (CZ-SP), feed-forward equalizer (FFE), hybrid equalization, transmitter (TX)

I. Introduction

The rapid growth of artificial intelligence (AI) workloads has increased the demand for high-throughput and energy-efficient interconnects in data centers and high-performance computing (HPC) systems. To meet these demands, optical interconnects have emerged as a key solution to overcome the bandwidth, power, and reach limitations of electrical interconnects. In particular, vertical-cavity surface-emitting laser (VCSEL)-based transmitters (TXs) employing multimode fibers provide a cost-effective solution for short-reach links. However, in VCSEL-based TXs, interface parasitics in the electrical current driving network (E–E) and the nonlinearity and intrinsic bandwidth limitations of the electrical-to-optical (E–O) response pose significant challenges for high-speed operation.

Various techniques have been proposed to address the nonlinearity and bandwidth limitations of VCSEL-based TXs. Nonlinear equalization methods improve signal quality by mitigating distortion and inter-symbol interference (ISI) [1], [2], but their effectiveness is limited since they do not fundamentally remove the intrinsic complex-pole behavior of the VCSEL. On the other hand, a complex-zero continuous-time linear equalizer (CZ-CTLE) has been proposed to compensate for this behavior, which achieves efficient bandwidth extension and favorable group delay characteristics [3]. However, such approaches may increase overall system complexity, as the reduced driver swing caused by source degeneration often needs to be restored through additional amplification stages.

In this work, we present a single-ended voltage-mode (VM) driver-based VCSEL TX employing a hybrid equalization scheme that combines complex-zero shunt peaking (CZ-SP) with a 3-tap asymmetric feed-forward equalizer (FFE). The CZ-SP is simply implemented as a parallel load at the driver output, enabling compensation of the VCSEL's complex poles while reducing the dependence of E–E bandwidth on modulation swing. The asymmetric FFE mitigates bias-dependent VCSEL nonlinearity by enabling independent control of rising and falling transitions, while enhancing the high-frequency response. As a result, this work achieves the highest bandwidth efficiency (data rate / VCSEL bandwidth) of 3.89 bps/Hz among serializer-integrated VCSEL TXs.

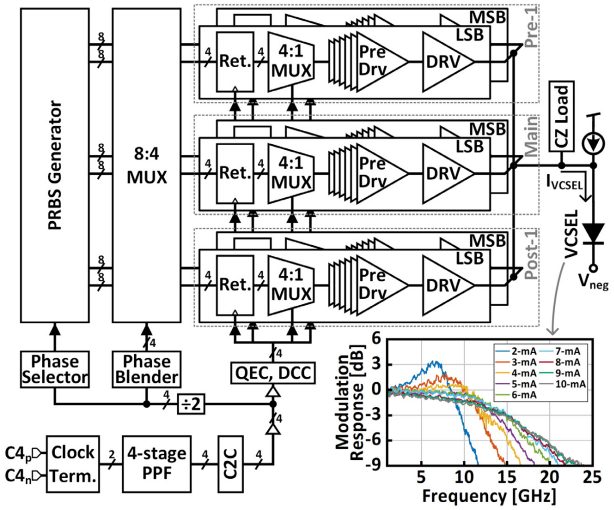

Fig. 1. Proposed VCSEL transmitter architecture.

II. Proposed VCSEL TX Architecture & Circuit Implementation

Fig. 1 shows the overall architecture of the proposed VCSEL TX. The clock path receives differential quarter-rate clocks and generates four-phase clocks. A poly-phase filter (PPF) is used to generate quadrature phases in the 6–13 GHz range. To compensate for clock distortion caused by process variation and routing, quadrature error correction (QEC) and duty-cycle correction (DCC) blocks are included. The data path employs a PRBS generator to produce a data sequence, where MSB and LSB data streams are generated in 8-bit parallel form. For NRZ operation, the MSB and LSB are generated with identical logic values, whereas for PAM-4 operation, they are generated with different logic values to

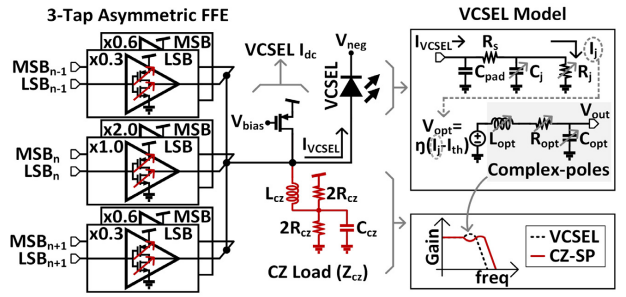

Fig. 2. Hybrid equalization scheme with CZ-SP and 3-tap asymmetric FFE.

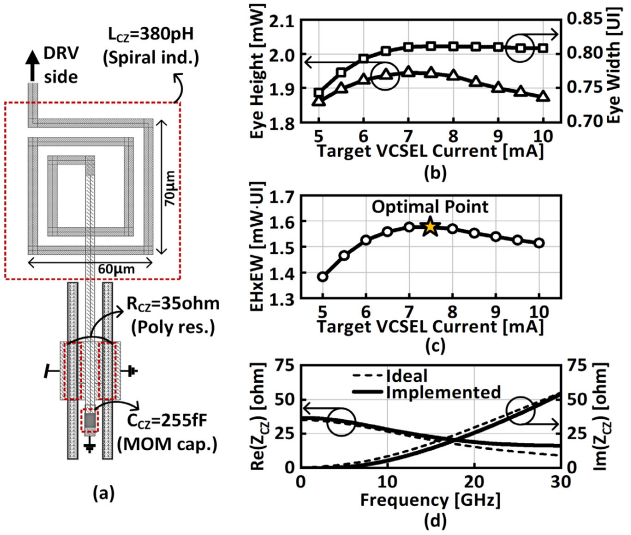

Fig. 3. Implementation and optimization of the CZ load: (a) the CZ load layout, (b) EH and EW, (c) EH×EW at 45-Gb/s NRZ simulation under the CZ load target optimization current, (d) implementation results compared to an ideal RLC circuit.

form four levels. The generated data are then serialized to 8:1. The serialized data are delivered to the VCSEL through a pre-driver and a main driver. The VCSEL is driven through its anode, where a PMOS current source sets the driver output common-mode voltage to VDD/2, ensuring sufficient voltage headroom while providing the DC bias current to the VCSEL. The cathode is negatively biased to provide voltage across the VCSEL for the required bias current, exceeding the driver supply voltage.

A. Hybrid Equalization

Fig. 2 illustrates the proposed hybrid equalization applied at the driver output stage. A 3-tap asymmetric FFE (pre-1, main, post-1) is introduced to compensate for high-frequency loss around the Nyquist frequency. To address the nonlinear dynamics of the VCSEL, the PMOS/NMOS strength ratio is independently controlled for each tap and MSB/LSB path, enabling an asymmetric implementation. This helps reduce the influence of the nonlinear dynamics of the VCSEL, particularly in multi-level modulation schemes. The elements shown on the right represent an equivalent circuit model [4] of the VCSEL. Based on this model, the E–O modulation response can be expressed as a second-order system exhibiting a complex-pole pair. These poles introduce an underdamped response characterized by second-order roll-off and ringing, leading to increased ISI, which is particularly critical for PAM-4 signaling. To address this issue, a CZ-SP technique is proposed. The CZ-SP introduces

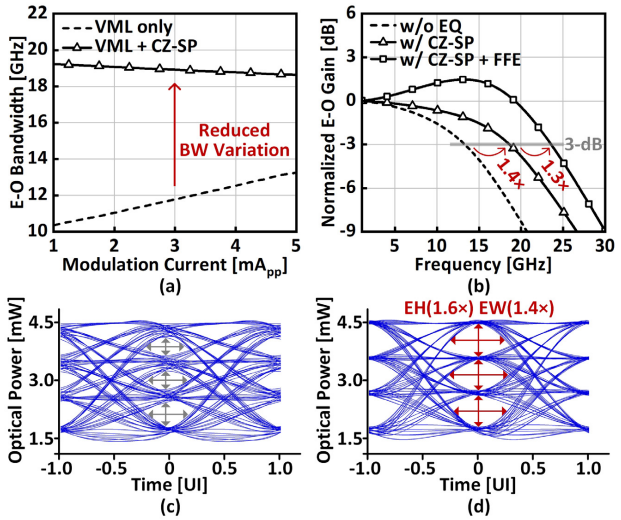

Fig. 4. Simulation results comparing conventional and proposed VCSEL driving methods in frequency and time domains: (a) E–O bandwidth versus modulation swing, (b) normalized E–O gain versus frequency, and PAM-4 eye diagrams at 58 Gb/s (c) without and (d) with hybrid equalization.

a complex-zero (CZ) to cancel the intrinsic complex-pole pair of the VCSEL and is implemented by connecting a CZ load in parallel with the VM driver. Since this parallel structure is applied at the driver output, it can be readily combined with other equalization techniques, such as the asymmetric FFE used in this work. As a result, the dominant bandwidth-limiting poles are suppressed, leading to an overall extension of the TX bandwidth.

Fig. 3 shows the optimization and implementation of the CZ load used in the proposed CZ-SP. Fig. 3(a) shows the layout of the CZ load. In this work, a bias current of 7.5 mA with a 5 mA_{pp} modulation swing is used as the design target. Since the large-signal behavior of the VCSEL depends on which bias point the complex-pole pair is compensated, the optimal bias point must be determined during the design. Fig. 3(b) and (c) show how this point is selected. They show the simulated 45-Gb/s NRZ eye diagram characteristics when the CZ load is tuned over a range from 5 mA to 10 mA with 0.5-mA steps. Both eye height (EH) and eye width (EW) are evaluated, and their product (EH×EW) is used as a simple metric. As shown in Fig. 3(c), the maximum value appears around 7.5 mA, which is chosen as the optimal point. The CZ load is then designed to match the complex-pole pair of the VCSEL at this bias condition. In practice, parasitics are unavoidable. Fig. 3(d) compares the impedance of the implemented CZ load with the ideal RLC response. The in-band response is close to the ideal case, indicating that the implementation is sufficiently accurate.

Fig. 4(a) shows the simulated E–O bandwidth versus modulation swing, obtained by sweeping the VM driver output impedance at a 7.5 mA bias current. In a VM driver, the output impedance varies with modulation swing, resulting in swing-dependent bandwidth. As shown in Fig. 4(a), the bandwidth exhibits non-negligible sensitivity to the modulation swing magnitude. This limits modulation swing control at high speeds, and large-signal impedance mismatch in the VM driver introduces additional nonlinearities, which is particularly critical for PAM-4 operation. When the CZ-SP is used together with the VM driver, this dependence is alleviated. The parallel CZ load reduces the effective load impedance seen by the VM driver, thereby suppressing

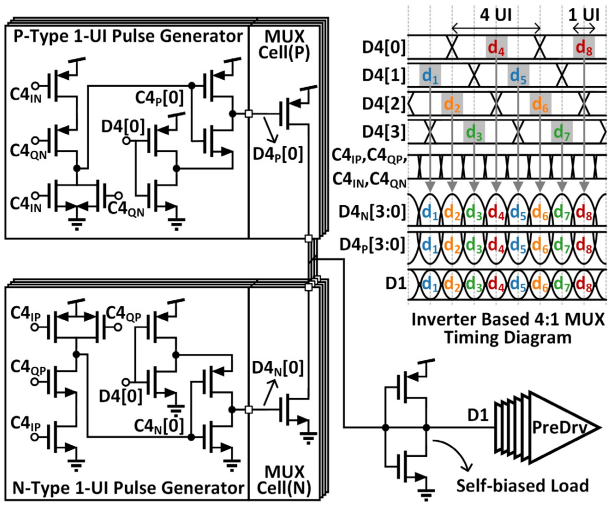

Fig. 5. Proposed inverter-based 4:1 MUX and its timing diagram.

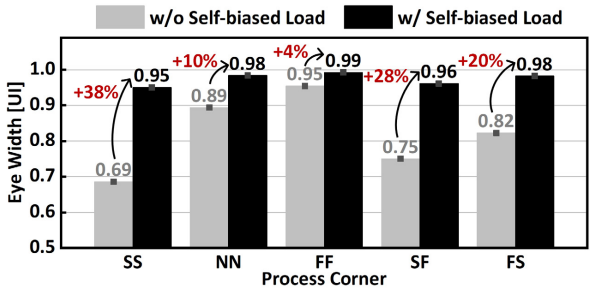

Fig. 6. Simulated eye width of the 4:1 MUX at 45 Gb/s across five process corners with and without the self-biased load.

bandwidth variation over the swing range while compensating for the E–O complex poles of the VCSEL.

Fig. 4(b) to (d) show the impact of the proposed hybrid equalization on both the system bandwidth and the large-signal behavior. Fig. 4(b) shows the normalized E–O frequency responses at a bias current of 7.5 mA, with the VM driver impedance set for a 5 mA_{pp} swing under different equalization conditions. Compared to the conventional VM driver, the CZ-SP alone extends the bandwidth from 13.3 GHz to 18.6 GHz (1.4×). When a 2-tap FFE operating at 45-Gb/s is added, the bandwidth further increases to 23.6 GHz, achieving an additional 1.3× improvement. Fig. 4(c) and (d) show the simulated PAM-4 eye diagrams at 58-Gb/s under the same bias and swing conditions, without and with the proposed hybrid equalization. Without equalization, the eye openings are degraded due to bandwidth limitation and level-dependent distortion. With the proposed CZ-SP and 2-tap asymmetric FFE, all three eye openings are significantly improved. Averaged across the three inner eye openings, the EH and EW increase by 1.6× and 1.4×, respectively. These results show that the proposed approach improves not only the small-signal bandwidth but also the large-signal behavior.

B. 4:1 Multiplexer

Fig. 5 shows the inverter-based 4:1 multiplexer (MUX) implemented in this work along with its timing diagram. To achieve high-speed operation in a compact single-ended TX compatible with an inverter-based pre-driver, an inverter-based 4:1 MUX is used. The 4:1 MUX consists of four MUX cell (N and P) pairs. Each MUX cell pair is driven by the complementary operation of N-type and P-type 1-UI pulse generators. The 1-UI pulse generator adopts a floating state

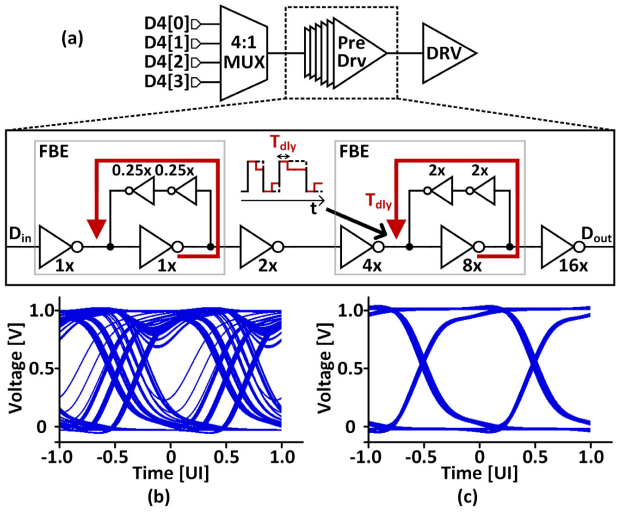

Fig. 7. (a) Pre-driver block diagram with feedback equalizer. Simulated eye diagrams at 45 Gb/s (b) without and (c) with the feedback equalizer.

	Block Name	Area [mm²]
1	Clock Path	0.021
2	Pattern Generator	0.003
3	Serializer	0.004
4	Driver	0.002
5	CZ Load	0.016

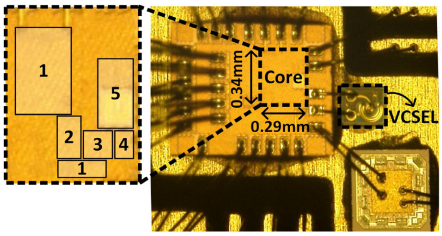

Fig. 8. Chip micrograph of the VCSEL transmitter with corresponding block areas.

free architecture to achieve low-jitter and high-speed operation [5]. In addition, the 4:1 MUX employs a self-biased load at the output, which effectively reduces deterministic jitter. A well-known drawback of inverter-based MUX structures is their sensitivity to process variations. The proposed architecture improves robustness against such variations. Fig. 6 shows the simulated EW of the 4:1 MUX at 45-Gb/s NRZ across five process corners. The proposed structure maintains deterministic jitter within 0.01–0.05 UI across all corners, a significant improvement over the 0.05–0.31 UI observed without the self-biased load. Additionally, the self-biased load is implemented as a diode-connected inverter which can be easily extended to an active inductor for higher-speed operation.

C. Feedback Equalizer

A low-impedance driver results in significant input capacitance. Directly driving this load with the 4:1 MUX leads to a substantial increase in its required size, which in turn increases the area and power consumption of both the data and clock paths. To mitigate this, a fan-out-of-2 multi-stage inverter chain is used as a pre-driver, and the 4:1 MUX is optimized for low power. However, such an inverter chain is limited by ISI at high data rates. To overcome this issue, a compact feedback equalizer (FBE) is introduced to effectively suppress ISI in the pre-driver. The FBE operates similarly to a 2-tap FFE with main and post-1 taps [6]. The feedback loop delay (T_{dly}) is approximately 18 ps, which sets a peak response around 28 GHz, making the structure increasingly effective at higher data rates. Fig. 7(b) and (c) show the simulated 45-Gb/s NRZ eye diagrams of the pre-driver without and with FBE, respectively. These results confirm that the FBE-based inverter chain significantly improves signal integrity under high-speed operation.

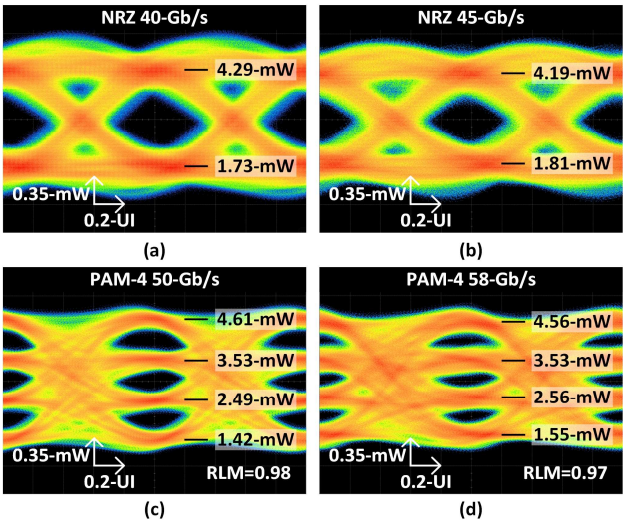

Fig. 9. Measured optical eye diagrams: NRZ with CZ-SP and 3-tap symmetric FFE at (a) 40 Gb/s and (b) 45 Gb/s, PAM-4 with CZ-SP and 2-tap asymmetric FFE at (c) 50 Gb/s and (d) 58 Gb/s.

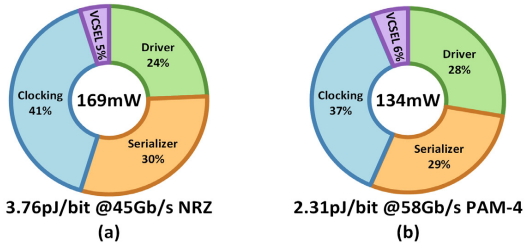

Fig. 10. Power breakdown of the proposed VCSEL TX at (a) 45-Gb/s NRZ and (b) 58-Gb/s PAM-4 operation

III. Measurement Results

Fig. 8 shows the chip micrograph of the proposed VCSEL TX fabricated in a 28-nm CMOS process, integrated with a commercial multimode VCSEL exhibiting a 14.9-GHz bandwidth at a bias current of 7.5 mA. The optical signal is coupled into a cleaved fiber and measured using a high-speed optical-to-electrical converter (Keysight N7004A) and a real-time oscilloscope (Keysight MSOV334A).

Fig. 9 presents the measured optical eye diagrams at a bias current of 7.5 mA for different data rates using a PRBS-7 pattern. Fig. 9(a) and (b) show the NRZ eye diagrams at 40 Gb/s and 45 Gb/s, respectively. The NRZ results are obtained using the CZ-SP combined with a 3-tap symmetric FFE. The optical modulation amplitude (OMA) values are 2.56 mW and 2.38 mW, respectively, where the reported OMA is de-embedded to account for the 3-dB coupling loss. Fig. 9(c) and (d) show the PAM-4 eye diagrams at 50 Gb/s and 58 Gb/s, respectively. Since PAM-4 operation is more sensitive to VCSEL nonlinearity, a 2-tap (main, post-1) asymmetric FFE is used together with CZ-SP. The measured OMA values are 3.19 mW and 3.01 mW, respectively. The corresponding level separation mismatch ratio (RLM) values are 0.98 and 0.97. Fig. 10 presents the measured power breakdown of the proposed VCSEL TX under different modulation schemes at the maximum achievable data rates.

Table I shows a performance summary and a comparison of the proposed VCSEL TX with recent works. Despite the limited VCSEL bandwidth of 14.9 GHz, this work achieves high-speed operation, attaining the highest bandwidth efficiency of 3.89 bps/Hz and an OMA of 3.01 mW while maintaining competitive energy efficiency.

TABLE I. Comparison with State-of-the-Art VCSEL TX

Reference	JSSC'22 [1]	JSSC'25 [2]	JSSC'25 [3]	CICC'25 [7]	**This Work**	
Technology	40-nm CMOS	40-nm CMOS	22-nm FinFET	22-nm SOI	28-nm CMOS	
Serializer	Quarter-rate	Quarter-rate	Quarter-rate	Half-rate	Quarter-rate	
Modulation	PAM-4	PAM-4	NRZ	PAM-4	NRZ	PAM-4
Data Rate [Gb/s]	56	56	64	100	45	58
VCSEL BW [GHz]	17	19	26	27	14.9	
Equalization	2-Tap Asym. FFE	CTLE + 2-Tap FFE	CZ-CTLE	8-Tap FFE	**CZ-SP + 3-Tap FFE**	**CZ-SP + 2-Tap Asym. FFE**
OMA [mW]	0.81	1.18	3.65	1.5	**2.38**	**3.01**
Data Rate / VCSEL BW [bps/Hz]	3.3	2.95	2.46	3.7	**3.02**	**3.89**
Energy Efficiency [pJ/bit]	1.73†	2.05*†	1.3	4.3	3.76	2.31

* Includes PLL power. † Excludes VCSEL power.

IV. Conclusions

This work presents a VCSEL TX employing hybrid equalization combining CZ-SP and 3-tap asymmetric FFE, achieving 45-Gb/s NRZ and 58-Gb/s PAM-4 operation with a limited bandwidth of 14.9-GHz VCSEL. The proposed design achieves a high bandwidth efficiency of 3.89 bps/Hz along with a large OMA of 3.01 mW. These results demonstrate that the proposed approach effectively overcomes the intrinsic bandwidth limitation of the VCSEL driving.

Acknowledgment

This work was supported by the Institute of Information and communications Technology Planning and evaluation (IITP) funded by the Korea Government (MSIT) Development of Tbps/mm chiplet interface IP and silicon photonics technology for AI and vehicle SoC, under Grant RS-2023-00222171. The chip fabrication and EDA tools were supported by the IC Design Education Center (IDEC), Korea.

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