An Ultra-Compact, 19.9–47-GHz LNA with 2.18–3.97-dB Noise Figure and ±0.5 dB Gain Ripple in 40nm CMOS

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***Abstract*—This paper proposes an ultra-low-noise wideband low-noise amplifier (LNA) fabricated in a 40-nm bulk CMOS process for 5G/6G applications. Both excellent noise figure (NF) and wideband input matching are achieved through parallel gate-source coupling and large-size transistors. A transformer-based matching network is introduced to improve inter-stage matching, extend bandwidth, and enhance noise performance. Additionally, an mild electrical decoupling (MED) current-reuse technique is utilized in the last two stages to ensure stability and improve gain flatness. Besides, two wideband high-Q transformers with 8-shaped winding are implemented to minimize performance degradation. Measured results show that the proposed LNA achieves a maximum gain of 16.9 dB with a 3-dB bandwidth of 19.9–47 GHz (81% fractional bandwidth). The noise figure (NF) ranges from 2.18 to 3.97 dB, with an average NF of 2.92 dB across the 3-dB bandwidth. The IP_{1dB} and IIP3 are –21.2 to –14.9 dBm and –12.4 to –8.3 dBm, respectively. The LNA consumes 13.9 mW dc power and occupies an ultra compact core area of 0.048 mm^2.**

***Index Terms*—low noise amplifier (LNA), low noise figure (NF) wideband, compact, gain flatness, current-reuse**

I. Introduction

With the standardization of multiple non-contiguous New Radio (NR) Frequency Range 2 (FR2) bands by 3GPP, millimeter-wave multi-band phased arrays have become a key enabling technique for future high-capacity systems. Large-scale phased arrays offer superior beamforming performance and multi-tasking ability, yet their multi-channel architecture leads to a drastic increase in overall area. As the first active block in the receiver chain, the low-noise amplifier (LNA) dominates the system noise figure (NF) and input matching performance, making it critical to achieve wide bandwidth, low noise, and high compactness simultaneously for large-scale array implementations.

Traditionally, dual-path noise canceling is an effective technique for achieving ultra-low NF [1]. This work achieves a minimum NF of 2.65 dB with promising bandwidth. However, the dual-path structure roughly doubles both area and power consumption, which significantly degrades its figure-of-merit (FoM). In [2], a quad-coil coupled transformer (QCCT) is used to integrate most inductors from the two amplification paths. A minimum NF of 2.79 dB is achieved with only 0.089 mm^2 core area, enabled by the QCCT technique. Moreover, power consumption is further reduced via a 0.6-V supply voltage. However, it still suffers from narrowband noise matching. When using dual-path noise canceling, phase alignment matches theoretical predictions only over a narrow bandwidth, typically centered at the design frequency, resulting in degraded NF at off-center frequencies. The work in [3] presents a novel solution using a co-directional tri-coil transformer and achieves a minimum NF of 2.17 dB. However, it consumes 14.9 mW of dc power and occupies 0.27 mm^2 core area owing to its three-stage common-source (CS) topology. Its bandwidth and gain flatness are also less competitive.

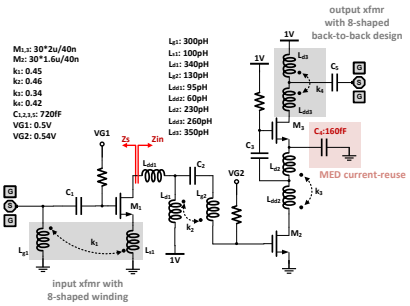
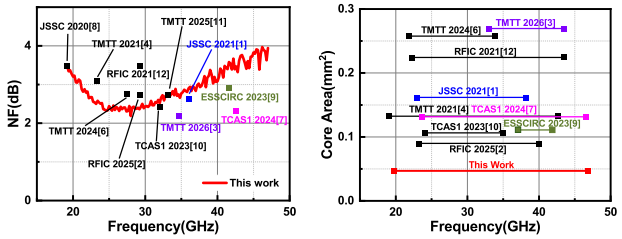


Fig. 1: Schematic of the proposed wideband LNA using mild electrical decoupling (MED) current-reuse topology.



(a) (b)

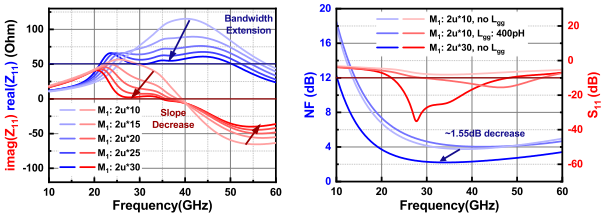
Fig. 2: Performance comparisons with state-of-the-arts: (a) Measured noise figure (minimum NF marked by dots), (b) core area versus 3-dB bandwidth range.

A CS-2CS LNA with mild electrical decoupling (MED) current-reuse topology, incorporating transformer-based inter-stage matching and two transformers with 8-shaped winding, is proposed to simultaneously balance and optimize noise, power, bandwidth and area performance, as shown in Fig. 1. This prototype achieves excellent performance across multiple key metrics. A minimum NF of 2.18 dB is achieved with only 13.9 mW dc power consumption and ultra small core area of 0.048 mm^2. Moreover, a 27.1 GHz bandwidth is realized with a gain ripple of only ±0.5 dB. To the best of the authors' knowledge, this work achieves the highest FoM among all reported bulk CMOS LNAs in this frequency range. Fig. 2 presents a comprehensive performance comparison between this work and state-of-the-arts versus 3-dB bandwidth range.

II. Circuit Design Techniques of The Proposed LNA

A. Input Matching and NF Optimization

In [4], a series inductor placed between the gate shunt inductor and the transistor gate, denoted as L_{gg}, is used to form wideband input matching. However, this additional series inductor introduces significant area overhead and noise contribution from its parasitic resistance. This work presents an alternative approach for wideband input matching. Fig. 3(a) plots the real (blue) and imaginary (red) parts of the input impedance with the matching network as a function of the gate width of transistor M_1. As the gate width increases, the real part of the input impedance achieves a wider bandwidth and converges to 50 Ω, while the imaginary part exhibits a reduced slope and approaches 0 Ω. As shown in Fig. 3(b), the proposed strategy of using large transistors without L_{gg} achieves excellent noise and matching performance with reduced chip area, despite an acceptable increase in power consumption.

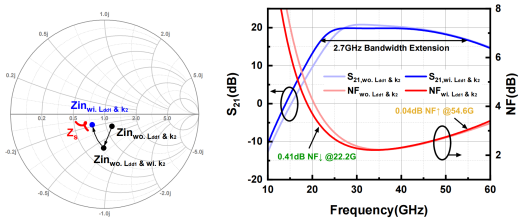


(a) (b)

Fig. 3: (a) Simulated real and imaginary part of the input impedance for different sizes of M_1. (d) Simulated S_{11} and NF for different input matching strategies.

B. Transformer-Based Inter-Stage Matching Network

With Zs and Zin indicated in Fig. 1, the inter-stage matching dominated by k_2 and L_{dd1} is analyzed. Fig. 4(a) shows the conjugate impedance Zs^* of the inter-stage source impedance Zs, and $Zin_{\text{wo. L}_{dd1}\text{ \& k}_2}$ denotes the original inter-stage input impedance without L_{dd1} and k_2. All simulations are performed at the center frequency of 33.5 GHz within the operating band. Since the real part of $Zin_{\text{wo. L}_{dd1}\text{ \& k}_2}$ is lager than that of Zs^*, we increase k_2 to move $Zin_{\text{wo. L}_{dd1}\text{ \& k}_2}$ to $Zin_{\text{wo. L}_{dd1}\text{ \& wi. k}_2}$, which has a lower real part accompanied by increased capacitive reactance. A series inductor is therefore required to match $Zin_{\text{wo. L}_{dd1}\text{ \& wi. k}_2}$ to the target impedance Zs^*. Finally, Zin is matched to $Zin_{\text{wi. L}_{dd1}\text{ \& k}_2}$ with L_{dd1} = 95 pH and k_2 = 0.46, as larger k_2 values are difficult to implement in reverse-coupling transformers due to unavoidable unidirectional coupling when connected to the transistor. Thanks to the well-matched inter-stage, the simulated bandwidth of the LNA is extended by 2.7 GHz. Simultaneously, due to the low-frequency bandwidth extension, the NF of the LNA is reduced by a maximum of 0.41 dB in the low-frequency band, while only a 0.04 dB maximum increase is observed in the high-frequency band, as shown in Fig. 4(b).



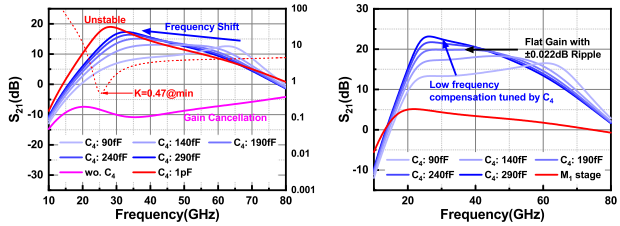
(a) (b)

Fig. 4: (a) Simulated Smith chart showing Zs and Zin during inter-stage matching optimization. (b) Simulated S_{21} and NF of the proposed LNA with and without L_{dd1} and k_2.

C. MED Current-Reuse Technique

In traditional current-reuse works [4][5], a decoupling capacitor between two reused stages is usually chosen to be pF-level to form reliable ac ground. However, in this work, the decoupling capacitor C_4 has a small capacitance and offer a mild electrical decoupling (MED) path for the two current-reused stages, as shown in Fig. 1. The MED capacitor C_4 is employed to balance low- and high-band gains, thereby fine-tuning the gain flatness of the overall LNA. In the current-reused stages depicted in Fig. 1, the stages of M_2 and M_3 operate at low and high bands, respectively. To minimize the area, source-degradation inductors are omitted for stages of both M_2 and M_3. This approach reduces noise contribution from these stages and effectively boosts gain. However, if C_4 is set as large as 1 pF, this structure faces severe stability issues, and the excessively high gain makes it difficult to achieve a wideband response, as shown by the red line in Fig. 5(a). Fig. 5(a) also shows the simulated S_{21} of the current-reused stages as C_4 is increase from 0 fF to 300 fF. When C_4 is removed, gain cancellation occurs as shown by the pink line. Since capacitive reactance decreases with increasing frequency for a fixed capacitance, the gain contribution of high-band stage becomes dominant earlier than that of low-band stage as C_4 increases. Thus, gain shifts from high frequencies to low frequencies as C_4 increases. Fig. 5(b) shows the simulated gain of the proposed LNA for various C_4. By tuning the low-frequency compensation via C_4, an optimal C_4 value of 190 fF is identified, achieving an ultra-low gain ripple of ±0.022

dB. The red lines shows the simulated gain of the first stage. Finally, a C_4 value of 160 fF is selected during post-simulation fine-tuning to achieve a balanced trade-off among gain flatness, relatively high gain, and large bandwidth.

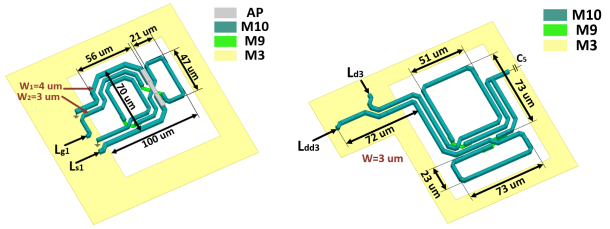


(a) (b)

Fig. 5: Simulated S_{21} of the (a) current-reused stages and (b) the proposed LNA varying different C_4 values.

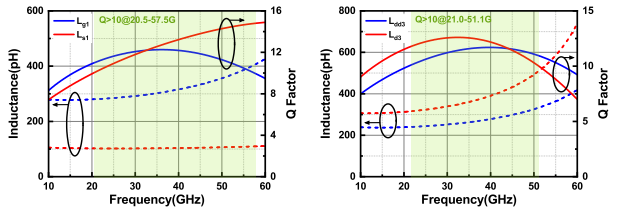
D. Wideband High-Q Transformer With 8-Shaped Winding

To achieve wideband high-Q performance, all passive components are implemented in a single metal layer except the tap layer. In addition, two transformers with 8-shaped winding are designed and used in the input and output matching networks, as shown in Fig. 6. While a medium coupling coefficient of about 0.4 is required, 8-shaped winding designs provide a flexible inductance tuning range. For transformers consisting of dual two-coil inductors as shown in Fig. 6(b), the 8-shaped back-to-back design can effectively minimize both the use of low-Q metal layers and the overlap area between the main and tap layers. According to electromagnetic simulation results shown in Fig. 7, all inductors in Fig. 6 have Q values larger than 10 across the 21.0-51.1 GHz band, which guarantees minimal performance degradation.



(a) (b)

Fig. 6: 3D layout of the proposed (a) input transformer with 8-shaped winding and (b) ouput transformer with 8-shaped back-to-back design.



(a) (b)

Fig. 7: Electromagnetic simulated inductances and Q factors of (a) the input transformer with 8-shaped winding and (b) the ouput transformer with 8-shaped back-to-back design.

III. Measurement Results

The chip is fabricated in 40-nm bulk CMOS process. The die micrograph is shown in Fig. 8. The LNA draws 13.9-mA from a 1-V dc supply and occupies an ultra-compact core area of 0.048mm^2.

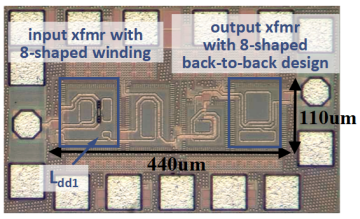
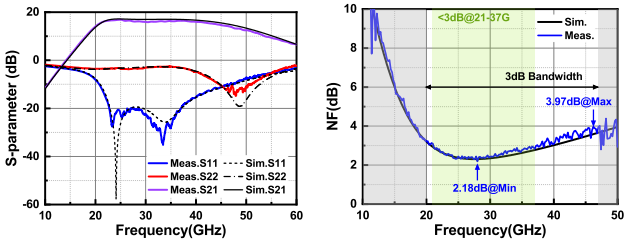


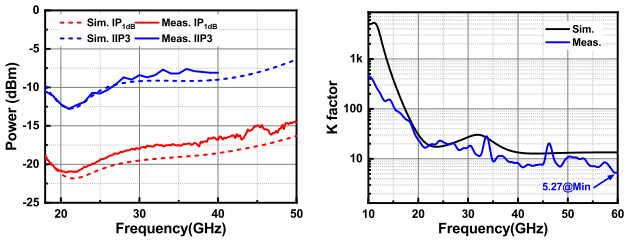
Fig. 8: Die micrograph of the proposed LNA.

Fig. 9(a) shows the simulated and measured S-parameters results. The LNA achieves a large 3-dB bandwidth of 27.1 GHz, covering 19.9-47 GHz with wideband input matching. Fig. 9(b) shows the simulated and measured NF. The LNA exhibits excellent noise performance with a minimum NF of 2.18 dB, a sub-3dB NF bandwidth of 16.4 GHz, and an average NF of only 2.92 dB. The simulated and measured IP_{1dB} and IIP3 is shown in Fig. 10(a). The IP_{1dB} is -21.2~-14.9 dBm across the 3dB-bandwidth. The IIP3 is -13.4~-8.3 dBm from 18 GHz to 40 GHz, due to the operating frequency limit of the power combiner used in the measurement. Fig. 10(b) shows the simulated and measured stability factor K, indicating a stable operation of the LNA.



(a) (b)

Fig. 9: Simulated and measured (a) S-parameters and (b) NF of the proposed LNA.



(a) (b)

Fig. 10: Simulated and measured (a) IP_{1dB}, IIP3 and (b) stability factor (K) of the proposed LNA.

Table I presents a comparison between this work and several previously reported state-of-the-art low-NF LNAs. The proposed LNA demonstrates ultra-low NF, large 3-dB wideband and high gain flatness with an ultra-compact chip area.

TABLE I: Performance Summary Of State-Of-The-Art Low-NF LNAs And This Work

Reference	**This Work**	[3] TMTT 2026	[1] JSSC 2021	[6] TMTT 2024	[2] RFIC 2025	[7] TCAS1 2024
Technology	**40-nm CMOS**	28-nm CMOS	28-nm CMOS	40-nm CMOS	65-nm CMOS	28-nm CMOS
Topology	**CS + MED-C.R.* 2CS**	3CS	D.P.-N.C.#	D.P.-N.C.#	D.P.-N.C.#	3Cascode
BW_{3dB} (GHz)	**27.1 (19.9-47)**	11(33.2-43.2)	15.3(22.9-38.2)	11.8(21.9-33.7)	17(23-40)	22.9(23.6-46.5)
Gain (dB)	**16.9**	19.8	14.5	12.3	15.7	23
Gain Ripple (dB)	**±0.5@21.4-41.4**	±1.5@BW_{3dB}	±1.5@BW_{3dB}	±0.3‡@23.6-30.1	±0.8‡@23.6-36.9	±1.05‡@25.6-45.7
NF (dB)	**2.18-3.97 <3dB@21-37.4GHz**	2.17-2.85	2.65-4.62	2.8-4.2	2.79-5.16	2.2-4.0
Average NF Variation (dB/GHz)	**0.066**	0.062	0.129	0.119	0.129	0.079
IP_{1dB} (dBm)	**-21.2∼-14.9**	-13.6∼-8.6	-13.2∼-6.6	-11.0∼-7.0	-20.4∼-14.2	-28∼-23.7‡
IIP3@freq (dBm)	**-13.4∼-8.3**	-4∼-0.6	-3.6∼3.2	-0.2∼3	-10.8∼-4.6†	-18.4∼-14.1†
Core Area (mm^2)	**0.048**	0.27	0.16	0.26	0.089	0.13
P_{DC} (mW)	**13.9**	14.9	18.9	8.5	14	26.8
FoM/$FoM_{Area}$$	**20.7/431.0**	11.1/41.2	5.1/31.9	6.3/24.3	8.2/92.3	18.3/140.8

* Mild electrical decoupling (MED) current-reuse. # Dual-path noise-canceling. † Estimated with IP_{1dB}+9.6dB.

‡ Estimated precisely from the figure using a digitizing tool. $ $FoM = \frac{Gain[lin.]\times Bandwidth[GHz]}{(NF_{\min}[lin.]-1)\times P_{DC}[mW]}$, $FoM_{\text{Area}} = \frac{FoM}{Core\,Area[mm^2]}$

IV. Conclusion

This paper presents an ultra-compact, wideband, low-NF and high-gain-flatness LNA implemented in a 40-nm bulk CMOS process, operating from 19.9 GHz to 47 GHz. By adopting large-size transistor, both low NF and wideband input matching are realized. Furthermore, a transformer-based inter-stage matching network and mild electrical decoupling (MED) current-reuse topology are employed to extend the bandwidth and improve gain flatness. In addition, two wideband high-Q transformers with 8-shaped winding are utilized, which guarantees wideband performance. These analyses and design strategies collectively boost the LNA's performance and yield an outstanding FoM. The results validate the effectiveness of the proposed design for wideband low-noise applications, demonstrating its potential for 5G/6G multi-bands multi-standard communication phased-array systems, especially in multi-channel and large-scale scenarios.

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