A 10b 450MS/s SAR ADC Using Low-Reference-Dependency Switching Strategies achieving 68.13dB SFDR and 14.21fJ/conv-step FoM_W

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***Abstract*—This paper presents a single-channel 450MS/s 10-bit successive approximation register (SAR) analog-to-digital converter (ADC) with a bitwise charge-average switching strategy (BCA-SS) and a double-settling switching strategy (DS-SS). The BCA-SS reduces reference ripple and halves the settling error by connecting the bottom plates of corresponding differential capacitors to perform charge averaging during each bit settling, rather than relying on reference buffer charging or discharging. The DS-SS reduces the CDAC area and eliminates the complex resistive DAC voltage division and selection network in the hybrid RC-DAC by reusing partial capacitors to complete successive approximation quantization, while retaining the benefit of lowered switching energy. To improve the sampling linearity, the bootstrapped switch is optimized by reducing the nonlinear capacitance in the boosting loop. Fabricated in a 28-nm CMOS technology, the ADC occupies 0.0072mm^2 and operates with a 1-V supply. The measurement results show that the ADC achieves a signal-to-noise-and-distortion ratio of 53.17dB and a spurious-free dynamic range of 68.13dB at the Nyquist frequency while consuming 2.38mW, resulting in a Walden figure of merit of 14.21fJ/conv-step.**

Keywords—SAR ADC, ripple suppression, bitwise charge-average, double-settling, CDAC

I. INTRODUCTION

High performance instruments such as oscilloscopes and bit error rate testers demand time-interleaved analog-to-digital converters (ADCs) featuring sampling rates in the tens of GS/s and approximately 10-bit resolution. The successive approximation register (SAR) architecture is a preferred choice for the sub-ADCs due to its compact area, high power efficiency, and superior compatibility with advanced processes. While extensive studies have driven remarkable advancements in SAR ADC sampling rates, power efficiency, and resolution, reference ripple remains a fundamental limitation in high-speed designs, which could become particularly severe in dense time-interleaved arrays [1-3]. The degradation of ADC accuracy and linearity due to reference voltage ripple can be mitigated through settling error cancellation and reference ripple reduction. The settling error cancellation technique typically employs an auxiliary CDAC to generate a compensation voltage, which is then subtracted from the output of the main CDAC by a multi-input comparator [1-2]. However, the introduced auxiliary CDAC not only increases the area and requires complex control logic but also necessitates a multi-input comparator with an elevated noise floor. Reference ripple can be reduced by optimized switching strategies (e.g., Vcm-based strategy, Monotonic strategy and Charge-Average strategy) and hybrid RC-DAC [4-5], which lower the energy drawn from the reference buffer [3]. Nevertheless, these switching strategies inevitably involve charging and discharging between GND and VREF through the reference buffer, thus still consuming substantial power to maintain a low output impedance for fast settling. Meanwhile, the settling speed of the hybrid RC-DAC is limited by the static power dissipation of the RDAC, which could severely compromise the overall energy efficiency at higher speeds.

To address the aforementioned issues, this paper proposes a single-channel 450MS/s 10-bit SAR ADC with a bitwise charge-average switching strategy (BCA-SS) and a double-settling switching strategy (DS-SS) to suppress the reference ripple and reduce the reference buffer power consumption. The BCA-SS settles each bit by connecting the bottom plates of corresponding differential capacitors to perform charge averaging. As a result, it avoids charging and discharging between different references and halves the settling error since half the capacitors per bit are connected to the same reference and couple identical errors that cancel each other out at the differential output. To reduce the CDAC area and eliminate the complex RDAC voltage division and selection network, the DS-SS reuses the lower bits capacitors of the CDAC to complete the successive approximation by adjusting their bottom plate voltages, thus replacing the complex RDAC network with one reference while retaining the low switching energy benefit. Combining BCA-SS and DS-SS not only achieves greater reduction in switching energy but also enables the RDAC to integrate into the reference buffer for power saving. Additionally, an optimized bootstrapped switch is also utilized to improve the sampling linearity by reducing the nonlinear capacitance in the boosting loop.

The remainder of this paper is organized as follows. Section II outlines the overall ADC architecture. Section III provides the proposed switching strategies and key circuit details. The measurement results and performance comparison are presented in Section IV. The conclusion is given in Section V.

II. OVERALL ADC ARCHITECTURE

The SAR ADC architecture is illustrated in Fig. 1(a). It mainly comprises a bitwise charge-average logic and a double-settling logic, and a split 7-bit CDAC with 1-bit redundancy. The bitwise charge-average switching logic and double-settling logic modules, both implemented in basic digital logic, control separately the settling of every bit and the last three bits of the CDAC to execute the respective switching strategies. As shown in Fig. 1(b), the ADC

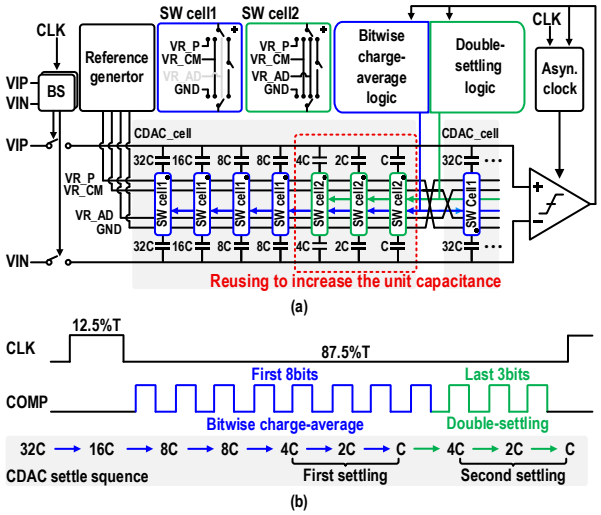

Fig. 1. Overall architecture and timing diagram of the ADC.

operates at 450MS/s, where the sampling phase occupies 12.5% of the cycle with the remainder dedicated to 11 quantization steps. Based on the results of the comparator, the BCA-SS settles the CDAC bit-by-bit through charge-averaging during the first 8 comparisons. The DS-SS then reuses lower bit capacitors of the CDAC to complete successive approximation quantization, thereby increasing the unit capacitance to eight times that of the conventional method without increasing the total capacitance. By synergizing the reference ripple suppression and halved settling error from BCA-SS with the structural simplification and enlarged unit capacitance from DS-SS, the strategies enable a high-accuracy ADC with better trade-off between CDAC area, linearity, and settling speed. All four required references (VR_P, VR_CM, VR_N, VR_AD) are generated simultaneously by a single low-power on-chip source follower circuit by virtue of the effective suppression of reference ripple.

III. Circuit Blocks

A. Bitwise Charge-Average Switching Strategy

Fig. 2 illustrates the implementation of the BCA-SS with a 7-bit split-CDAC, where the voltage difference between VR_P and GND is set equal to the differential peak-to-peak input value. As shown in Fig. 2(a), the CDAC is partitioned into four segments (i.e., PL, PR, NL, NR) with identical total capacitance. During the sampling phase, the ADC samples the inputs and resets the CDAC by connecting the bottom plates of the PL and NR arrays to VR_P and those of the PR and NL arrays to GND. The comparator then performs the first comparison. In the case of VIP > VIN [see Fig. 2(b)], the BCA-SS executes a two-phase operation on the MSB capacitor (i.e., 32C) in the PL and NL arrays. During the averaging phase, it disconnects their bottom plates from VR_P and GND and then interconnects them through low-resistance switches to perform charge averaging. In the subsequent connecting phase, after a brief period, these bottom plates are collectively connected to VR_CM to eliminate plate voltage differences caused by the capacitor mismatch. The same operation is performed on the MSB capacitor in the PR and NR arrays if VIP < VIN. The

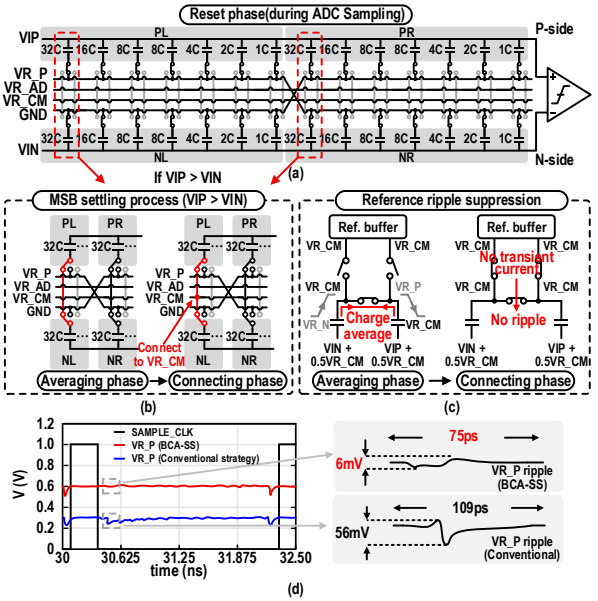

Fig. 2. Detailed implementation of the BCA-SS. (a) Reset phase. (b) MSB settling process when VIP > VIN. (c) Reference ripple suppression principle. (d) VR_P ripple simulation results during MSB settling.

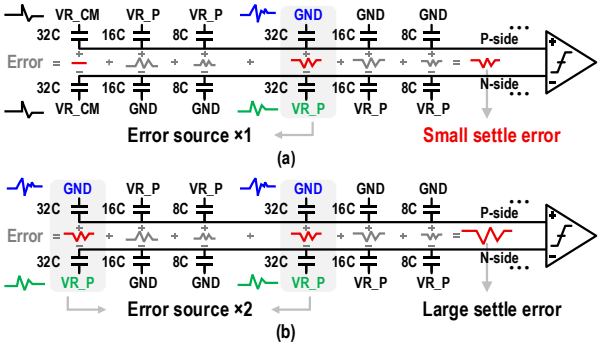

Fig. 3. Settling error halving principle and comparison between (a) the BCA-SS and (b) the conventional strategy.

remaining bits are settled using the same procedure. Fig. 2(c) illustrates the principle of reference ripple suppression by the BCA-SS. By settling the bottom plate voltage at VR_CM after charge averaging between differential capacitances, the BCA-SS avoids the large transient currents induced by capacitors charging or discharging when connected to the reference buffer, thereby effectively reducing the reference ripple amplitude. The simulation results in Fig. 2(d) demonstrate this suppression effect. During MSB settling, the BCA-SS achieves a VR_P ripple of only 6mV and a settling time of 75ps, while the conventional strategy exhibits a ripple of 56mV and requires 109ps to settle.

In addition to reducing the reference ripple amplitude, the BCA-SS can also halve the settling error caused by the ripple. As shown in Fig. 3(a), during MSB settling, the BCA-SS connects half of the 32C capacitors on the differential sides to VR_CM. This connection ensures that any ripple originating from VR_CM affects both differential sides equally, thereby achieving cancellation at the differential terminals. Consequently, the BCA-SS halves the settling error, as only half of the 32C capacitors couple the reference

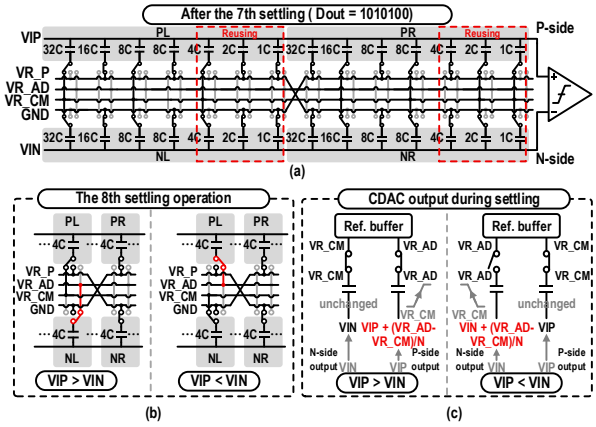

Fig. 4. Working principle of the DS-SS. (a) CDAC connection status after the 7th settling. (b) Detailed settling operation. (c) CDAC output during settling.

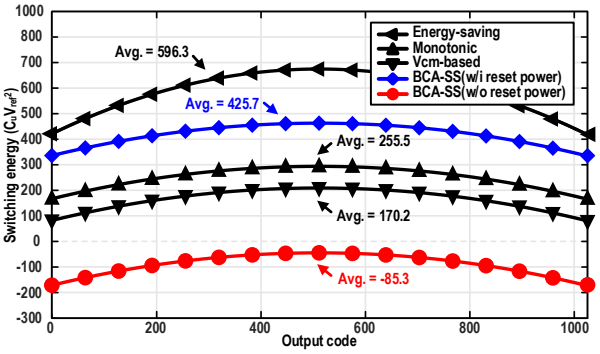

Fig. 5. Comparison of the switching energy of the BCA-SS with that of other switching strategies versus the output code for a given CDAC value.

ripple to the CDAC output. In contrast, the conventional strategy [see Fig. 3(b)] connects all P-side 32C capacitors to GND and N-side 32C capacitors to VR_P, directly coupling reference ripple to the output through all four 32C capacitors and worsening settling error. By simultaneously suppressing reference ripple amplitude and halving settling error, the BCA-SS improves both CDAC settling precision and speed while also easing the reference buffer requirements.

B. *Double-Settling Switching Strategy*

Fig. 4 illustrates the working principle of the DS-SS, which reuses the 4C, 2C, and C capacitors of the CDAC to generate quantization voltages for the final 3 bits. Specifically, after the CDAC completes the 7th settling, the plates of these capacitors are already connected to the corresponding references. The DS-SS then successively switches the bottom plate of these capacitors from VR_CM to VR_AD on the N-side or P-side based on the comparison result [see Fig. 4(b) and (c)]. This strategy requires only one reference by operating on a single CDAC side during each bit settling, removing the need for the complex reference selection network and seven additional references used in hybrid RC-DAC. Additionally, by reusing part of the CDAC, the DS-SS allows the CDAC to use larger unit capacitors, which directly match the process-limited minimum dimensions, thus avoiding the excessive area overhead of paralleling larger capacitors to achieve a small unit capacitor.

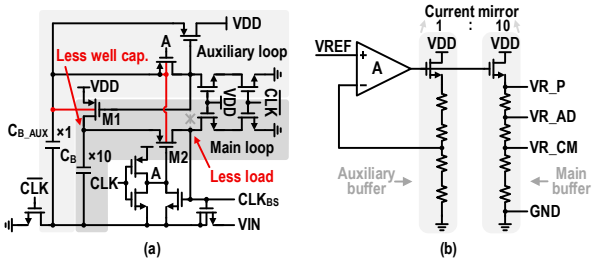

Fig. 6. (a) Schematic of the improved bootstrapped switch. (b) Schematic of the reference buffer.

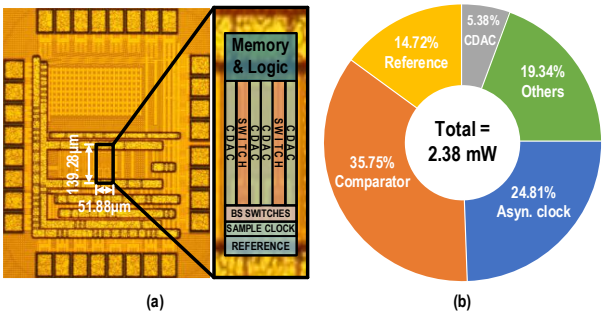

Fig. 7. (a) Die micrograph. (b) Power breakdown.

Fig. 5 compares the switching energy of the BCA-SS with that of other switching strategies versus the output code for a given CDAC value. It can be seen that although the overall energy consumption of this switching strategy is relatively large, it does not draw energy from the reference buffer during conversion. The reason is that the DAC pre-stores a large amount of energy during reset, and achieves voltage settling by gradually discharging this stored energy. This behavior results in a small energy variation, demonstrating that the proposed strategy generates less reference ripple. Since the longer sampling phase affords ample time for the reference buffer to fully reset the CDAC, the ADC is enabled to utilize a low-power reference buffer, thereby achieving substantial power savings while maintaining satisfactory settling accuracy.

C. *Imporved Booststrapped Switch and Reference Buffer*

Fig. 6(a) illustrates the improved bootstrapped switch circuit. It splits the conventional bootstrapped loop into a larger main loop and a smaller auxiliary loop, with a size ratio of 10:1 between them. The bulk of M1 and M2 and the gate of M1 in the main loop are driven by the auxiliary loop, thus reducing the effect of the well capacitances and load capacitances on the main loop to improve linearity. Simulation results show that the optimized bootstrapped switch achieves a 4 dB improvement in linearity compared to its conventional counterpart. Fig. 6(b) depicts the circuit implementation of the reference buffer, where a simple source follower is adopted since the BCA-SS effectively eases the buffer requirements. The RDAC is densely integrated into the buffer to generate multiple references by appropriately setting the resistance ratios of the serial resistor.

IV. Measurement Results

The SAR ADC prototype was fabricated in a 28-nm CMOS process. Fig. 7 shows the die photograph and power breakdown. It occupies an area of 0.0072mm² and consumes 2.38mW of total power, with the on-chip reference buffer

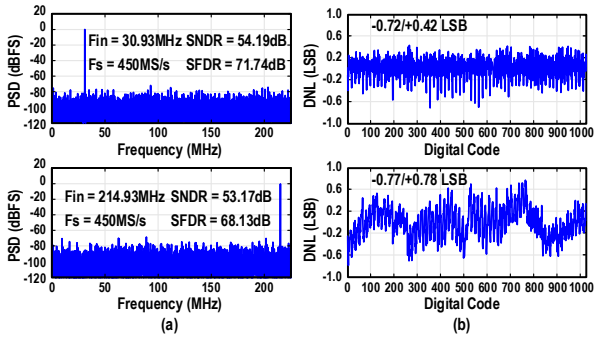

Fig. 8. Measurement results. (a) Output spectra. (b) DNL and INL.

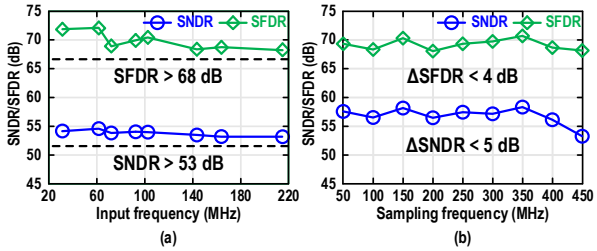

Fig. 9. (a) SNDR/SFDR versus input frequency at a sampling rate of 450 MS/s. (b) SNDR/SFDR versus sampling frequency at an input frequency of 214.93MHz.

contributing only 0.35mW. Fig. 8(a) shows the measured 65536-point power spectral density with a sampling rate of 450MS/s. The ADC exhibits a signal-to-noise ratio (SNDR) of 54.19dB and a spurious-free dynamic range (SFDR) of 71.74dB at a 30.93MHz input. When the input frequency increases around the Nyquist frequency, the SNDR and SFDR are 53.17dB and 68.13dB, respectively. Fig. 8(b) displays the static differential non-linearity (DNL) and integral non-linearity (INL), which separately achieve −0.72/+0.42LSB and −0.77/+0.78LSB. Fig. 9(a) and (b) present the measured SFDR and SNDR across various input frequencies and sampling frequencies. When input frequency changes from 20 to 220MHz at 450MS/s, the SNDR and SFDR always remain above 53dB and 68dB. Over a sampling frequency range of 50 to 450MS/s with a 214.93MHz input, the SNDR and SFDR degrade less than 5dB and 4dB, correspondingly. This can be mainly attributed to the developed switching strategies and optimized bootstrapped switch. Based on the measured SNDR, SFDR, and power consumption near the Nyquist frequency, the Walden figure of merit (FoM_W) and the Schreier FoM (FoM_S) can be calculated as 14.21fJ/conv-step and 162.93dB. Table I summarizes the performance of the fabricated prototype with a comparison to similar designs. The designed ADC demonstrates better performance in FoM_S, FoM_W, and SFDR compared to other designs.

V. Conlusion

A 450MS/s 10-bit SAR ADC with both BCA-SS and DS-SS is developed. It aims to lower the reference ripples, thus improving the linearity and power efficiency of the overall ADC. The BCA-SS achieves reference ripple suppression and halves the settling error by settling each bit through charge averaging rather than charging or discharging through the reference buffer. The DS-SS retains the lower switching energy advantage of hybrid RC-DAC and eliminates the need for a complex RDAC by reusing partial capacitors for settling. Fabricated in a 28-nm CMOS process, the designed SAR ADC is measured to achieve an SNDR of 53.17dB, an SFDR of 68.13dB, and a FoM_W of 14.21fJ/conv-step.

TABLE. I. Performance Comparison With The State-Of-The-Art ADCs

	This Work	VLSI 2025[6]	ISSCC 2021[7]	JSSC 2020[8]	VLSI 2020[9]	CICC 2017[10]
Architecture	SAR	SAR	Pipe-SAR & DSM	2-3 b/c SAR	SAR & FLASH	2 b/c SAR
Technology (nm)	28	65	7	40	28	40
Active area (mm^2)	0.0072	0.0300	0.0370	0.0140	0.0056	0.0080
Resolution (bit)	10	8	12	7	8	10
Sample rate (MS/s)	450	100	600	900	1000	300
Reference buffer power (mW)	**0.35**	NA	NA	0.38	NA	0.40
Total power (mW)	2.380	0.599	13.000	2.600	2.550	2.100
SNDR@Nyq. (dB)	53.17	48.70	55.30	39.70	45.50	47.00
SFDR@Nyq. (dB)	**68.13**	65.60	67.80	54.80	59.40	63.00
FoM_S (dB)	**162.93**	157.92	158.93	152.08	158.42	155.54
FoM_W (fJ/conv-step)	**14.21**	26.93	45.55	36.61	16.57	38.27

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