A 2MHz 48V/10A Dual 3-Level Bridge Hybrid Buck-Boost Converter with Complete Soft-Charging and Responsive Loop-Free V_{CF} Balancing

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***Abstract*—To fully leverage the potential of the hybrid structure in buck-boost system, this work presents a dual 3-level bridge hybrid buck-boost converter (D3B-HBBC), achieving complete soft-charging to significantly enhance the power rating capability. A responsive loop-free balancing (RLB) scheme is developed to swiftly stabilize the flying capacitors (C_F) without any additional regulation loops. Moreover, a phase-shifted control is realized to enable seamless mode transition while effectively reducing the inductor current ripple. Fabricated in a 180nm BCD process, the 2MHz GaN-based D3B-HBBC with a 48V output delivers a maximum power of 480W, attaining a peak efficiency of 97.1% with 6×0.47μF C_F. This design improves the power rating by 3.3 times while reducing C_F by over 28.4 times.**

***Index Terms*—hybrid buck-boost converter, complete soft-charging, responsive loop-free V_{CF} balancing.**

I. Introduction

To efficiently meet the high-power demands, data center racks commonly use the 48V power delivery architecture. As shown in Fig. 1 (top), a battery backup unit provides continuous current when the main power supply fails. This makes the buck-boost converter (BBC) essential for handling the battery pack's voltage range of 36V to 60V. The widely used non-inverting BBC (NIBBC) [1, 2] suffers from low efficiency, requires dedicated mode control and needs a large inductor for high power delivery. In contrast, hybrid BBC (HBBC), which incorporates the favorable utilization of active device of switch-capacitor (SC) network and high energy density of the flying capacitor (C_F), can improve efficiency and ensure smooth mode transition while reducing the sizes of the passive components. However, the foundation of these advantages is soft-charging [3], which is still challenging in HBBC. As shown in Fig. 1 (bottom), the existing HBBCs generally employ a hard-charging phase (Φ_{HC}) after a soft-charging one (Φ_{SC}) for power delivery [4-8]. In Φ_{HC}, C_F is connected in parallel with a fixed voltage (e.g. the input V_{IN}, output V_O, or $V_O - V_{IN}$). Such an operation inevitably incurs charge sharing loss (P_{CS}), which increases with the load current I_O following a square-law. As a result, in order to sustain a high efficiency for high-power delivery, C_F must be sufficiently large [4]. Such a strong correlation between C_F and I_O significantly constrains the power delivery capacity of the conventional HBBCs. In addition, C_F imbalance in a hybrid structure remains a persistent issue when performing complete soft-charging. Closed-loop control can balance V_{CF}

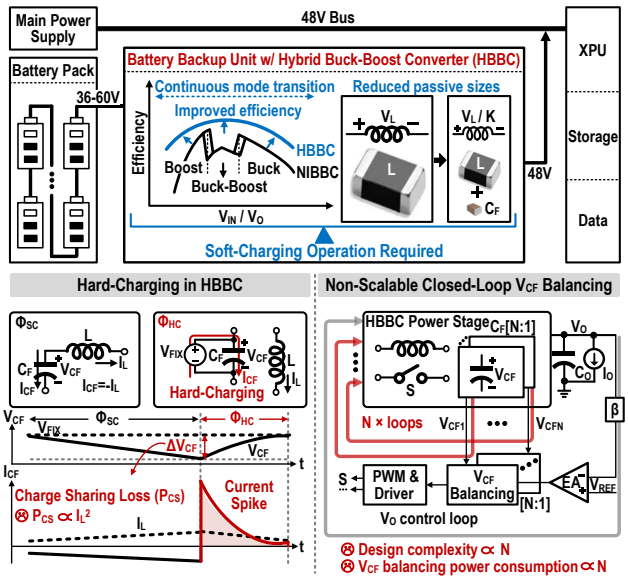

Fig. 1. Main challenges on designing hybrid buck-boost converter (HBBC) for high power delivery.

actively, suitable for the hybrid topology with a single C_F [9]. However, due to the increased design complexity and power consumption, it becomes impractical in HBBCs, which generally incorporate multiple C_Fs to implement both the step-up and step-down functionalities.

II. Proposed Dual 3-Level Bridge HBBC

This work proposes a dual 3-level bridge HBBC (D3B-HBBC) to fully utilize the potential of the hybrid architecture in buck-boost conversion. As shown in Fig. 2, compared to the bilaterally-symmetrical HBBC using step-up SC networks [5], the D3B-HBBC cascades two identical 3-level bridges with a central inductor (L). By charging and discharging the flying capacitors (C_{FL} and C_{FR}) always through the inductor current (I_L), D3B-HBBC eliminates the hard-charging phases, successfully achieving complete soft-charging. As the benefit, D3B-HBBC significantly reduces the total sizes of C_{FL} and C_{FR} for the same power rating, or equivalently improves the load capability with the same C_{FL} and C_{FR}. Furthermore, the voltage fluctuations at the switching nodes, V_{SW1} and V_{SW2},

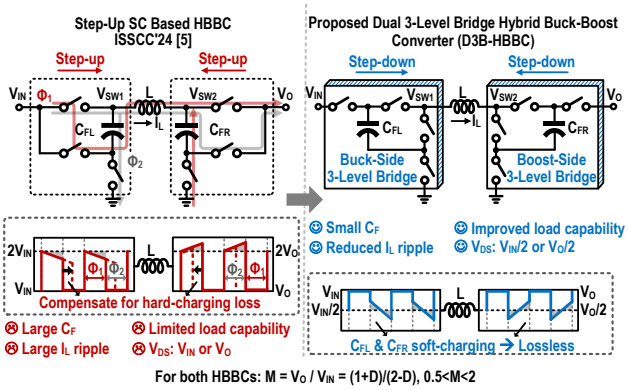

Fig. 2. Proposed dual 3-level bridge hybrid buck-boost converter (D3B-HBBC) in comparison with the conventional step-up SC based HBBC.

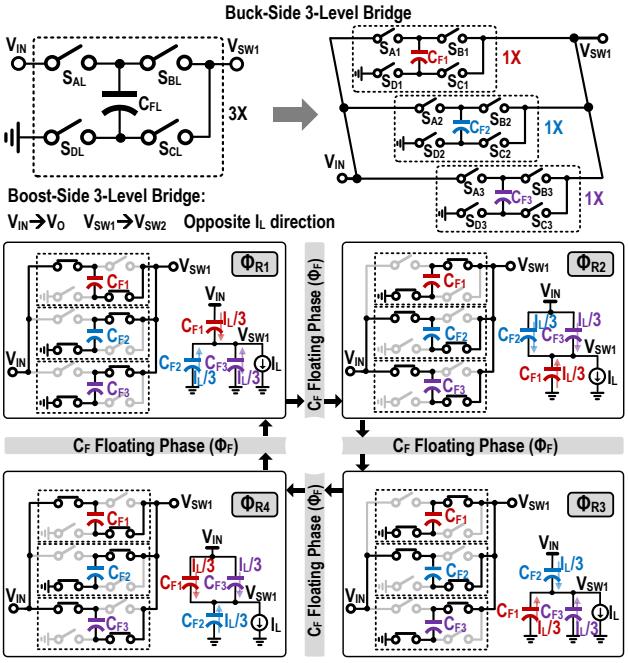

Fig. 3. Proposed responsive loop-free balancing (RLB) scheme and the phases to stabilize the flying capacitors in 3-level bridge.

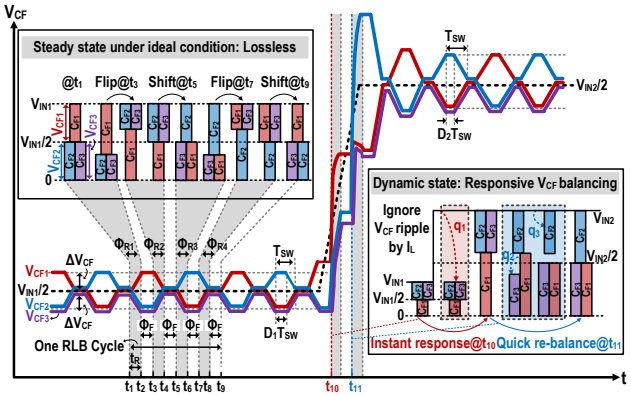

Fig. 4. Operating principle of the proposed responsive loop-free balancing (RLB) scheme at steady state and dynamic response.

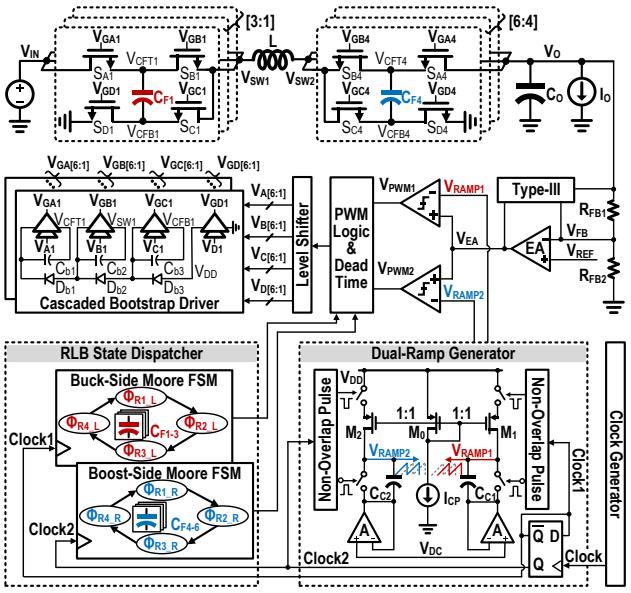

Fig. 5. System diagram of the designed dual 3-level bridge hybrid buck-boost converter (D3B-HBBC).

are halved thanks to the step-down operations of the 3-level bridges. Thus, the inductance is suppressed considerably to maintain the same I_L ripple. Meanwhile, the voltage stresses (V_{DS}) of the power devices are compressed sufficiently, improving the conversion efficiency. It has been observed that D3B-HBBC exhibits all the aforementioned features with the same voltage conversion ratio M=(1+D)/(2−D) as that in [5], while maintaining a symmetrical structure.

However, it is not straightforward to implement the D3B-HBBC in practice, given the persistent V_{CF} imbalance issue in 3-level stage. To avoid introducing any additional V_{CF} regulation loops as in multi-level NIBBC [10], a responsive loop-free balancing (RLB) scheme is devised in this work. As depicted in Fig. 3, based on the buck-side bridge, the 3-level stage is split into three identical branches, with the same total capacitor and power switch sizes. The resultant capacitors, C_{F1}, C_{F2} and C_{F3}, are reconfigured in four phases, Φ_{R1}, Φ_{R2}, Φ_{R3} and Φ_{R4}, with a floating phase, Φ_F, between each pair, during which $S_{A1\text{-}3}$ and $S_{B1\text{-}3}$ are turned on. The RLB principle is detailed in Fig. 4. Ideally, Φ_{R1}, Φ_{R2}, Φ_{R3} and Φ_{R4} all have the same period (t_R) at steady state. At the start of Φ_{R1} (t_1), C_{F1} is in series with the parallel combination of C_{F2} and C_{F3}, connected between V_{IN} and ground. In Φ_{R1} from t_1 to t_2, C_{F1} charges while C_{F2} and C_{F3} discharge, causing a voltage variation ΔV_{CF} from $V_{IN}/2$. At t_3, the tri-C_F network flips to initiate Φ_{R2}, discharging C_{F1} and charging C_{F2} and C_{F3} until t_4. Then all three capacitors reach equilibrium again. At t_5 after a Φ_F, C_{F3} is reconfigured in parallel with C_{F1}, and no charge redistribution occurs because V_{CF1}=V_{CF3}. Similar process repeats in Φ_{R3} and Φ_{R4} from t_5 to t_8, maintaining balance

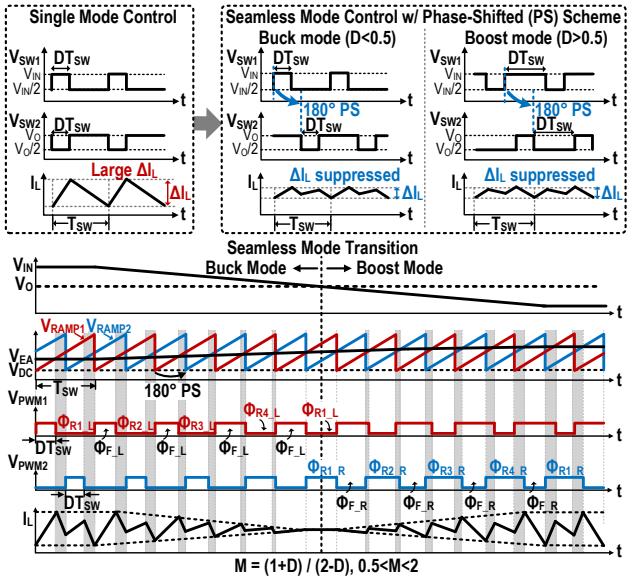

Fig. 6. Phase-shifted control for D3B-HBBC achieving seamless mode transition and suppressing inductor current ripple.

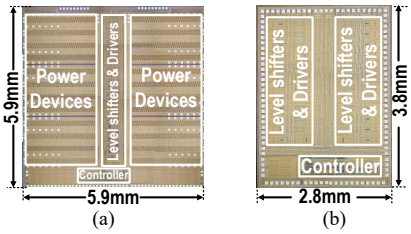

Fig. 7. Die photoes: (a) monolithic chip integrating LDMOS transistors as power switches and (b) controller chip to drive external GaN power devices.

on C_{F1}, C_{F2} and C_{F3}. At t_9, a new RLB cycle begins. As can be seen from the above, the RLB scheme eliminates charge-sharing loss. This is a fundamental difference from the series-parallel operation, which involves paralleling two capacitors with different voltages and thus incurs hard-charging [11]. In practice, phase mismatch may cause a time variance, e.g. Δt between Φ_{R1} and Φ_{R2}. Thus, V_{CF3} differs from V_{CF1} when C_{F3} shifts in parallel with C_{F1} at t_5. However, charge redistribution between C_{F1} and C_{F3} help balance their voltages quickly, while the voltage difference between V_{IN} and the tri-C_F network is corrected by charge injection or absorption from V_{IN}. Thus, the slight imbalance due to phase mismatch is removed with negligible power loss, avoiding long-term V_{CF} drifting. When V_{IN} rises from V_{IN1} to V_{IN2} at t_{10}, higher V_{IN2} instantly injects charge into the network, raising V_{CF1}, V_{CF2} and V_{CF3} towards the new balance state of $V_{IN2}/2$. As C_{F3} shifts to parallel with C_{F1} at t_{11}, it redistributes charge again, driving $C_{F1\text{-}3}$ towards new balance within a few RLB cycles.

Fig. 5 shows the D3B-HBBC system with all N-type power switches $S_{A\text{-}D[1:6]}$ and six flying capacitors $C_{F1\text{-}6}$, driven by cascaded bootstrap gate drivers. The output (V_O) feedback loop uses a type-III compensator and a dual-ramp generator

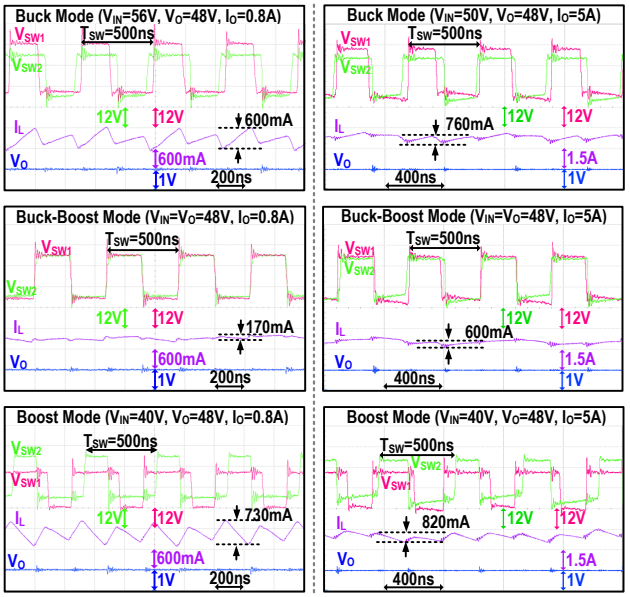

Fig. 8. Measured switching waveforms of D3B-HBBC with (a) integrated LDMOS power transistors and (b) external GaN power transistors.

to regulate V_O, and an RLB state dispatcher with two Moore finite state machines (FSMs) to balance $C_{F1\text{-}6}$. As shown in Fig. 6, with continuous M, D3B-HBBC can switch in a single mode, but this causes large I_L ripple (ΔI_L). To reduce ΔI_L, phase-shifted control is designed to respectively split the energizing and deenergizing phases of L into two sub-intervals with lower voltages across L. This is implemented by comparing the out-of-phase ramp signals ($V_{RAMP1,\,2}$) to the output of the error amplifier V_{EA}, achieving seamless mode transition. The periods of V_{SW1}=V_{IN}/2 and V_{SW2}=V_O/2 are implemented in turn by the four RLB phases.

III. Measurement Results

As shown in Fig. 7, two prototype chips were fabricated in a 180nm BCD process. The first chip is a monolithic D3B-HBBC integrating LDMOS transistors as the power switches, occupying an area of 5.9mm×5.9mm. The second one is a D3B-HBBC controller with an area of 2.8mm×3.8mm to drive external GaN power devices. Fig. 8 shows the measured switching waveforms of the two systems under buck, buck-boost and boost modes. With an input range from 36V to 60V, both the systems can operate at 2MHz. As demonstrated in Fig. 9, the GaN-based D3B-HBBC is able to deliver a maximum power of 480W using the total flying capacitances of 6×0.47μF, improving the power rating by 3.3 times and reducing the required C_F by over 28.4 times compared to the previous works. Based on the measurements in Fig. 10, the monolithic D3B-HBBC achieves a peak efficiency of 93.5% with >85% efficiency over 88.8% of I_O range from 0.1A to 1A. The GaN-based D3B-HBBC attains a peak efficiency of 97.1% with >84% efficiency over the entire power range from

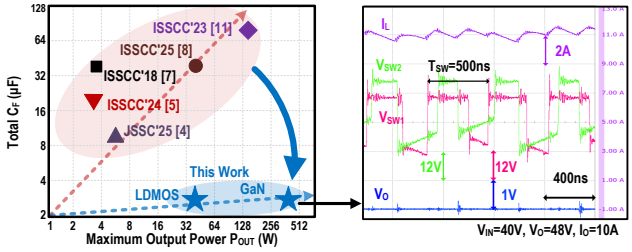

Fig. 9. Output power comparison with the prior works

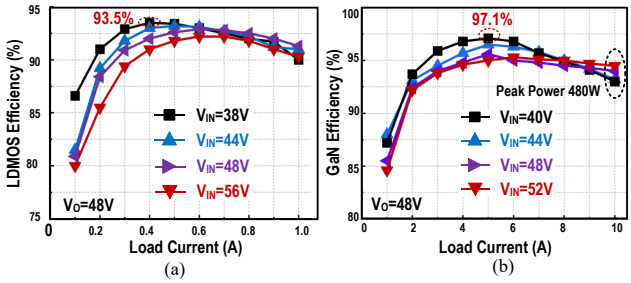

Fig. 10. Efficiency plots of proposed D3B-HBBC with (a) integrated LDMOS transistors as the power switches and (b) external GaN power transistors.

48W to 480W. Fig. 11 shows the seamless mode transitions as V_{IN} changes between 40V and 56V at 1V/ms, maintaining stable V_O and balanced V_{CF}. In start-up test, V_{IN} rises from 0 to 48V in 5ms, showing well-built V_O and balanced V_{CF}. Table I compares the proposed D3B-HBBC with the state-of-the-art buck-boost converters. Compared to the GaN-based NIBBC in [2], the GaN-based D3B-HBBC improves the power delivery by 16.8 times with superior power efficiencies. Compared to the fully-integrated counterparts in [5, 6], the monolithic D3B-HBBC enhances the power rating by more than 5 times, while reducing C_F by nearly 10 times. Although the work in [11] can output 3 times higher power, it requires 6.6 times (C_O+C_F) with generally lower efficiencies, particular in the boost mode.

IV. Conclusion

This work constructs a dual 3-level bridge hybrid buck-boost converter, achieving complete soft-charging and hence significantly enhancing the power delivery capability. A loop-free flying capacitor (C_F) balancing strategy is devised to responsively stabilize C_F, without increasing chip area. Further, a phase-shifted control accomplishes seamless mode transition.

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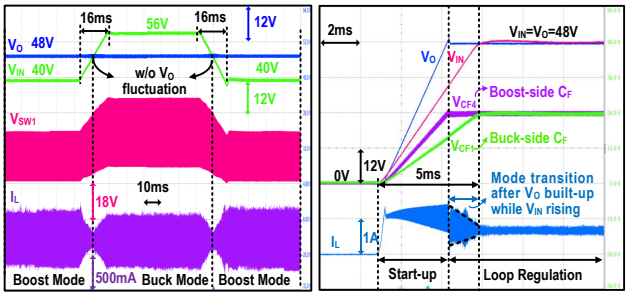

Fig. 11. (a) Seamless mode transition and (b) start-up process.

TABLE I
Performance Comparison with State-of-the-Arts.

Work		VLSI'24 [6]	ISSCC'24 [5]	ISSCC'23 [11]	ISSCC'21 [2]	This Work LDMOS-Based	This Work GaN-Based
Process		180nm CMOS	180nm CMOS	150nm BCD	350nm BCD	180nm BCD	
Power Stage	Power Transistor	Si MOSFET	Si MOSFET	Si MOSFET	100V GaN	Si MOSFET	40V GaN
	Topology	SDC-BBC	BSHBBC	SHBBC	NIBBC	D3B-HBBC	
Input Voltage [V]		2.5-4.5	2.7-4.2	5-48	4-60	36-60	
Output Voltage [V]		3-6	3.4	5-48	0-100	48	
Switching Freq. [MHz]		2	1	2	2	2	
Max. I_O [A]		1	1	3	1.5	1	10
Inductor [μH]		4.7	4.7	0.47	NR	2.2	
C_O [μF]		10	10	4.7	NR	10	22
C_F [μF]		10	10×2	10×8	NA	0.47×6	0.47×6
Peak Output Power [W]		6	3.4	144 / 27.1***	28.5	48	480
Max. V_{DS} of Switch		V_{IN}	V_{IN} or V_O	V_{IN}/3 or V_O/3	V_{IN} or V_O	V_{IN}/2 or V_O/2	
Peak Eff.(%)	Buck Mode	96.2	96.3*	89**	89.6	92.9	95.3
	Buck-Boost	NR	96.9	NR	85*	92.2	95.6
	Boost Mode	96.4	96.5*	86**	92	93.5	97.1
Mode Transition		Seamless	Single Mode	Required	Required	Seamless	
Complete Soft-Charging		No	No	No	NA	Yes	

*Estimated value according to paper **Estimated eff. when V_{IN} (V_O)=48V at buck (boost) mode according to paper
*** Peak output power under buck mode / Peak output power under boost mode

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