Novel Back-Gate Thermometry Technique for Self-Heating Analysis in FD-SOI Devices down to 4 K

M. Vanbrabant[#1], V. Dieuzeide[#], M. Rack[#], A. Grill*, A. Caglar*, S. Balamurali*, J.-P. Raskin[#], V. Kilchytska[#]
[#]Université catholique de Louvain, Louvain-la-Neuve, Belgium
*imec, Leuven, Belgium
[1]martin.vanbrabant@uclouvain.be

***Abstract*—This work proposes a novel technique for the mapping of temperature rise in advanced fully depleted silicon-on-insulator (FD-SOI) MOSFETs taking advantage of the presence of the transistor back-gate. For the first time to the author's best knowledge, the back-gate resistance is used as a thermometer to sense the local temperature caused by self-heating effect. This technique is demonstrated to be very sensitive, particularly at cryogenic temperatures, thanks to the strong back-gate resistance temperature dependence at cryogenic temperatures (contrarily to the gate resistance which tends to saturate in this temperature range). Therefore, this technique is very promising as a complementary self-heating characterization technique which provides (i) reliable extraction in the temperature range where standard gate thermometry loses sensitivity and (ii) additional information on the temperature under the buried oxide (BOX), and thus vertical heat distribution. Thermal coupling measurements between adjacent transistors down to 4 K provide complementary information on the lateral heat propagation. Those two approaches for extraction/mapping of temperature rise in FD-SOI structures are complementary and allow for more accurate thermal modeling.**

***Keywords*—Characterization, Cryogenic Temperatures, FD-SOI MOSFET, Self-Heating, Thermometry, Thermal Coupling**

I. Introduction

Quantum computers represent a promising technology for solving problems beyond the capabilities of classical computers in key applications such as factorization [1], database searches [2], chemistry [3] or medicine [4]. To achieve fault-tolerant quantum computation with error correction code, millions of qubits will need to be integrated to achieve practical quantum advantage [5]. One of the candidate platforms for developing quantum computers is based on silicon spin qubits, where the robust nano-scale manufacturing process and advanced large-scale integration capabilities of the semiconductor industry can be leveraged. Classical control electronics, placed in the close vicinity of qubits to reduce the number of DC/RF control lines, however, present a challenge as their operation can lead to self-heating, resulting in increased on-chip temperature which can alter the qubit state. It is thus crucial to evaluate this phenomenon down to cryogenic temperatures where the power dissipation should be limited. A large variety of on-chip temperature-sensing techniques, such as gate thermometry [6], diode thermometry [7], quantum dot and superconducting phase transition thermometry [8] and RF technique [9], [10], have been developed and applied down to cryogenic temperatures.

In this work, self-heating in fully depleted silicon-on-insulator (FD-SOI) transistors down to cryogenic temperatures is assessed through (i) a novel technique which uses the back-gate not as threshold voltage tuning knob but as local thermometer and (ii) the thermal coupling between adjacent devices. As thermal effects are strongly layout dependent and material thermal conductivities vary with temperature [11], large characterization efforts and complimentary temperature-sensing techniques are required in order to develop accurate and scalable electro-thermal models, integrated in the future cryogenic process design kit (PDK).

II. Experimental Setup and Devices Description

The devices under study are fabricated in a commercial advanced FD-SOI CMOS technology. The structure consists of two multi-fingers low threshold voltage nFETs, both having their respective n-doped well (Nwell), placed side-by-side at 2.74 µm from each other (center-to-center distance) as represented in Fig. 1. Both devices feature a gate length below 30 nm and a total width of 50 µm.

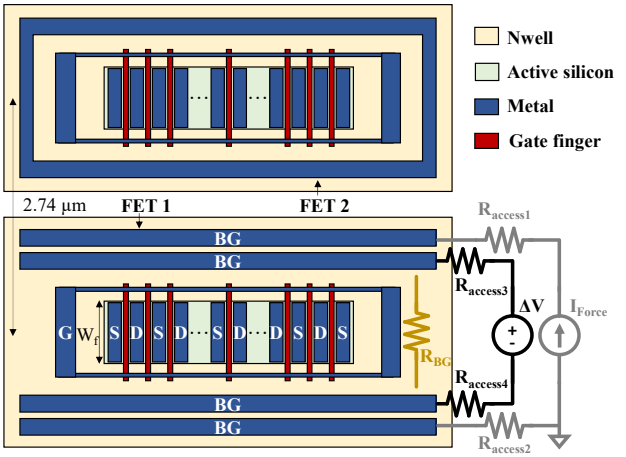

Fig. 1. Schematic (not to scale) of two multi-fingers FD-SOI nFETs with a gate center-to-center distance of 2.74 µm. Additional back-gate contacts are present on FET 1 to perform back-gate resistance thermometry.

FET 1 has an original specific design allowing for back-gate thermometry. The back-gate contacts of FET 1 are designed by using the top-bottom option from the standard cell with two additional contacts placed manually in order to perform 4-point resistance measurements. FET 2 uses the default back-gate ring option. Measurements were performed down to 4 K using a LakeShore CRX cryogenic probe station with a Keysight B1500A semiconductor analyzer and B2902A SMU for DC characterization.

Fig 2 shows I_{DS}-V_{GS} characteristics of FET 1 in the linear regime (V_{DS} = 50 mV) at 300 K and 4 K, highlighting a threshold voltage, V_{TH}, increase of 0.12 V at 4 K with respect to its room-temperature value (V_{TH} = 0.27 V). The V_{TH} tunability with the back-gate voltage (V_{BG}) remains functional at 4 K, with a V_{TH} tunability of 78 mV/V similar to the 84 mV/V value obtained at 300 K. The same values are obtained for FET 2, proving that our specific design does

not alter V_{BG} tunability. In the following study, all currents and voltages referring to FET 2 are explicitly mentioned with a "2" (e.g. V_{GS2}) and V_{BG} always equal to 0 V except during back-gate thermometry.

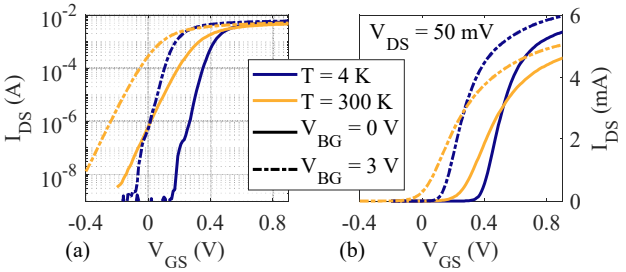

Fig. 2. I_{DS}-V_{GS} characteristics of FET 1 in the linear regime (V_{DS} = 50 mV) at 4 K and 300 K for two different back-gate voltages (0 V and 3 V) in (a) logarithmic and (b) linear scales.

III. Back-Gate Thermometry

As in most electrical-based temperature extraction methods [8], a temperature calibration is required in order to estimate a local temperature increase ΔT. In this case, the metric of interest, namely the back-gate resistance R_{BG} (see Fig. 1), is first measured at various ambient temperatures down to 4 K, while the device is biased under "cold conditions" (i.e. no self-heating). These first measurements $R_{BG}(T)$ serve as a temperature reference (calibration curve). The same metric (R_{BG}) is then measured again but this time when the device is biased under usual operating conditions (i.e. generating heat). By comparing these new R_{BG} values to the reference curve, the local temperature increase is estimated.

A. Back-Gate Resistance Temperature Dependence

In order to estimate the back-gate resistance of the device, a small current I_{Force} is forced into the two outer BG contacts and the voltage difference ΔV is measured in between the two BG inner contacts as shown in Fig. 1. Since no current is flowing through the two inner BG contacts, these 4-point measurements enable the accurate estimation of R_{BG} without the contribution of access resistances ($R_{access1}$ and $R_{access2}$). Fig. 3 shows the ΔV-I_{Force} characteristics when FET 1 is biased at V_{GS} = 0 V and V_{DS} = 0.9 V and at different temperatures. Except for measurements at 4 K and 10 K, a linear relationship between ΔV and I_{Force} is observed due to the resistive behavior of the well. The non-linearities at 4 K and 10 K are attributed to a Schottky contact between the metal via and the n+ silicon region present at these temperatures but it will not critically impact the extraction procedure as the purpose is to have reference curves at each temperature.

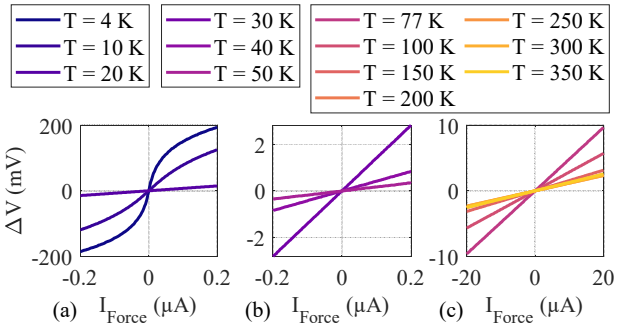

Fig. 3. ΔV-I_{Force} characteristics of FET 1 (V_{GS} = 0 V and V_{DS} = 0.9 V) in various temperature ranges: (a) 4-20 K, (b) 30-50 K and (c) 77-350 K.

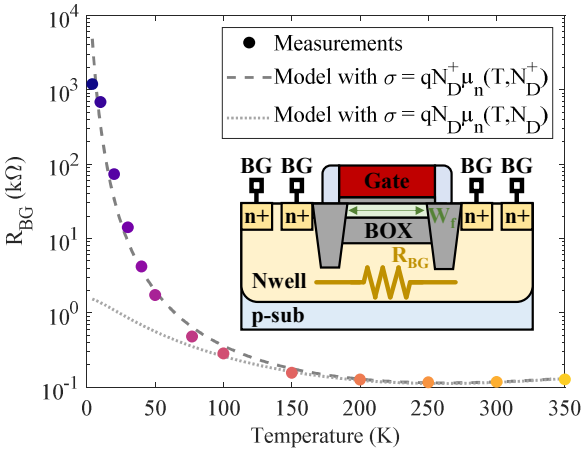

Fig. 4. R_{BG} vs temperature of FET 1 (V_{GS} = 0 V and V_{DS} = 0.9 V). Schematic cross-section of an FD-SOI SLVT transistor (inset).

From Fig. 3, R_{BG} is computed as the slope of ΔV-I_{Force} using a linear regression at each temperature and the results are plotted in Fig. 4. An increase of R_{BG} by 4 orders of magnitude is observed when temperature is reduced from 300 K to 4 K. This strong sensitivity of R_{BG} to temperature, particularly below 150 K, is one of the advantages of this technique over other techniques such as gate thermometry where the front-gate resistance tends to saturate at cryogenic temperatures [6] and thus loses the precision.

B. Back-Gate Resistance Modeling

To model this sharp transition, the Nwell resistance can be expressed as $R_{BG}' = 1/\sigma$, where the conductivity σ is equal to $qn\mu_n$, with q the elementary charge, n the electron density and μ_n the electron mobility. The hole density p contribution is neglected in the expression of R_{BG}' as they are minority carriers. As shown in Fig. 5a, the analytical expression of μ_n, based on Caughey-Thomas model [12], [13], is dependent on both temperature and the ionized impurity concentration. Figs. 5b and 5c then show the band diagrams obtained from the 0D solution of the charge neutrality equation (1) at 300 K and 50 K, respectively. The ionized donor density N_D^+ is defined in (2) where $g_D(E)$ is the donor energy distribution (3) and $F(E)$ is the Fermi-Dirac distribution (4). In this study, $g_D(E)$ follows a Gaussian distribution with an energy of E_D = 45 meV from the conduction band E_C (corresponding to the energy of phosphorus) and a characteristic width of the Gaussian distribution of W_{GD} = 0.01 eV. The N_{GD} parameter is chosen in order to have the integral of $g_D(E)$ over energy equals to 10^{17} cm^{-3}, where a uniform well doping profile is assumed for the model (the real doping profile being not constant along the silicon thickness).

$$n = p + N_D^+ \tag{1}$$

$$N_D^+ = \int_{E_V}^{E_C} g_D(E)(1 - F(E)dE \tag{2}$$

$$g_D(E) = N_{GD} \exp\left(-\left(\frac{E_C - E_D - E}{W_{GD}}\right)^2\right) \tag{3}$$

$$F(E) = \frac{1}{1 + \exp\left(\frac{E - E_F}{kT}\right)} \tag{4}$$

Based on these equations, n and N_D^+ can be computed. It is shown that under thermal equilibrium, the majority carrier concentration n is close to the well doping N_D (10^{17} cm^{-3}) at

room temperature (Fig. 5b) but it is significantly lower than N_D at cryogenic temperatures (Fig. 5c), due to the stronger incomplete ionization of dopants at these temperatures. Finally, two R_{BG} models are derived, one considering incomplete ionization for both n and μ_n and the other not. As shown in Fig. 3, the model with incomplete ionization is in good agreement with the experimental data in the whole temperature range whereas the other one (without incomplete ionization) being sufficiently precise until 150 K, strongly underestimates R_{BG} at cryogenic temperatures below that.

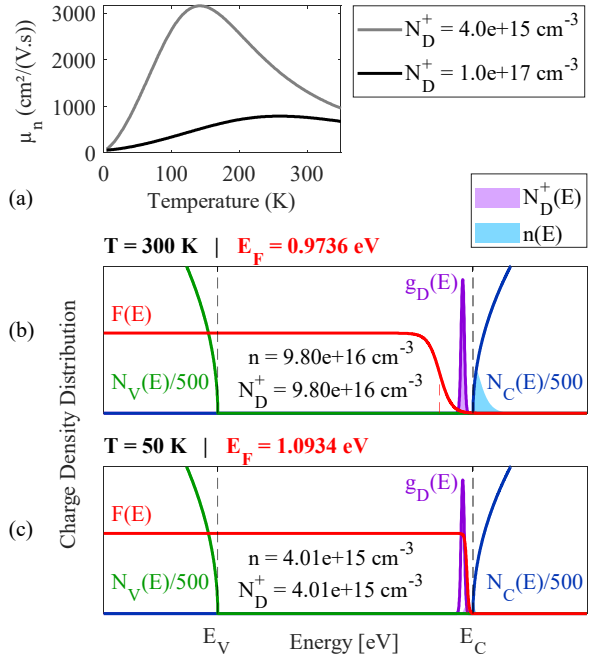

Fig. 5. (a) Electron mobility μ_n vs temperature using Caughey-Thomas model [12], [13] which includes doping- and temperature-dependent terms. (b-c) Band diagrams obtained from the 0D solution of the charge neutrality equation at (b) 300 K and (c) 50 K, where E_F is the Fermi energy, $g_D(E) = N_{GD} \exp(-(E_C-E_D-E)^2/W_{GD}^2)$ is the donor Gaussian distribution with an energy of E_D = 45 meV from the conduction band (corresponding to phosphorus) and a characteristic width of the Gaussian distribution of W_{GD} = 0.01 eV. N_{GD} is chosen to have the integral of $g_D(E)$ over energy equals to 10^{17} cm^{-3}.

C. Thermometry

After obtaining the reference $R_{BG}(T)$ curve (Fig. 3), different biasing conditions are now applied to the transistor, with V_{GS} ranging from 0 V to 0.9 V (with V_{DS} = 0.9 V), in order to achieve increasing levels of dissipated power ($P = I_{DS}V_{DS}$). Figs. 6a and 6b show an example of ΔV-I_{Force} and R_{BG}-power characteristics at 30 K for different V_{GS}, respectively.

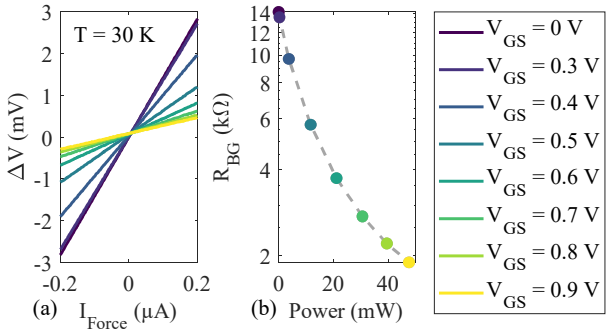

Fig. 6. (a) ΔV-I_{Force} characteristics of FET 1 at different gate voltages V_{GS} (V_{DS} = 0.9 V) at 30 K and (b) the corresponding R_{BG} vs power ($P = I_{DS}V_{DS}$).

By comparing R_{BG}'s power dependence (e.g. from ~14 kΩ to ~2 kΩ in a given example of 30 K, Fig. 6b) to the reference curve (Fig. 3), one can estimate the local average temperature increase ΔT in the well. Results are plotted in Fig. 7a for 4, 30, 77, 150 and 300 K. For all temperatures, one observes that ΔT increases in accordance with the dissipated power. At P = 40 mW, a ΔT of 33.4 K is reached at 4 K, whereas a more modest value of ΔT = 22 K is extracted at room temperature (Fig. 7b). ΔT extracted using front-gate thermometry (standard approach) is also higher at 4 K with respect to 300 K [14]. ΔT extracted using front-gate thermometry is expected to be higher than extracted with the back-gate thermometry, because the front-gate oxide is thinner than the BOX and thus the sensor is closer to the channel/"hot spot". Another key difference between both techniques is that ΔT extracted using back-gate thermometry is not decreasing monotonously (Fig. 7b) with ambient temperature at a fixed power level (e.g. $\Delta T_{77K} < \Delta T_{300K} < \Delta T_{4K}$), highlighting a complex interplay between the different material (i.e. silicon, silicon oxide, gate stack materials, metals) thermal conductivities and their thermal interface resistances, all being temperature dependent [11].

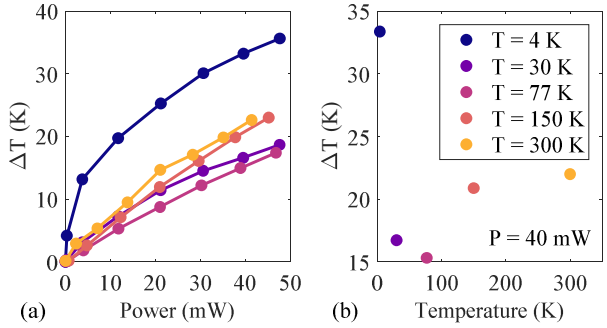

Fig. 7. (a) ΔT (extracted at the back-gate level) vs the dissipated power of FET 1 at different temperatures and (b) the corresponding ΔT extracted at P = 40 mW at each temperature.

IV. Thermal Coupling

In this section, the thermal coupling between two adjacent transistors is investigated. Referring to Fig. 1, FET 1 acts as the "aggressor" device, generating heat, while FET 2 serves as the "victim" device, experiencing a temperature increase ΔT due to the operation of FET 1. The drain current I_{DS2} of FET 2 is used as the temperature-sensitive metric.

The methodology follows the same general approach as back-gate thermometry. First, reference curves $I_{DS2}(T)$ are measured at several V_{GS2} values with FET 1 turned off. Then, FET 1 is activated to dissipate power, and the resulting variation in I_{DS2} is mapped to extract a temperature increase ΔT using the previously obtained calibration data.

A. DC Characteristics of FET 2

Fig. 8a shows I_{DS2}-V_{GS2} characteristics of FET 2 in the linear regime at different temperatures. The drain current I_{DS2} measured at V_{GS2} in the range between 0.2 and 0.4 V (by step of 10 mV) is chosen as the metric of reference. Being in the weak inversion regime in this bias range, I_{DS2} strongly depends on temperature, and does not require a derivation (contrarily to the case when g_m/I_D or subthreshold slope are used as a metric). In Fig. 8b, I_{DS2} as a function of temperature is plotted for five V_{GS2} values but in practice all V_{GS2} in the 0.2-0.4 V range are used to generate a calibration matrix.

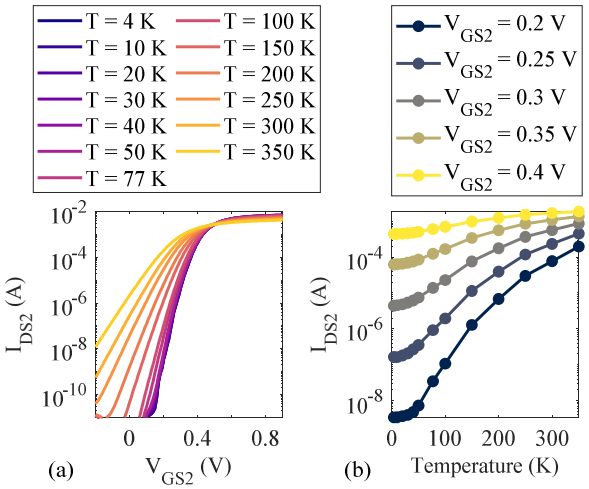

Fig. 8. (a) I_{DS2}-V_{GS2} characteristics of FET 2 in linear regime (V_{DS} = 50 mV) when FET 1 is biased at V_{GS} = 0 V and V_{DS} = 0.9 V and (b) the corresponding I_{DS2} vs temperature characteristics at different V_{GS2}.

B. *Thermal Coupling Effects*

Similarly to the back-gate thermometry, by repeating the measurements at different power levels and comparing the obtained I_{DS2} values vs power to the reference curves (at various V_{GS2}), one can extract the ΔT in the neighbor device (FET 2) as a function of the power dissipated by FET 1 (Fig. 9a). The local temperature increase is plotted in Fig. 9b as a function of ambient temperature at a dissipated power of 40 mW. Error bars correspond to the standard deviation computed by extracting ΔT at different V_{GS2} from 0.2V to 0.4 V (by step of 10 mV). From Fig. 9b, one can observe that the value of ΔT at 4 K (22.9 K) is lower than the value obtained from back-gate thermometry, which is not surprising because temperature is sensed at different positions. Indeed, the distance between FET 1 and FET 2 is larger than between FET 1 and its own well and the thermal paths/materials are also different. The non-linear behavior of ΔT with respect to ambient temperature (Fig. 9b), similar to the one in Fig. 7a, again suggests complex thermal heat dissipation paths between devices where some material thermal conductivities dominate over others in the different temperature ranges [15].

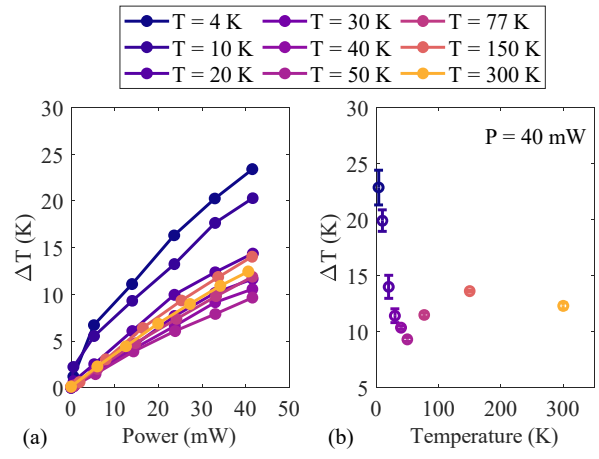

Fig. 9. (a) ΔT of FET 2 vs the dissipated power of FET 1 and (b) the corresponding ΔT extracted at P = 40 mW at each temperature. Error bars correspond to the standard deviation computed by extracting ΔT at different V_{GS2} from 0.2V to 0.4 V (by step of 10 mV).

V. Conclusion

In this work, a novel electrical-based temperature rise/self-heating extraction technique taking advantage of the transistor back-gate was elaborated. From the designer point of view, back-gate thermometry requires little layout effort as it uses the already available PDK standard cell without any additional design work. Furthermore, as the back-gate resistance increases sharply when temperature decreases, it provides a good alternative to front-gate thermometry for which the resistance tends to saturate at cryogenic temperatures. For our specific test structure, a temperature increase ΔT at the back-gate of 33.4 K was extracted at 4 K compared to ΔT = 22 K at room temperature (for a power of 40 mW). This study was supplemented by additional thermal coupling measurements between adjacent devices, providing another location where temperature is probed. To develop reliable quantum technologies, it is critical to characterize self-heating and heat dissipation effects and develop related models as an elevated temperature can alter the qubit state. Complementary extraction techniques, such as back-gate thermometry, front-gate thermometry and thermal coupling, which moreover sense the temperature at different locations, are thus needed for the development of accurate cryo-PDK models.

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