Characterization and Modeling of the Effect of Lateral Electric Field in Cryo-CMOS Transistors

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***Abstract*—This paper investigates the impact of the lateral electric field induced by the drain-source voltage on incomplete ionization in bulk CMOS transistors at cryogenic temperatures. It demonstrates how this effect influences DC currents, channel conductivity, and low-frequency noise across two technology nodes, while also examining the role of the lightly-doped-drain (LDD) regions in shaping these behaviors. A physics-based model for cryogenic operation is proposed based on dopant ionization through tunneling. By validation using both DC and low-frequency noise measurements, the model reveals that the observed electrical and noise characteristics stem from a single underlying physical mechanism, marking a crucial step toward a complete cryogenic compact model.**

***Index Terms*—Cryogenic electronics, Cryo-CMOS, quantum computing, incomplete ionization, cryogenic modeling.**

I. Introduction

Cryo-CMOS technology is gaining growing attention thanks to its expanding application areas, including quantum computers and cryogenic sensors [1]. Due to the drastic cryogenic shift in device characteristics, a compact model specifically tuned for the cryogenic operation of MOS transistors is necessary for reliable circuit design. Since incomplete ionization due to carrier freeze-out is an essential element of such models [2]–[4], any ionization induced by gate/drain-dependent electric field plays a crucial role. While the effect of gate-induced vertical electric field on field-assisted-ionization is included in early cryogenic compact models [2], [3], the effect of the lateral electric field induced by the V_{DS} has been investigated only in LDMOS devices and down to 77 K so far [5], despite its relevance. For instance, the g_{DS}-V_{DS} characteristics (Fig. 1) exhibit a marked deviation from the expected behavior as described by the simplified equation for room temperature in the linear region:

$$g_{DS} = \mu C_{ox} (W/L) (V_{GS} - V_{TH} - V_{DS}) \qquad (1)$$

The observed deviation at low V_{DS}, and hence low lateral field, highlights the effect of the V_{DS}-induced electric field at low drain bias. This region is especially relevant when transistors are used as switches, such as in sample-and-hold and other switched-capacitor circuits.

To include these effects in a lateral-field-aware cryogenic model, this paper investigates the effects of lateral field on DC and low-frequency-noise measurements and proposes a physics-based model to explain both effects based on the same physical origin.

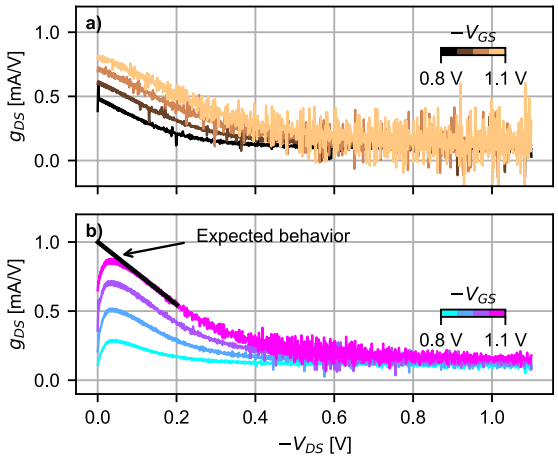

Fig. 1. g_{DS}-V_{DS} measurement of a 40-nm PMOS (W/L=1 μm/40 nm): a) standard behavior at 300 K; b) deviation for low V_{DS} at 4.2 K.

II. Effect of Lateral Electric Field on Conductance

Using a multiplexed 40-nm bulk-CMOS structure [6], the systematic behavior of the g_{DS} anomaly is tested to exclude random measurement errors. The same behavior –within matching limits [7]– appearing in eight identical devices (Fig. 2a) demonstrates that the anomaly is systematic, while comparing devices with different geometries (Fig. 2b-c) shows a stronger effect for shorter channels and lower V_{GS}. The same behavior also appears in 160-nm CMOS thick-oxide devices (Fig. 3), thus proving it is not technology-specific, although it may be affected by the specific doping profile.

To explain this behavior, present models [2], [3], which include only the gate-induced electric-field-assisted ionization, must be revisited. For a p-type polysilicon gate and an n-type bulk, the Fermi level E_F is below the donor energy E_D with the help of band-bending (Fig. 4) [2]. Thus, present models predict the ionization in the channel induced by the vertical electric field. On the contrary, since the lightly doped drain (LDD) regions have the same doping type as the gate, acceptor energy level E_A stays above E_F, and band bending due to nominal negative voltages does not create ionization, at least according to the existing model. As incomplete ionization in the LDD would result in low conductance, the lateral electric field must necessarily contribute to field-dependent ionization in these regions.

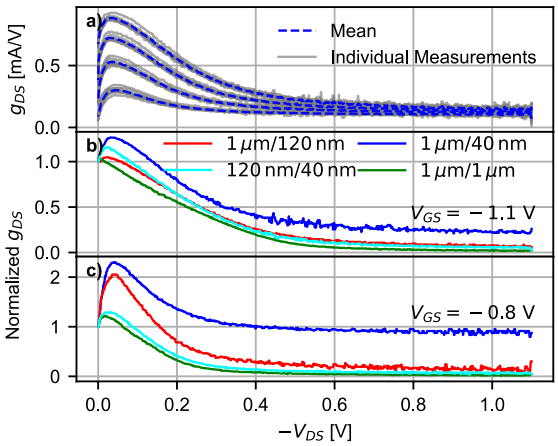

Fig. 2. a) g_{DS}-V_{DS} measurements of eight identical W/L = 1 μm/40 nm PMOS devices and their mean for V_{GS} = −0.8 V, −0.9 V, −1 V, −1.1 V. b-c) g_{DS}-V_{DS} measurements of four devices with different geometries, normalized to the value at V_{DS} = 0 V for b) V_{GS} = −1.1 V and c) V_{GS} = −0.8 V.

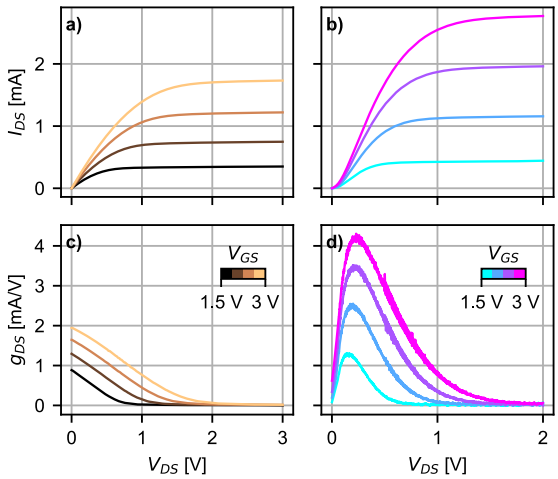

Fig. 3. I_{DS}-V_{DS} (a,b) and g_{DS}-V_{DS} (c,d) measurement results of a 5-V thick-oxide 160-nm bulk NMOS (W/L=10 μm/1.2 μm) at 300 K (a,c) and at 4.2 K (b,d).

To develop a lateral-electric-field-aware ionization model, the conductivity of doped silicon σ is expressed as a function of the transmission probability $T(E)$, the total electric field magnitude E, the tunnel attempt frequency f, the measurement time t, unit charge q, doping concentration N_D, and carrier mobility μ:

$$\sigma = T\left(E\right) ftN_D q\mu \tag{2}$$

Even though models based on nuclear tunneling or Fermi's Golden Rule [6], [8], [9] are more physically accurate to compute $T(E)$, they are computationally expensive and not suitable for a compact modeling perspective. As an alternative, we use the WKB approximation for a parabolic barrier [10]:

$$T\left(E\right) = exp\left[-\frac{\pi m^* \left(U'\right)^{\frac{3}{2}}}{2\sqrt{2}q\hbar E}\right] \tag{3}$$

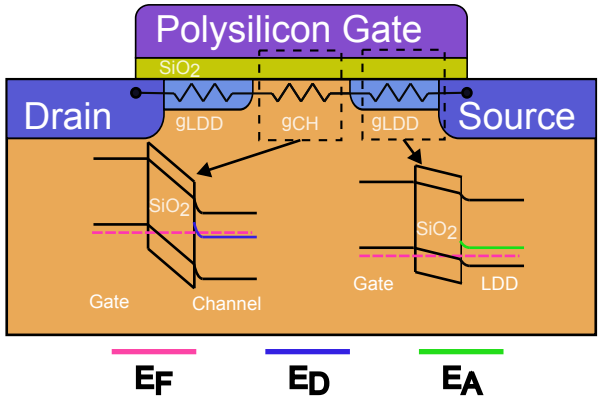

Fig. 4. Illustration of a p-type MOSFET with band diagrams for the LDD and channel regions.

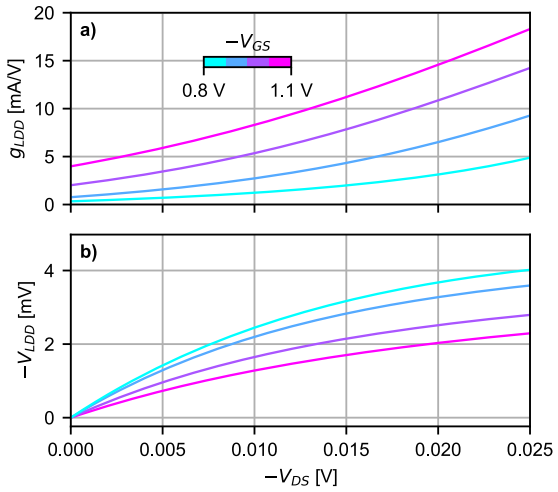

Fig. 5. Calculated a) g_{LDD} and b) voltage drop in the LDD, V_{LDD}, for a W/L = 1 μm/40 nm PMOS at 4.2 K.

where m^* is the carrier effective mass, U' is reduced barrier energy, and $\hbar$ is the reduced Planck constant.

With those assumptions, while constants in Eq. 2 and Eq. 3 can be fitted easily, the electric field in the LDD region–or equivalently the voltage drop across the LDD–and its conductance are key parameters in this model and must be calculated. To compute the electric field in the LDD region, the following methodology is adopted.

The total drain-to-source conductance can be modeled by the combination of the conductance describing the LDD regions (g_{LDD}) and the intrinsic channel (g_{CH}), as in Fig. 4. Since the region of interest is mainly limited to low drain voltages and relatively high gate bias, the resistances of the two LDD regions are assumed identical. As the LDD regions become highly conductive in the fully ionized regime, g_{DS} is dominated by g_{CH}, leading to the expected linear V_{DS} dependence of Eq. 1. The deviations from Eq. 1 are then caused by the non-linear LDD resistances due to incomplete ionization. By using the standard model in Eq. 1 for g_{CH},

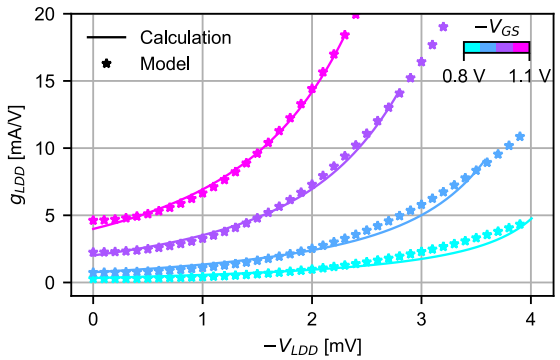

Fig. 6. Measured g_{LDD}-V_{LDD} characteristics (from Fig. 5) and model of a W/L = 1 μm/40 nm PMOS at 4.2 K.

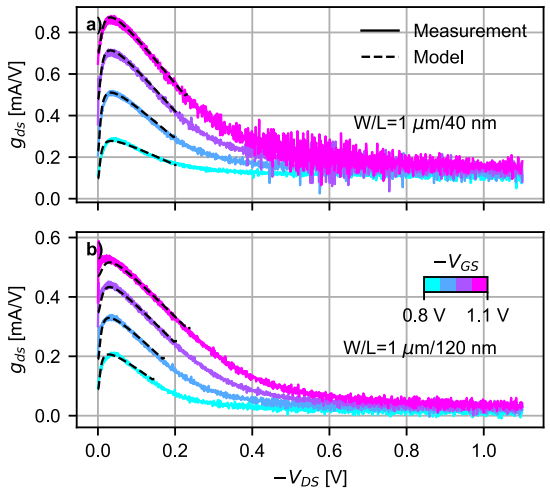

Fig. 7. Reconstructed measurement results using the proposed model for a) W/L = 1 μm/40 nm and b) W/L = 1 μm/120 nm PMOS.

both g_{LDD} and the voltage across the LDD region (V_{LDD}) can be computed from the measurements, as in Fig. 5. By using V_{DS} as a parameter, g_{CH}-vs.-V_{LDD} can be plotted (Fig. 6) to benchmark the model.

By using only the first two terms of the binomial expansion of the reduced barrier energy equation [10] in Eq. 2 and Eq. 3, the physical model in Eq. 4 and Eq. 5 is obtained. In this model, physical constants and uncertain parameters, such as mobility and doping concentration, are grouped into fitting parameters, where k_0 represents the pre-exponential factor, k_1 accounts for the barrier drop induced by the electric field, and k_2 models the V_{GS}-dependent vertical component of the total electric field. The term C is treated as a constant, and the values of these parameters are extracted by fitting the data in Fig. 6.

$$g_{LDD} = k_0 exp\left[-\frac{C\left(1-k_1\sqrt{E}\right)}{E}\right] \tag{4}$$

$$E = \sqrt{k_2^2 + \left(\frac{V_{LDD}}{L_{LDD}}\right)^2} \tag{5}$$

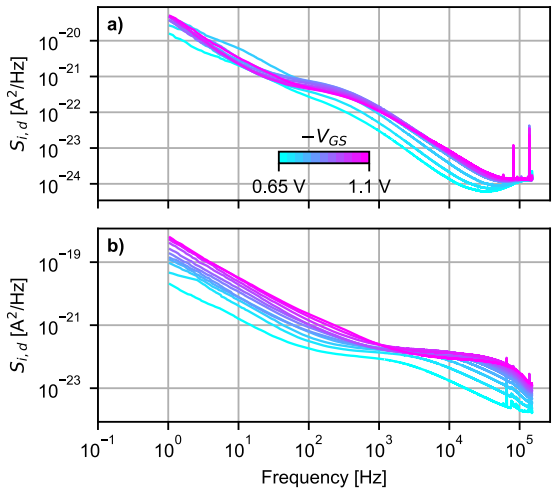

Fig. 8. Noise characterization of W/L = 1 μm/1 μm PMOS in a) triode region ($V_{DS} = -50$ mV) and b) saturation region ($V_{DS} = V_{GS}$).

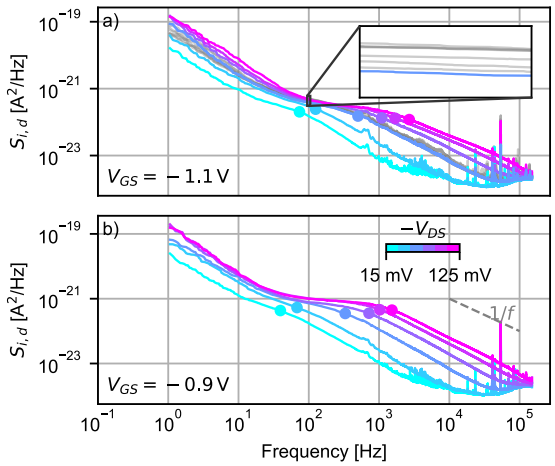

Fig. 9. Noise characterization of a W/L = 1 μm/1 μm PMOS with various V_{DS} when a) $V_{GS} = -1.1$ V and b) $V_{GS} = -0.9$ V. Measurements of eight identically sized devices at $V_{DS} = -50$ mV is shown in the inset in a). Dots indicate the cutoff frequency for each curve.

By computing V_{DS} and g_{DS} as functions of V_{LDD} using Eq. 4 and Eq. 5, the g_{DS}-V_{DS} curves are reconstructed in Fig. 7a. Since the LDD profile is expected to be similar across device geometries within the same technology, the model is applied to both short and long devices by keeping the LDD-related parameters fixed and scaling only the linear channel conductance (g_{CH}). The good agreement with the measurements in Fig. 7b confirms the model's scalability.

III. Effect of Lateral Electric Field on Noise

The incompletely ionized dopant atoms in the LDD region introduce excess noise at cryogenic temperatures and their emission rate can be expressed as $e_n = T(E)\, f$ [10]. To test this effect, noise measurements using the setup described in [6] were performed on large devices to minimize the effect

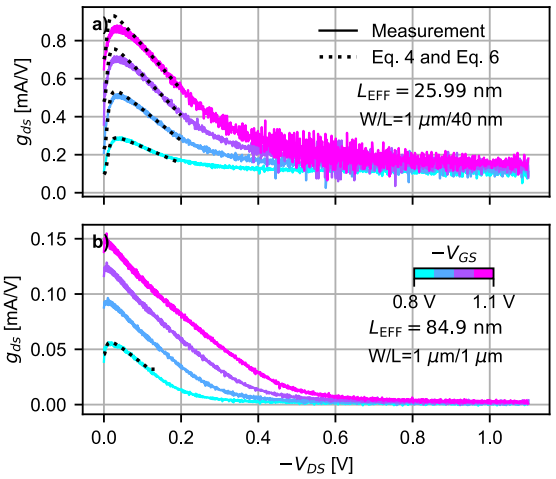

Fig. 10. a) Comparison of the model using (4) and (6) with experimental results for PMOS devices with W/L = 1 μm/40 nm and b) W/L = 1 μm/1 μm, only at $V_{GS} = -0.8$ V.

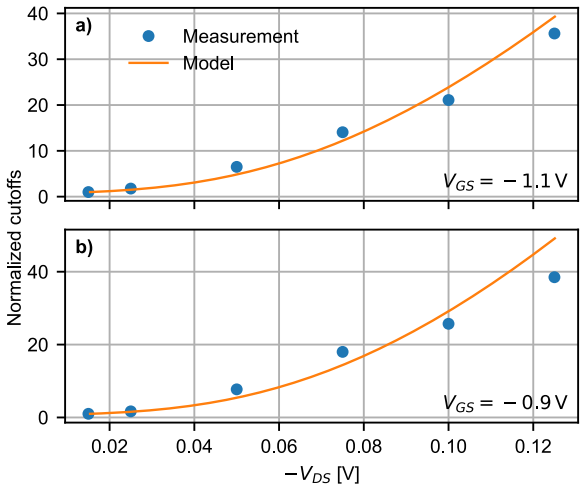

Fig. 11. Calculated normalized cutoff frequencies and model prediction (7) for a) $V_{GS} = -1.1$ V and b) $V_{GS} = -0.9$ V. $V_{DS0} = -15$ mV.

of standard random traps. By comparing the noise in triode and saturation in Fig. 8, almost no frequency shift is observed on the flat plateau in triode operation, whereas a clear shift appears in saturation, highlighting the role of the lateral electric field in the noise spectrum. Repeating the measurements on eight identical devices (inset in Fig. 9a) highlights the systematic nature of the observed behavior. Across different bias conditions, a pronounced plateau followed by a 1/f-like roll-off indicates clustered dominant noise sources. To investigate the systematic behavior of these noise sources, the -3-dB cutoff frequency at which the 1/f roll-off takes over is systematically extracted for each bias and marked in Fig. 9.

To benchmark the model, the V_{LDD} corresponding to an applied V_{DS} must be defined. As g_{CH} is dominant in long-channel devices and suppresses the effect of g_{LDD} at low drain biases and high gate biases, the extraction method proposed in Section II is numerically unstable. As a workaround, the V_{LDD}-V_{DS} relation (Fig. 5b) is linearized, and Eq. 5 is replaced by Eq. 6 by introducing the effective length L_{eff}:

$$E = \sqrt{k_2^2 + \left(\frac{V_{DS}}{L_{eff}}\right)^2} \tag{6}$$

A single L_{eff} is fitted for all biases in the short-channel device, as shown in Fig. 10a. For the long-channel device, L_{eff} is extracted using low-gate-bias measurements, as shown in Fig. 10b. To model the noise behavior, the emission rate equation is employed, leading to Eq. 7, which is normalized to the first data point to remove dependence on k_0:

$$\frac{f_C\left(V_{DS}\right)}{f_C\left(V_{DS0}\right)} = \frac{exp\left[-\frac{C\left(1-k_1\sqrt{E(V_{DS})}\right)}{E(V_{DS})}\right]}{exp\left[-\frac{C\left(1-k_1\sqrt{E(V_{DS0})}\right)}{E(V_{DS0})}\right]} \tag{7}$$

Model predictions using the extracted L_{eff} are compared with measurements in Fig. 11 for two gate biases, demonstrating that the model accurately captures the observed trends.

IV. Conclusions

The presented model highlights the role of the lateral field in a complete cryogenic compact model, validated through experimental and physical-model benchmarks on both conductance and noise. It also provides a plausible cause for the observed excess and systematic noise sources in [6], [11]. As a result, this work lays the groundwork for future compact models needed for reliable cryo-CMOS circuit design.

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