A Scalable Sub-Ranging Voltage Reference Achieving 4.9ppm/°C from -40°C to 125°C

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***Abstract*—This work presents a low-drift voltage reference based on a scalable sub-ranging temperature coefficient (TC) compensation method, which divides a wide operating temperature range into *N* continuous sub-ranges. This design adopts a conductance-ratio-based k-selector for independent compensation parameter control, a sensor-less multi-sub-range detection scheme based on internal node voltage comparison, and seamless output transitions at boundary temperatures with inherent process, voltage and temperature (PVT) insensitivity. Fabricated in a 180nm CMOS process, the proposed voltage reference with three sub-ranges achieves an average untrimmed TC of 4.9ppm/°C over -40°C to 125°C and an initial inaccuracy of ±0.16% (3σ).**

I. Introduction

The temperature stability of voltage references plays a critical role in high-precision signal chains, particularly for data converters. A low temperature coefficient (TC) drift below 10ppm/°C is critical for high resolution ADC references. Conventional first-order TC compensation schemes for bandgap references cannot fully suppress the inherent higher-order temperature nonlinearity, leaving residual drift that limits stability over wide operating temperature ranges. Multi-segment TC compensation is accomplished by multi-segment compensation currents that are triggered at different temperature thresholds. Although this approach improves upon first-order designs by shaping the temperature characteristic, the switching thresholds and compensation magnitude of each segment are highly process-sensitive, leading to excessive tuning complexity and poor robustness against process variation. The sub-ranging compensation approach divides a wide temperature range into narrower continuous sub-ranges, where first-order compensation can be applied independently to mitigate higher-order nonlinearity. However, existing sub-ranging designs still face critical limitations: they either suffer from output voltage discontinuities at sub-range boundary temperatures [1], or rely on non-scalable architectures that cannot meet the increasingly stringent TC requirements of high-precision signal chains [2].

To address these limitations, this work proposes a seamless-output voltage reference architecture with N sub-ranges (N≥3). The proposed architecture achieves full structural integration, with a sensor-less sub-range detection scheme, and a conductance-ratio-based k-selector that enables independent control of each compensation parameter k_n. Chopping and dynamic element matching (DEM) techniques are combined to further suppress residual low-frequency noise and offset. A voltage reference with three sub-ranges is implemented, which achieves a competitive untrimmed TC performance.

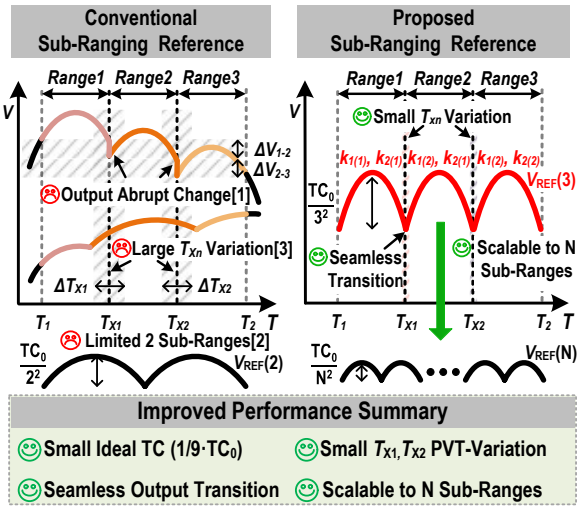


Fig. 1. Performance comparison of the proposed sub-ranging reference with prior sub-ranging references.

II. Circuit Architecture

A. Seamless-output Voltage Reference with Three Sub-Ranges

As shown in Fig. 1, the operating temperature range in this design is divided into three sub-ranges, where T_{X1} and T_{X2} are the two boundary temperatures between adjacent sub-ranges. By properly setting the TC compensation parameters k_1 and k_2 in each sub-range, the first-order TC compensation is achieved. The proposed voltage reference achieves PVT-insensitive boundary temperatures T_{x1} and T_{x2}, and ensures seamless transitions of the three-sub-range output voltage $V_{REF}(3)$ at these temperatures. Moreover, the architecture is scalable to N sub-ranges, for which the ideal TC is TC=1/N²·TC₀ (1/9·TC₀ for N=3), where TC₀ represents the residual TC after first-order compensation.

Fig. 2 shows the schematic of the proposed circuit and the expression for $V_{REF}(3)$:

$$V_{REF}(3)=I_{REF}(3)\cdot R_L=\frac{k_1\cdot\Delta V_{BE1}+k_2\cdot\Delta V_{BE2}+(1-k_1-k_2)\cdot V_{BE0}}{k_1R_1+k_2R_2+(1-k_1-k_2)\cdot R_3}\cdot R_L \quad (1)$$

where V_{BE0} and $\Delta V_{BE1}=V_{BE0}-V_{BE1}$, $\Delta V_{BE2}=V_{BE0}-V_{BE2}$ which have CTAT and PTAT characteristics, respectively. $V_{REF}(3)= I_{REF}(3)\cdot R_L$, where $I_{REF}(3)$ is the output current.

In the circuit, k_1 and k_2 are realized by the k-selector. As shown in Fig. 3, V_4 is the weighted sum of V_1, V_2, V_3 ($V_4=k_1\cdot V_1+k_2\cdot V_2+k_3\cdot V_3$) and $k_n=s_{Tn}/s_{Tsum}$, where s_{Tn} is the conductance of resistor R_{Tn}, and s_{Tsum} is the sum of s_{T1}, s_{T2} and s_{T3}. By controlling R_{T1}, R_{T2}, k_1, k_2 can be

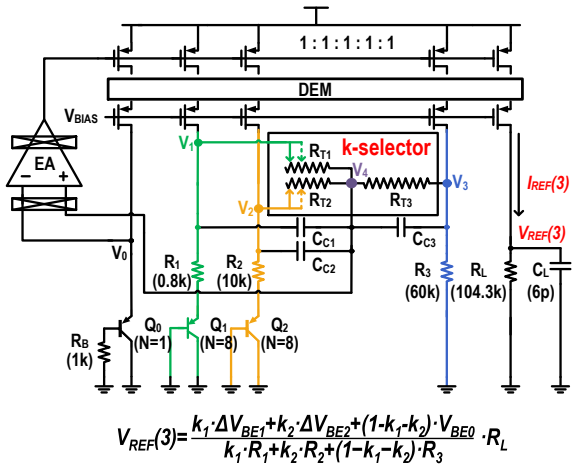


Fig. 2. Schematic of the proposed seamless-output voltage reference with three sub-ranges.

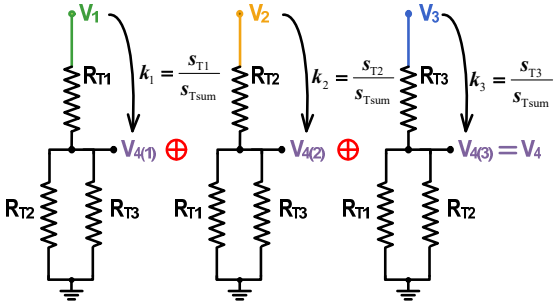


Fig. 3. Generation of k_n via the superposition principle.

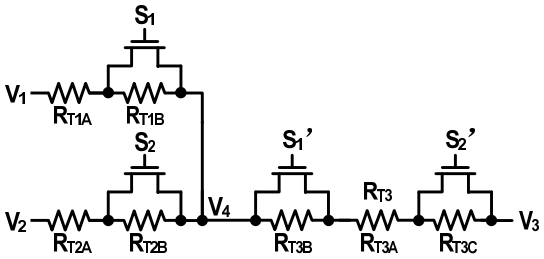


Fig. 4. Circuit implementation of the k-selector and its operating principle.

independently adjusted while tuning R_{T3} to maintain constant s_{Tsum}. As shown in Fig. 4, during range transitions, the conductance of R_{Tn} is modulated by enabling/disabling series resistors, thereby switching k_n. This conductance-ratio-based control enables independent tuning and switching of k_1 and k_2. Moreover, k_1 and k_2 are determined by R_{Tn} ratios, making them inherently PVT-insensitive.

A key feature of the $V_{REF}(3)$ expression is that its numerator and denominator share the same algebraic form with respect to k_1 and k_2. As illustrated in Fig. 5, taking k_1 as an example: the terms independent of k_1 in the numerator and denominator of the $V_{REF}(3)$ expression are regarded as constants m, n, respectively, and the coefficients of k_1 in the numerator and denominator are set as μ, η, respectively. It follows that $V_{REF}(3)$ becomes independent of k_1 when $\mu/\eta=m/n=\theta$, which defines the boundary temperature $T=T_{X1}$. Similarly, T_{X2} can be defined where the output voltage $V_{REF}(3)$ is independent of k_2. Thus, switching k_n at the corresponding T_{Xn} ensures a seamless output voltage transition. The condition that

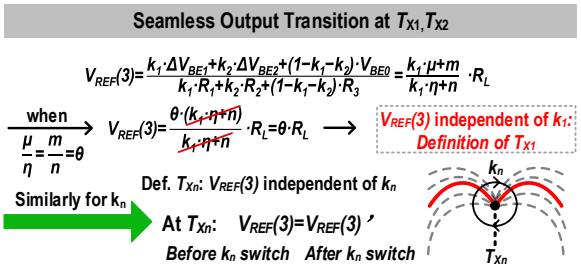


Fig. 5. Principle enabling seamless output transitions at T_{X1}, T_{X2}.

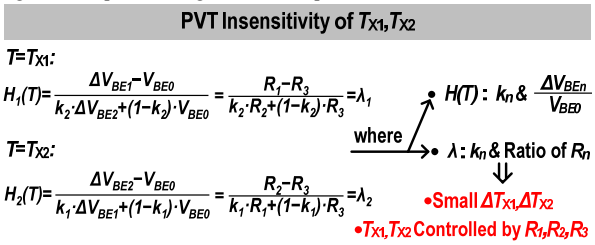


Fig. 6. Control of T_{X1}, T_{X2} and their inherent PVT insensitivity.

$V_{REF}(3)$ is independent of k_n uniquely determines T_{Xn}, as illustrated in Fig. 7.

As shown in Fig. 6, T_{Xn} is determined by the function $H_n(T)$ and the coefficient λ_n. $H_n(T)$ depends on k_n, $\Delta V_{BEn}/V_{BE0}$, and λ_n is determined by k_n and the R_n resistance ratio. This characteristic inherently guarantees the PVT insensitivity of T_{Xn}. T_{Xn} is uniquely determined by λ_n. A unique set of T_{X1}, T_{X2} can be determined from a single set of resistors R_1, R_2, R_3. In this design, T_{X1}, T_{X2} are set near the trisection points of the entire temperature range.

Accurate sub-range detection relies on precise identification of the boundary temperatures T_{Xn}. For T_{X1}, $I_{REF}(3)$ is k_1-independent ($I_{REF}(3)|_{k1=0}=I_{REF}(3)|_{k1=1}=i$) at $T=T_{X1}$. By substituting $k_1=0$ and $k_1=1$ into the expression of $I_{REF}(3)$ respectively and simplifying the results, (3) is obtained:

$$I_{REF}(3)=\frac{k_1\cdot\Delta V_{BE1}+k_2\cdot\Delta V_{BE2}+(1-k_1-k_2)\cdot V_{BE0}}{k_1R_1+k_2R_2+(1-k_1-k_2)\cdot R_3} \quad (2)$$

$$V_{BE1}+iR_1=k_2\cdot\Delta V_{BE2}+(1-k_2)\cdot V_{BE}-k_2\cdot i\cdot(R_2-R_3)=i\cdot R_3 \quad (3)$$

From the circuit shown in Fig. 2, the term $V_{BE1}+i\cdot R_1$ in (3) is equal to the voltage expression of node V_1 in Fig. 2, and the term $i\cdot R_3$ in (3) is equal to the voltage expression of node V_3 in Fig. 2. Thus, when $T=T_{X1}$, $V_1=V_3$. Similarly, when $T=T_{X2}$, $V_2=V_3$. As shown in Fig. 7, since V_1 has a more negative TC than V_3, comparing V_1 with V_3 identifies whether $T<T_{X1}$ or $T>T_{X1}$. Similarly, comparing V_2 with V_3 detects T_{X2}. By combining these two comparisons, sensor-less detection of the three sub-ranges is realized. This analysis confirms that T_{Xn} is uniquely determined by λ_n.

The PVT insensitivity of this approach is further confirmed by Monte Carlo simulations (covering process variations and device mismatch) of the output TC with an average TC of 4.5ppm/°C, as shown in Fig. 8.

In Fig. 2, a 50kHz DEM cascode current mirror mitigates channel-length modulation and current mirror mismatch for $V_{REF}(3)$'s line/load sensitivity and temperature stability. The error amplifier is 10kHz chopper-stabilized to suppress offset-induced nonlinear TC.

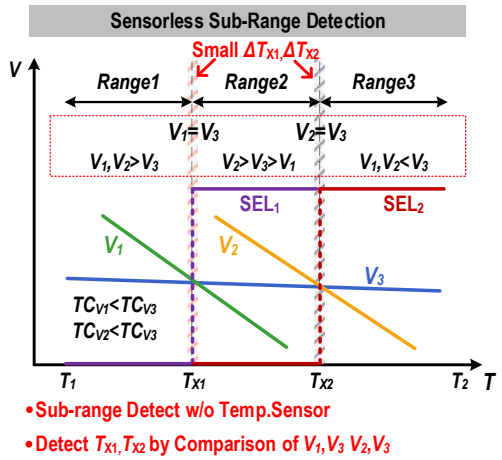


Fig. 7. Principle enabling sensor-less temperature sub-range detection.

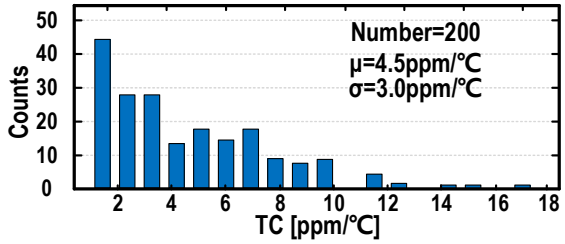


Fig. 8. Monte Carlo simulation results of the output voltage TC.

Both DEM and chopping reduce 1/f noise. Local electrical isolation is implemented on power-noise-sensitive paths for improved PSRR performance. R_B beneath Q_0 compensates for temperature-dependent β of Q_0-Q_2.

B. Scheme of the Seamless-Output Voltage Reference with N Sub-Ranges

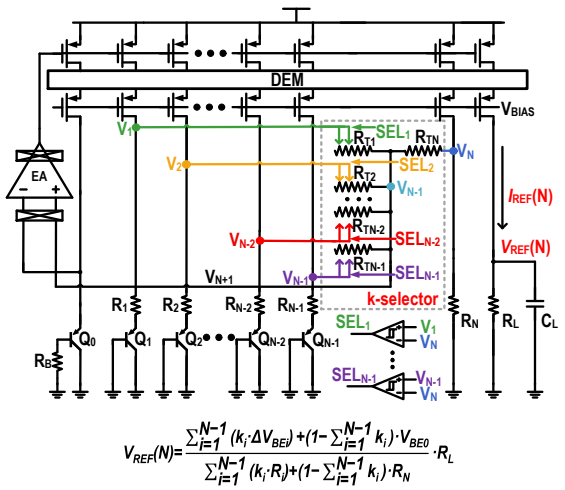
In this design, the operating temperature range is divided into N continuous temperature sub-ranges, where T_{Xn} is the boundary temperature between adjacent sub-ranges. Within each sub-range, by configuring the values of k_n, the first-order TC compensation is achieved. Fig. 9 presents the scheme of the proposed circuit and $V_{REF}(N)$ expression. In the expression, V_{BE0} and $\Delta V_{BEi}=V_{BE0}-V_{BEi}$ which have CTAT and PTAT characteristics, respectively.

Similar to $V_{REF}(3)$, the numerator and denominator of the $V_{REF}(N)$ expression share an identical algebraic form with respect to the coefficients k_n. By defining T_{Xn} as the temperature at which $V_{REF}(N)$ becomes independent of k_n, seamless switching of $V_{REF}(N)$ at the sub-range boundary temperature T_{Xn} is realized. And the boundary temperatures T_{X1},T_{X2}, ..., T_{XN-1} can be uniquely determined by the values of R_1, R_2, ..., R_{N-1}, and the control process ensures the inherent PVT insensitivity of T_{Xn}.

In the proposed k-selector, V_{N+1} is the weighted sum of V_1, V_2, …, V_N:

$$V_{N+1}=\sum_{i=1}^{N} k_n \cdot V_n, k_n=\frac{sT_n}{\sum_{i=1}^{N} sTi}=\frac{sT_n}{sT_{sum}} \quad (4)$$

where k_n is controlled by conductance ratios. This conductance-based control model provides an independent and easily tunable network to set and switch the k_n. Furthermore, k_n is determined by R_{Tn} ratios, inherently PVT-insensitive.



$$V_{REF}(N)=\frac{\sum_{i=1}^{N-1}(k_i\cdot\Delta V_{BEi})+(1-\sum_{i=1}^{N-1}k_i)\cdot V_{BE0}}{\sum_{i=1}^{N-1}(k_i\cdot R_i)+(1-\sum_{i=1}^{N-1}k_i)\cdot R_N}\cdot R_L$$

Fig. 9. Scheme of the proposed seamless-output voltage reference with N sub-ranges.

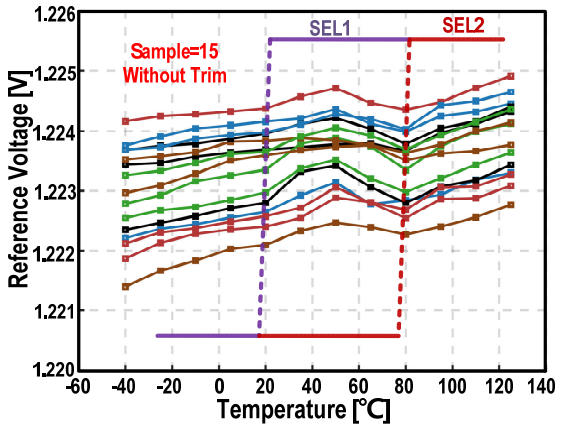


Fig. 10. Measured reference voltage of 15 chips over -40°C to 125°C.

By substituting k_1=0 and k_1=1 into the expression of $I_{REF}(N)$ respectively, and leveraging the difference in temperature characteristics between V_n (n=1, 2, …, N-1) and V_N, the proposed architecture accurately detects N (N≥3) sub-ranges without external temperature sensors. This scheme provides solid theory support for lower TC and better robustness in wide temperature range.

A prior seamless-output current reference with two sub-ranges limited achieves an average TC of 11.4ppm/°C [2]. This level of performance is insufficient for many high-precision applications. In comparison, the theoretical TC of this work is only 40% of that of the N=2 architecture in [2]. The measurement results further demonstrate that this work achieves an average TC of 4.9ppm/°C, which satisfies the requirements of high-precision application scenarios with minimal area and power overhead. For this reason, N=3 is selected in this work as a practical tradeoff.

III. Measurement Results

Implemented in 180nm CMOS (0.12mm², Fig. 13(b)), it consumes 55μA at 2.2V; Fig. 10 shows the measured $V_{REF}(3)$ of 15 chips across -40°C to 125°C. The measured TC ranges from 3.0 to 6.9ppm/°C, with an average of 4.9 ppm/°C as detailed in Fig. 11(a). The untrimmed inaccuracy is characterized by a standard deviation (σ) of 0.65mV, corresponding to σ/μ=0.053% (Fig. 11(b)). Fig. 12 shows the output noise spectrum (4.5μVrms, 0.1-10Hz

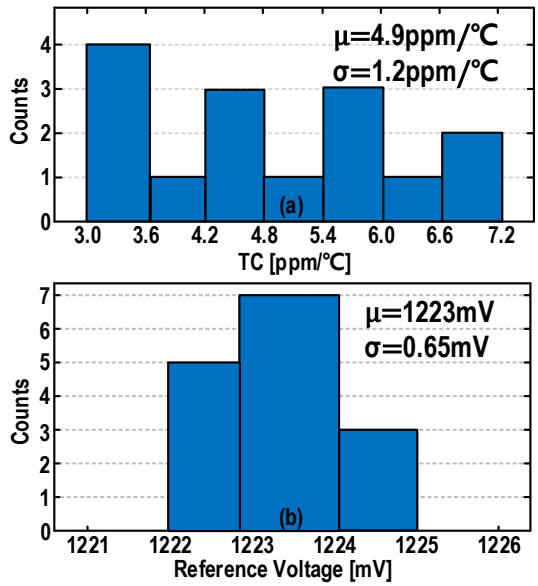


Fig. 11. Histograms of (a) TC and (b) average reference voltage.

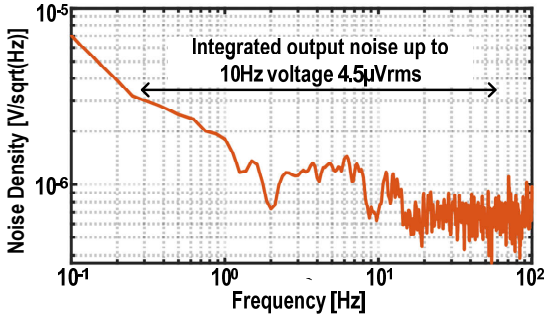


Fig. 12. Measured output noise of the implemented voltage reference.

integrated). Fig. 13 shows the PSRR (-95dB@10Hz, -68dB@10kHz), and line regulation (0.112% over 2.2-5V).

The performance of the proposed voltage reference is comprehensively summarized and compared with state-of-the-art CMOS voltage references based on three mainstream TC compensation topologies in Table I. Compared with prior works, this work proposes a sub-ranging TC compensation architecture that achieves excellent performance without trimming, highlighting its advantages in accuracy and temperature stability. Specifically, it achieves the lowest average TC and initial inaccuracy among the compared works, while also delivering competitive noise and PSRR performance, as summarized in Table I.

IV. Conclusion

This article presents a low-drift voltage reference based on a scalable sub-ranging TC compensation method, which achieves an average untrimmed TC of 4.9ppm/°C from -40°C to 125°C and an initial inaccuracy of ±0.16% (3σ). A conductance-ratio-based k-selector, sensor-less sub-range detection, and seamless output transition at boundary temperatures are implemented to ensure PVT insensitivity.

Acknowledgement

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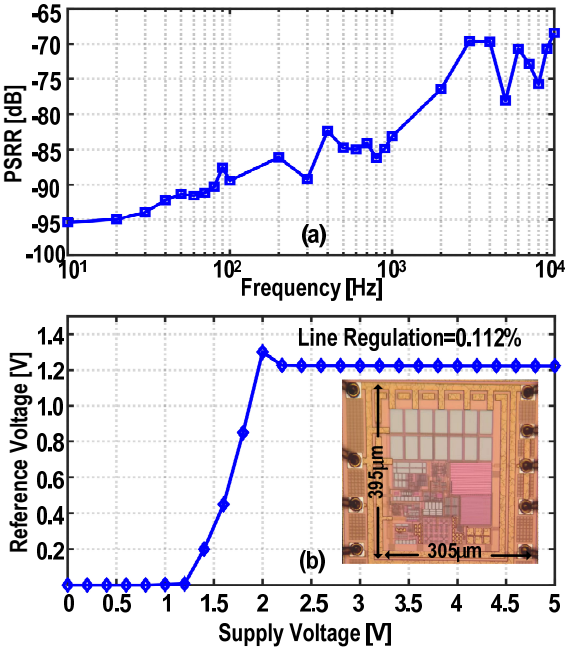

Fig. 13. Measured (a) output PSRR, (b) line regulation of the implemented voltage reference and die micrograph of the chip.

TABLE I. COMPARISON WITH STATE-OF-THE-ART WORKS

	This Work	JSSC'21 [4]	JSSC'24 [2]	JSSC'11 [5]
Process (nm)	180	130	180	160
Method of TC Compensation	Sub-Ranging[a] (3 sub-ranges)	Multi-Segment	Sub-Ranging[b] (2 sub-ranges)	V_{BE} Linearization
V_{DD} (V)	2.2-5	2-3.3	1.3-2.4	1.8±10%
Supply Current (μA)	55	120	43.5	55
Inaccuracy (%)	±0.16	±1.62	±1.61[b]	±0.75
TC Trimming	No	No	Batch	1-pt
TC Range (°C)	-40-125	-40-150	-20-125	-40-125
Best/Average TC (ppm/°C)	3.0/4.9	5.7/8.75	7.8/11.4	5/N.A
Noise (μVrms) (0.1-10Hz)	4.5	1158	N/A	6.1
PSRR (dB@Hz)	-95@10 -68@10K	-82@10 -45@10K	N/A	-74 @dc
Line Sensitivity (%)	0.112	0.03	0.126	N/A
Area (mm^2)	0.12	0.08	0.08	0.12

a.Scalable. b.Current reference.

References

[1] C. -W. U, C. Liu, R. P. Martins and C. -S. Lam, "An 1 V Supply, 740 nW, 8.7 ppm/°C Bandgap Voltage Reference With Segmented Curvature Compensation," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 70, no. 12, pp. 4755-4766, 2023.

[2] P. Park, J. Lee and S. Cho, "A PVT-Insensitive Sub-Ranging Current Reference Achieving 11.4-ppm/ ° C From -20 °C to 125 °C," in IEEE JSSC, vol. 59, no. 12, pp. 4057-4067, 2024.

[3] B. Yousefzadeh, S. Heidary Shalmany and K. A. A. Makinwa, "A BJT-Based Temperature-to-Digital Converter With ±60 mK (3σ) Inaccuracy From −55 °C to +125 °C in 0.16-μm CMOS," in IEEE Journal of Solid-State Circuits, vol. 52, no. 4, pp. 1044-1052, 2017.

[4] K. Chen, L. Petruzzi, R. Hulfachor and M. Onabajo, "A 1.16-V 5.8-to-13.5-ppm/°C Curvature-Compensated CMOS Bandgap Reference Circuit With a Shared Offset-Cancellation Method for Internal Amplifiers," in IEEE Journal of Solid-State Circuits, vol. 56, no. 1, pp. 267-276, 2021.

[5] G. Ge, C. Zhang, G. Hoogzaad and K. A. A. Makinwa, "A Single-Trim CMOS Bandgap Reference with a 3σ Inaccuracy of ±0.15% from −40°C to 125°C," in IEEE JSSC, vol. 46, no. 11, pp. 2693-2701, 2011.