A 37.44GHz Fractional-N Harmonic Subsampling PLL Achieving 63.6fs$_{rms}$ Jitter and −49.2dBc Worst Case Fractional Spur

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***Abstract* — A 37.44GHz fractional (frac.)-N phase-locked loop (PLL) leveraging the harmonic subsampling (HSS) technique to improve the jitter and spurs is presented. Prototyped in 28nm CMOS, the proposed HSS-PLL achieves 63.6fs integrated rms jitter including frac. spurs at 37.4GHz, with a FoMs of −248.2dB. The measured reference spur is -71.4dBc, while the worst-case frac. spur is -49.2dBc.**

***Keywords*—Fractional-N, Phase-Locked Loop, Harmonic Subsampling, Low Jitter, Low Spur.**

I. Introduction

Mm-Wave frac.-N PLLs with low jitter and low spurs are demanded by high-speed communication systems. As shown in Fig. 1 (top), cascading a frequency multiplier after a GHz frac.-N PLL is a straightforward way to generate the mm-Wave frequencies [1], but at the cost of large power and area overhead from the frequency multiplier. Directly operating the VCO at mm-Wave frequencies suffers from high phase noise (PN) since the Q of the tunable capacitor degrades. Utilizing high-gain phase detectors (PDs), e.g., a bang-bang PD (BBPD) [2] or subsampling (SS) PD [3], to reduce the loop noise allows using a large loop bandwidth (BW) to suppress the VCO PN. Due to the narrow linear range of these high-gain PDs, a digital-to-time converter (DTC) is required to compensate for the quantization error (Q-error) induced by the frac.-N operation. The noise and linearity of the DTC depend on its delay range. In the digital SS-PLL [4], the required DTC range is limited by the SS-BBPD's maximum operating frequency. By using an analog polarity-reversible SSPD (PR-SSPD) [3], the required DTC range in a 27GHz SSPLL can be reduced to one VCO cycle (T_{VCO}) when using a 2nd-order delta-sigma modulator (DSM). However, further increasing the VCO frequency could degrade its PN performance, limiting the PLL's output jitter. The two-stage harmonic-mixing PLL can avoid using the DTC and the related time-consuming calibrations [5]. However, using two LC VCOs increases the chip area substantially.

The proposed harmonic subsampling (HSS) PLL relies on a VCO with implicit 2nd-harmonic extraction (Fig. 1-bottom). By using the PR-SSPD to directly sample the VCO's 2f_0 output, the required DTC range is reduced to T_{VCO}/2 (~26.7ps at f_0 = 18.7GHz) when a 2nd-order DSM is employed. Shrinking the DTC range improves its noise and linearity. The inductor coil for 2nd-harmonic extraction also isolates the VCO main tank from the 2f_0 output, effectively reducing the reference (ref.) spur induced by the SSPD.

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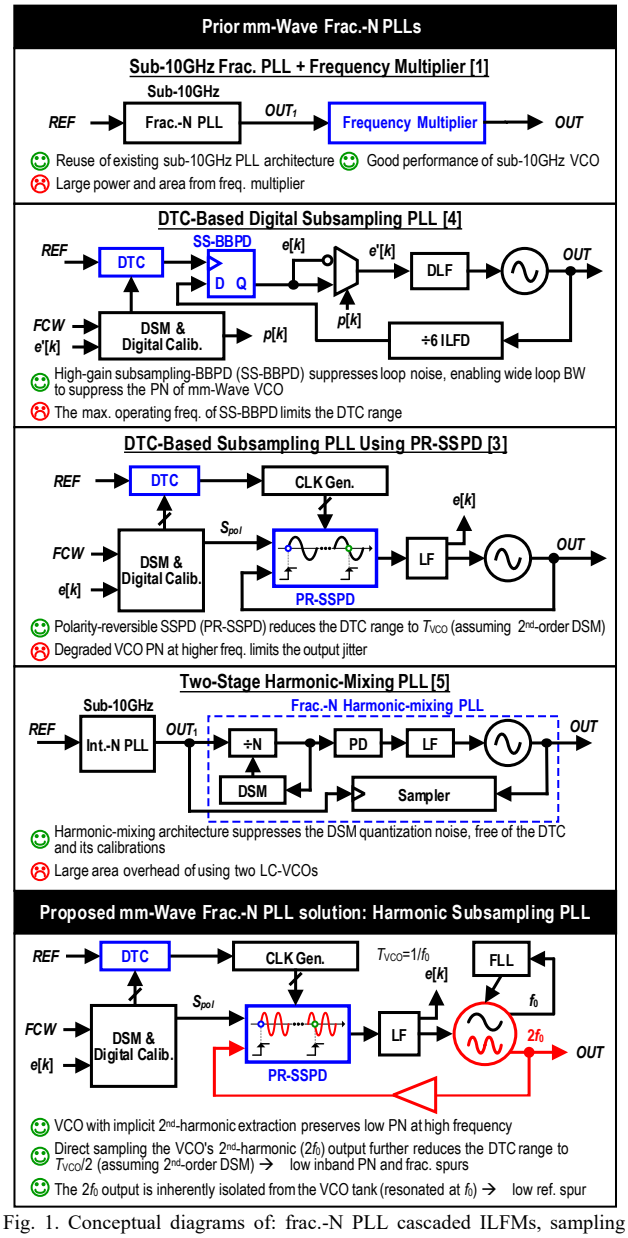


Fig. 1. Conceptual diagrams of: frac.-N PLL cascaded ILFMs, sampling BB-DPLL, proposed PLL.

II. Proposed Harmonic Subsampling PLL

A. Dual-Core Class-F^{-1} VCO with 2nd-Harmonic Extraction

The VCO with implicit 2nd-harmonic (2f_0) extraction [Fig. 2 (a)] is based on a dual-core inverse-class-F (class-F^{-1}) VCO [6], featuring a high-Q circular transformer for reducing the PN. The class-F^{-1} topology also features a high tank

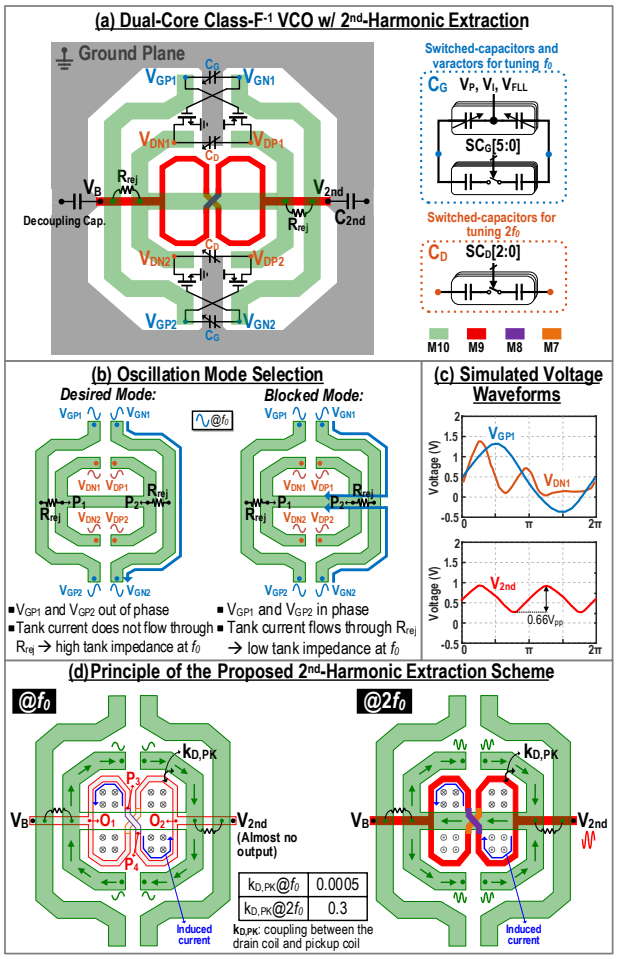


Fig. 2. Circuit diagram (a) of the dual-core class-F^{-1} VCO with 2nd-harmonic extraction, including the oscillation mode selection (b) and simulated voltage waveforms (c), and principle of the proposed 2nd-harmonic extraction scheme (d).

impedance at $2f_0$ [7], aiding in generating a strong 2nd-harmonic voltage. The dual-core Class-F^{-1} VCO in [6] relies on a narrow common trace P_1P_2 [Fig. 2 (b)] to block the undesired mode at f_0. However, its large resistance also degrades the tank impedance and Q at $2f_0$. Instead, this work still maintains a wide trace P_1P_2 with small resistance and uses two resistors ($R_{rej}\approx4.2\Omega$) to block the undesired mode.

The 2nd-harmonic is extracted by the pickup coil constituted by two parallel S-shaped inductors. When excited by the fundamental signals at f_0 [Fig. 2 (d)], the induced voltages at the two traces (O_1P_3 and O_2P_4) in one S-shaped inductor cancel each other, preventing the fundamental voltages at the drain and gate nodes from leaking to the $2f_0$ output (V_{2nd}), and thereby eliminating the subharmonic spur at f_0. Considering the small asymmetry introduced by the underpass of the S-shaped inductor, the proposed $2f_0$ extraction scheme achieves a low subharmonic spur of −58dBc according to the simulation. In the reverse direction, the magnetic isolation between the pickup coil and the coil at the drain or gate node ensures that the capacitor (C_{2nd}) at the V_{2nd} node does not affect the tank's resonant frequency. Therefore, the variation of C_{2nd} induced by SSPD will not disturb f_0, minimizing the associated ref. spur. In contrast, the SSPLL in [8] inserts a ÷2 divider between the $2f_0$ output and SSPD, due to the insufficient magnetic isolation of the

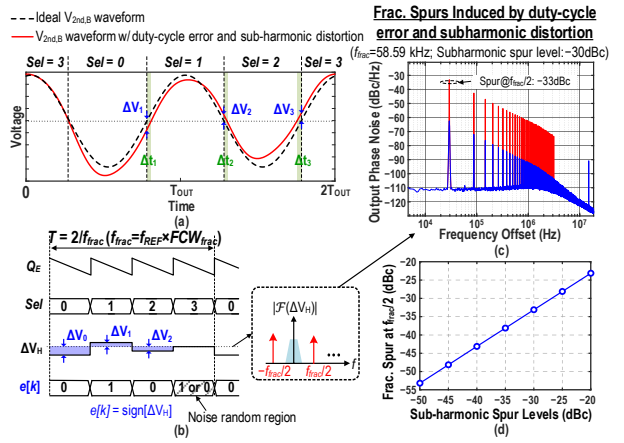


Fig. 3. The voltage offsets caused by the duty-cycle error and subharmonic (a). The principle of the duty-cycle error and subharmonic calibration (b). The impact of the duty-cycle error and subharmonic on phase noise (c) and frac. spurs (d).

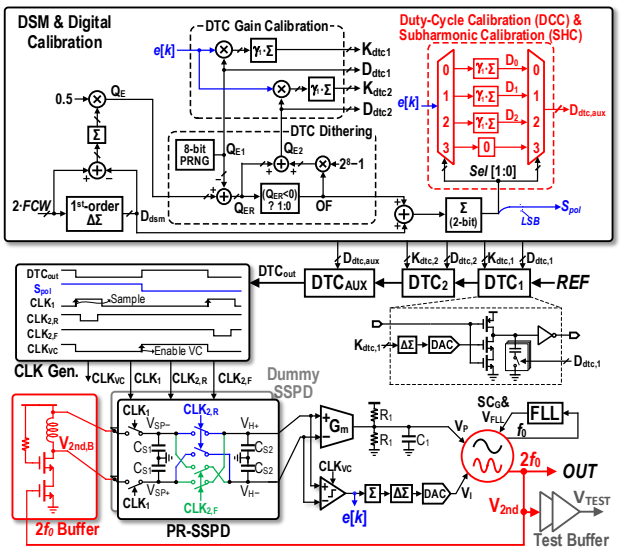
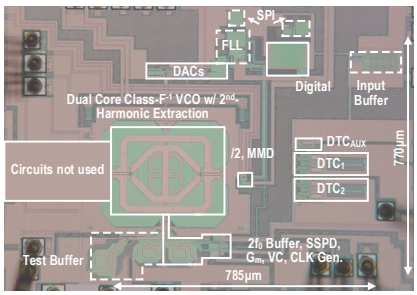


Fig. 4. Overall architecture of the proposed HSS-PLL, including the harmonic sampling path and schematics of the digital blocks.

existing 2nd-harmonic extraction scheme [9]. When excited by the 2nd-harmonic signals at $2f_0$ [Fig. 2 (c)], the induced voltages at O_1P_3 and O_2P_4 become in phase, generating a large V_{2nd} at $2f_0$. Connecting two S-shaped inductors in parallel helps boost the amplitude of V_{2nd}. The simulation shows that the amplitude of V_{2nd} reaches 0.66V at C_{2nd}=30fF.

B. Suppression of Fractional Spurs Induced by the Subharmonic Distortion

The DTC delays the sampling clock to the nearest zero-crossing point of $V_{2nd,B}$ during Q-error compensation. However, duty-cycle error and subharmonic distortion perturb the zero-crossing points of $V_{2nd,B}$, causing deterministic voltage offsets ($\Delta V_{1\text{-}3}$) at the output (V_H) of the PR-SSPD (Fig. 3). These offsets repeat at a period of $2/f_{frac}$, generating frac. spurs at $f_{frac}/2$ and its harmonic frequencies. Simulation shows that a subharmonic spur of −30dBc on $V_{2nd,B}$ induces a frac. spur of −33dBc at $f_{frac}/2$ offset. Also, the inband frac. spur increases linearly with the subharmonic spur. Although subharmonic spurs below −40dBc may satisfy typical wireless applications, the frac. spurs induced by subharmonic distortion of $V_{2nd,B}$ can severely degrade the



	Power (mW)	Area (mm^2)
VCO	28.2	0.08
$DTC_{1,2}$ + DTC_{AUX}	1.57	0.015
G_m + VC + CLK Gen. + DACs	0.63	0.0026
$2f_0$ Buffer	2.7	0.015
/2 + MMD	1.36	0.00037
Digital	3.15	0.01
Total	37.61	0.123

Fig. 5. Die micrograph of the proposed PLL with power consumption and area breakdown.

jitter especially when f_{frac} is small. To suppress these frac. spurs, an auxiliary DTC (DTC_{AUX}) with a 5ps range is exploited to eliminate $\Delta V_{1\text{-}3}$, as shown in Fig. 4. DTC_{AUX} is controlled by digital logic for duty-cycle calibration (DCC) and subharmonic calibration (SHC).

Fig. 4 also shows the overall architecture of the proposed HSS-PLL. A cascode buffer is inserted between the V_{2nd} and PR-SSPD to prevent loading the $2f_0$ output with the PR-SSPD that exhibits a low input impedance. The main DTC is realized by cascading two identical DTCs ($DTC_{1,2}$). Thanks to the reduced DTC range by sampling $2f_0$, only the gains of $DTC_{1,2}$ are calibrated. DTC dithering is added to ensure the convergence of all the calibrations at near-integer channels [3]. S_{pol} indicates the sampling occurs at the rising or falling edge of $V_{2nd,B}$, which controls the polarity of PR-SSPD.

III. Measurement Results

Fabricated in 28nm CMOS, the PLL occupies a compact area of 0.12mm^2 and consumes 37.6mW using a 120MHz ref. clock (Fig. 5). Fig. 6 shows the measured PN and spectra at a near-integer channel around 37.44GHz. When both DCC and SHC are off, the worst-case frac. spur and output jitter (including spurs) are −24.6dBc and 465.2fs, respectively. Enabling DCC only reduces frac. spur and output jitter to −26.8dBc and 291fs. Enabling both DCC and SHC further lowers frac. spur and output jitter to −49.2dBc and 63.6fs. Across different frac.-N channels where FCW_{frac} varies from 2^{-15} to 2^{-3}, enabling SHC improves the worst-case frac. spur and output jitter by >20dB and >76fs [Fig. 6 (c) and (d)]. The measured output jitter and ref. spur at the integer channel (37.44GHz) are 39.4fs and −71.0dBc (Fig. 7).

IV. Conclusion

This paper presents a 37.44GHz frac.-N PLL leveraging a harmonic subsampling (HSS) technique to achieve ultra-low jitter and ref. spur. Compared with prior mm-Wave frac.-N PLLs [Fig. 8 (a) and TABLE I], the proposed HSS-PLL demonstrates the advantage of achieving low jitter with compact area at the frequency band over 30GHz. Moreover, the HSS-PLL realizes the lowest jitter and ref. spur compared with prior mm-Wave PLLs operating in the integer-N mode [Fig. 8 (b)].

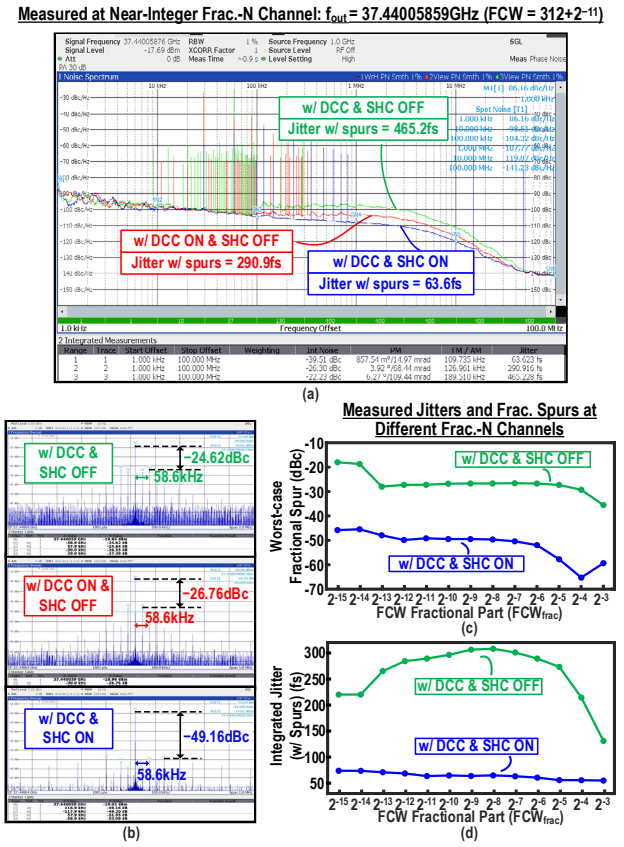


Fig. 6. Measured phase noise (a) and fractional spur (b) with DCC on/off and SHSC on/off at the same fractional-N channels near 37.44GHz. Measured jitter (c) and fractional spur (d) performance across different fractional-N channels near 37.44GHz.

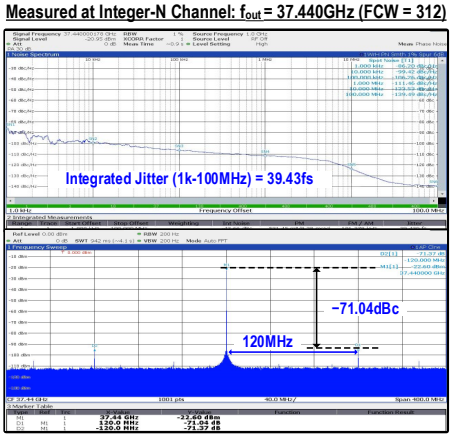


Fig. 7. Measured phase noise and spectra at integer-N channel (37.44GHz).

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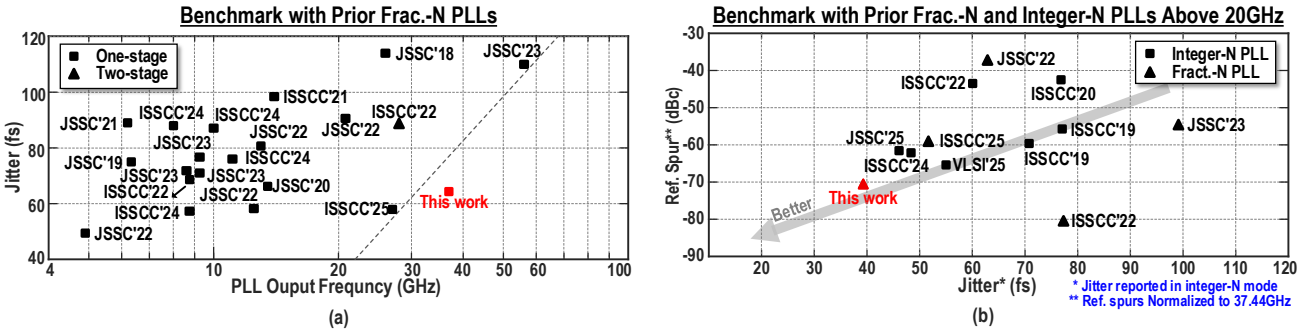

Fig. 8. Jitter at fractional-N mode comparison with prior fractional-N PLLs (a), reference spur and jitter at integer-N mode comparison with prior PLLs above 20GHz (b).

TABLE I. COMPARISON WITH STATE-OF-THE-ART PLLS

	This work	L. Grimaldi ISSCC'19	W. Tao JSSC'25	H. Li ISSCC'25	S. EK JSSC'18	S. Kalia JSSC'22	D. Yang ISSCC'22	H. Yoon ISSCC'18
Technology	28nm CMOS	65nm CMOS	22nm CMOS	28nm CMOS	28nm FD-SOI	22nm FD-SOI	7nm CMOS	65nm CMOS
PLL Architecture	HSS-PLL	SSBB-DPLL	CSS-ADPLL	SSPLL+PR-SSPD+DFLL	CPPLL	CPPLL	SPLL+Harm. Mixing-PLL	GHz-PLL +ILFMs
	One-stage						Two-stage	
Frequency Range(GHz)	**36.7 to 43.5**	30.6 to 34.2	21 to 25	23.2 to 27	23.3 to 30.2	18.1 to 21.2	25 to 28	25 to 30
Ref. Freq.(MHz)	120	100	250	120	491.52	2500	74	120
Frac-N Jitter w/o Spurs(fs)	**55.27**	N/A	N/A	54.7	160	N/A	N/A	N/A
Frac-N Jitter w/ Spurs(fs)	**63.62**	197.6	167.8	57.9	N/A	90.6	88	206
Integration Bandwidth(Hz)	1k to 100M	30k to 10M	10k to 40M	1k to 100M	20k to 500M	10k to 100M	10k to 40M	1k to 100M
[a]FoM$_J$(dB)	**-249.4**	N/A	N/A	-250.2	-244	N/A	N/A	N/A
[b]FoM$_S$(dB)	**-248.2**	-238.6	-244.1	-249.7	N/A	-246	-250	-238.1
Total Power(mW)	37.61	35	13.81	32.16	15.4	30.5	12.9	36.4
[c]Fractional Spur(dBc)	**-49.2**	-40.3	-43.9	-52.4	-26.8	-37.9	-58.5	N/A
[c]Ref. Spur(dBc)	**-71.04**	N/A	-56.1	-59.8	-61.9	N/A	-80.5	-80.8
Active Area(mm^2)	0.123	0.55	0.08	0.098	0.11	0.31	0.24	0.95

[a]FoM$_J$ =10*log$_{10}$[(Frac-N Jitter$_{w/o\ spurs}$/1s)2*(Power/1mW)] [b]FoM$_S$ =10*log$_{10}$[(Frac-N Jitter$_{w/\ spurs}$/1s)2*(Power/1mW)] [c]Normalized to 37.44GHz

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