Multi-Step Gate Dielectric Engineering for 2.5 kV-class GaN MIS-MBDS with 62 mV Low Hysteresis and Improved Interface Quality

Ningyu Luo[1,2], Huiqing Wen[1,2,*], Guohao Yu[3], Xiaodong Zhang[3], and Qiang Zha[3]

[1]School of Advanced Technology, Xi'an Jiaotong-Liverpool University, Suzhou 215123, China
[2]Department of Electrical Engineering and Electronics, University of Liverpool, L69 3GJ, UK
[2]Suzhou Institute of Nano-Tech and Nano-Bionics, Suzhou 215000, China
[*]Email: Huiqing.Wen@xjtlu.edu.cn

***Abstract*—Gallium nitride (GaN) metal-insulator-semiconductor (MIS) monolithic bidirectional switches (MBDS) hold significant potential for advanced power applications, yet their reliability is severely limited by threshold voltage instability induced by etch damage, interface mismatch, and oxide-related defects. This work proposes a multi-step gate dielectric engineering combining N_2 remote plasma pretreatment, an atomic layer deposited AlN interlayer, and O_2 remote plasma pretreatment, for better gate interface quality. The fabricated 2.5 kV-class GaN MIS-MBDS exhibit a low hysteresis of 62 mV, and an interface trap density of below $2.5 \times 10^{12} cm^{-2} eV^{-1}$ near the conduction band edge. Benefiting from the improved interface quality, PBTI characterizations verify good threshold voltage stability under gate bias stress, with shifts less than 0.3 V after 1000 s stress and below 0.75 V after 10000 s stress. This work demonstrates a reliable gate dielectric scheme suitable for high-voltage GaN MIS-MBDS applications with enhanced interface quality and improved threshold stability.**

***Index Terms*—GaN, monolithic bidirectional switches, gate dielectric engineering, interface traps, PBTI, trap dynamics, GaN MIS-HEMTs.**

I. Introduction

Gallium nitride (GaN) monolithic bidirectional switches (MBDSs), developed based on GaN HEMT platforms, have attracted intensive attention in power electronics owing to their wide bandgap, high power density and bidirectional control capability [1]. For reliable high-voltage operation, a recessed MIS gate stack is one of the common choices to achieve E-mode operation and low gate leakage [2], with Al_2O_3 being the current widely-adopted dielectric for its high permittivity and thermal stability [3]. Nevertheless, such a recessed Al_2O_3 MIS gate suffers from nitrogen vacancies introduced during gate recessing, interfacial mismatch between layers, and oxygen diffusion during Al_2O_3 deposition, leading to high interface trap density ($D_{\rm it}$) and degrade $V_{\rm th}$ stability. To mitigate these traps, various interface engineering approaches have been explored. For example, N_2 remote plasma pretreatment (RPP) was proven capable of fill nitrogen vacancies [4], while O_2 RPP was validated to modify surface chemistry to enhance Al_2O_3 nucleation [5]. However, these single-step treatments are inherently limited in achieving a synergistic combination of multiple interface engineering effects [6]. For instance, N_2 RPP alone offers limited improvement for interfacial mismatch compared to O_2 RPP, while O_2 RPP only partially passivates nitrogen vacancies without fully filling them [6], [7]. Moreover, neither of the above approaches addresses the oxygen diffusion during subsequent Al_2O_3 growth [8].

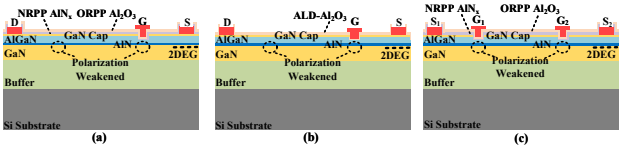

Fig. 1. Device architecture of (a) GDE-processed HEMT device, (b) reference HEMT device, (c) GDE-processed MBDSs.

In this work, we propose a synergistic multi-step gate dielectric engineering (GDE) that combines N_2 RPP, an AlN interlayer, and O_2 RPP prior to Al_2O_3 deposition, with each step targeting a specific trap origin. This approach yields a hysteresis below 100 mV, low $D_{\rm it}$, and sub-1 V $V_{\rm th}$ shift after 10000 s of PBTI stress. This work offers an effective gate engineering scheme for interface optimization and threshold stability improvement in recessed-gate GaN MIS-MBDS

II. Device Fabrication and Interface Engineering

A. Epitaxial Stack and Device Structure

To validate the proposed GDE scheme, demonstration devices were fabricated on a GaN-on-Si epitaxial wafer featuring a 1 nm GaN cap layer. The 2DEG channel forms at the GaN/AlN/$Al_{0.25}Ga_{0.75}N$ heterointerface, where the AlN and AlGaN thicknesses are 0.8 nm and 25 nm, respectively. To minimize etch damage during gate recess, atomic layer etching (ALE) was employed to precisely remove the GaN cap and 18 nm of AlGaN barrier, leaving a partially recessed gate trench. On this recessed surface, the proposed GDE and subsequent processes were applied to fabricate the MBDS and HEMT devices with structure shown in Fig. 1(a) and (c). Reference HEMT devices with a 25 nm thick Al_2O_3 deposited by atom later deposition (ALD) were also fabricated for comparison under otherwise identical conditions, as illustrated in Fig. 1(b).

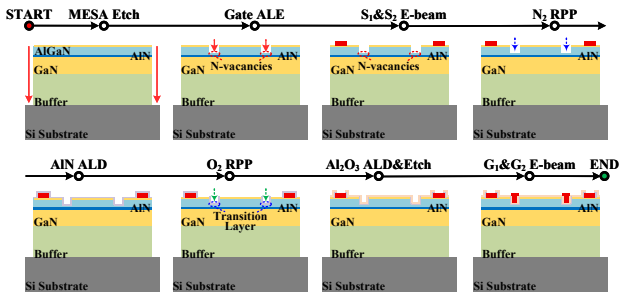

Fig. 2. Fabrication flow of GDE-processed devices.

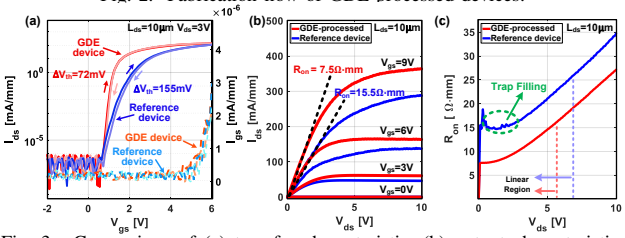

Fig. 3. Comparison of (a) transfer characteristic, (b) output characteristic, and (c) R_{on} of GDE-processed HEMT device and reference HEMT device.

B. Multi-Step Synergistic Gate Dielectric Engineering

To address the nitrogen vacancies, interfacial mismatch, and oxygen diffusion identified in the introduction, we propose a synergistic multi-step gate dielectric engineering scheme that targets each defect individually. The detailed integration sequence is summarized in Fig. 2 and described as follows:

- **N_2 RPP:** After gate recess and source metal deposition, N_2 RPP was conducted on the TMAH-cleaned AlGaN surface to fill nitrogen vacancies via highly reactive nitrogen radicals, establishing a stable starting surface for subsequent film growth [4], [9].
- **ALD-AlN Interlayer Growth:** Following the N_2 RPP, a 5-nm AlN layer is then deposited by thermal ALD, providing reduced lattice mismatch with AlGaN to suppress interface states and acting as an oxygen diffusion barrier to prevent Ga-O_x bond formation [3].
- **O_2 RPP:** Prior to Al_2O_3 deposition, O_2 RPP was applied on the AlN surface to create an Al-O-N initiation layer that reduces interlayer mismatch and improves Al_2O_3 nucleation uniformity [5].

Finally, a 20-nm Al_2O_3 film was deposited by ALD as the main gate dielectric, followed by Ti/TiN gate metal deposition by electron-beam (E-beam) evaporation and lift-off. All samples underwent identical post-metallization annealing.

III. Result and Discussion

Fabricated devices are characterized using KEYSIGHT B1500A and B1505A analyzers for dual-gate MBDSs and single-gate HEMTs.

A. Static Electrical Characteristics

Fig. 3(a) compares the transfer characteristics (I_{ds}-V_{gs}) of the GDE-processed and reference HEMT devices with dual-directional sweeps. The GDE-processed device exhibits E-mode operation with $V_{th} = 1.1$ V and reduced V_{th} hysteresis of 72 mV from 155 mV, indicating lower interface trap density.

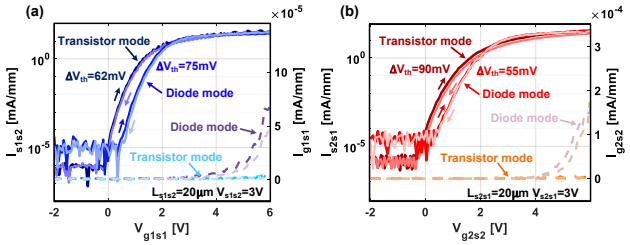

Fig. 4. Transfer characteristic of GDE-processed MBDS device in (a) forward and (b) backward direction.

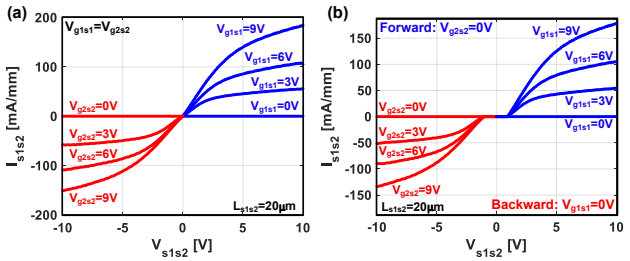

Fig. 5. (a) Bi-directional output characteristic, (b) gate signals of AC wave-chopping, and (c) S_1-S_2 voltage waveform during AC wave-chopping.

Fig. 3(b), (c) illustrate the output (I_{ds}-V_{ds}) characteristics and extracted R_{on}. The GDE-processed device achieves a higher saturation current of 366 mA/mm, and a lower R_{on} of 7.5Ω·mm, indicating improved channel transport. Notably, the reference device exhibits a prominent trap-filling process in Fig. 3(c), whereas the GDE-processed device shows smooth and stable R_{on} from the onset of the linear region. This evidences the effective passivation of interface traps by the N_2 RPP treatment.

Fig. 4(a), (b) illustrate the I_{ds}-V_{gs} characteristics of fabricated GDE-processed MBDS device in both direction. According to the figure, for the transistor mode ($V_{g1s1} = V_{g2s2}$) operation, the device exhibits a V_{th} of 1.1 V and an on/off current ratio exceeding 10^8 in both directions, confirming process uniformity. For the transfer characteristics measured in diode mode with one gate biased at 0 V, the on/off ratio degraded by one order of magnitude, accompanied by an increased V_{th}. The fabricated MBDS exhibits excellent symmetry in both diode mode and transistor mode. Additionally, it demonstrates a low hysteresis of 62 mV in transistor mode and 55 mV in diode mode, which indicates superior gate interface quality and high process uniformity. Fig. 5 presents the I_{ds}-V_{ds} characteristics of the fabricated GDE-processed MBDS in transistor and diode modes, with a saturation current exceeding 150 mA/mm in transistor mode. Fig. 5(b) reveals a ≈ 1.2 V turn-on voltage for both directions in the diode mode, indicating good symmetry as well.

B. Breakdown Characteristics

Fig. 6(a), (b) compares the gate breakdown ($V_{gs,break}$) and drain-to-source breakdown ($V_{ds,break}$) characteristics of the GDE-processed HEMTs and reference devices. As illustrated, the GDE-processed device exhibits an improved breakdown performance, achieving a gate breakdown voltage exceeding 17 V and a drain-to-source breakdown voltage surpassing

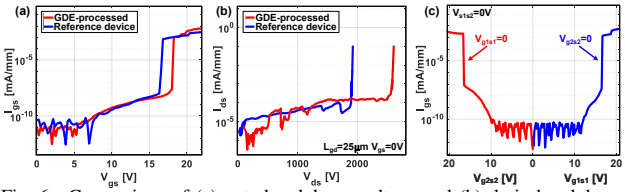

Fig. 6. Comparison of (a) gate breakdown voltage and (b) drain breakdown voltage between GDE-processed HEMT device and reference HEMT device.

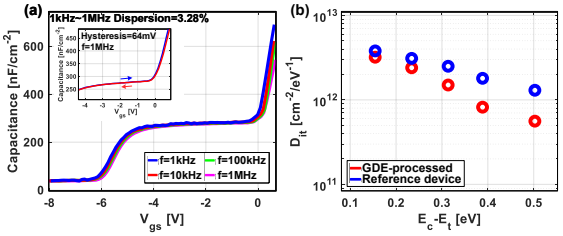

Fig. 7. (a) C-V characteristics of HEMT processed by proposed GDE and (b) comparison of $D_{\rm it}$ vs E_c-E_t between GDE-processed HEMT device and reference HEMT device.

2.5 kV, both of which are higher than those of the conventional counterpart. These evidence demonstrate the effectiveness of the proposed GDE process in enhancing the voltage blocking capability, enabled by the improved interface quality and suppressed trap-assisted dielectric breakdown (TADB).

Fig. 6(c) demonstrates the $V_{gs,break}$ characteristics for both gates. As the figure shows, both gates exhibit nearly identical gate breakdown characteristics, with the $V_{gs,break}$ of both gates exceeding 16 V, which is consistent with the HEMT results.

C. Interface Quality Characterization

To evaluate the interface quality achieved by the proposed GDE, capacitance-voltage (C-V) measurements were performed on both GDE-processed and reference devices. As shown in Fig. 7(a), the GDE-processed device exhibits an excellent frequency dispersion of 3.28% from 1 kHz to 1 MHz. Moreover, the GDE-processed device also exhibits a low C–V hysteresis of 64 mV under 1 MHz sweeping. The energy-dependent $D_{\rm it}$ as a function of $E_c - E_t$ was then extracted from C-V and G-V data using the conductance method. Fig. 7(b) compares $D_{\rm it}$ of the GDE-processed device and reference device. For the GDE-processed device, $D_{\rm it}$ is below 2.5×10^{12} cm^{-2}eV^{-1} near the conduction band edge and decreases to less than 6×10^{11} cm^{-2}eV^{-1} at $E_c - E_t \approx 0.51$ eV. This energy-dependent reduction arises from the synergistic multi-step interface engineering: N_2 RPP fills nitrogen vacancies to suppress shallow-level traps; the AlN interlayer blocks oxygen diffusion to reduce deeper-level $D_{\rm it}$; and O_2 RPP improves Al_2O_3 nucleation uniformity, mitigating interface roughness and mismatch. In contrast, the reference device shows higher $D_{\rm it}$ across all energies, especially at deeper levels. This indicates the GDE process is particularly effective at suppressing deeper-level traps, likely by preventing oxygen-related defects, resulting in a much larger $D_{\rm it}$ difference at deeper energy levels.

To further probe trap characteristics, positive bias temperature instability (PBTI) measurements were performed under

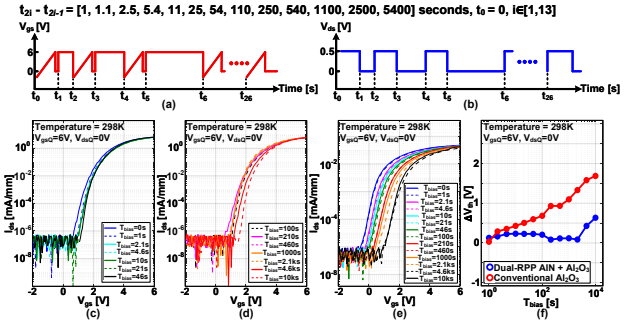

Fig. 8. (a)-(b) V_{gs}/V_{ds} time sequences during PBTI. (c)-(e) Transfer curve evolutions for GDE-processed and reference HEMTs under varied stress durations. (f) Comparison of V_{th} shifts for both devices after PBTI stress.

$V_{\rm gs,stress} = +6$ V at 298 K, with its stress timing sequence shown in Fig. 8(a). The comparison of ΔV_{th} evolution of two devices after 0 s to 10000 s stress time is shown in Fig .8(b)-(f). As the figure shows, the GDE-processed device exhibits lower V_{th} drift through almost all stress history, with ΔV_{th} less than 0.3 V after 1000 s stress and 0.75 V after 10000 s, demonstrating improved long-term stability.

In contrast to the monolithic increase observed from the reference device during PBTI stress, the GDE device shows a non-monotonic $\Delta V_{\rm th}$ evolution during PBTI stress that can be understood based on sequential trapping and detrapping processes. The rapid initial rise of $\Delta V_{\rm th}$ to about 0.4 V within 0-2 s can be attributed to the fast filling of shallow interface traps. The subsequent plateau from 2–100 s may arise from the saturation of shallow interface trap filling. Between 100 s and 210 s, $\Delta V_{\rm th}$ gradually decreases to below 0.3 V, with a subsequent plateau extending from 210 s to 2100 s. This behavior may be explained by slow electron detrapping from near-band shallow traps. At stress times beyond 2100 s, $\Delta V_{\rm th}$ resumes a gradual increase with a similar slope to that of the reference device. Given that both devices share identical Al_2O_3 deposition conditions and differ only in the GDE process applied near the gate interfaces, this late-stage increase can be attributed to slow charging of bulk traps inherent to the Al_2O_3 layer. This evolution is consistent with the effectively suppressed near-interface trapping achieved by the proposed GDE scheme.

D. Practical AC Operation and Performance Benchmark

In order to verify the actual functionality of the GDE-processed MBDS in a real power circuit, an AC regulating test was conducted. Fig. 9(a) shows the circuit setup of AC regulating experiment for this study. The AC wave-chopping operation is demonstrated at a gate switching frequency of 100 kHz with a 10 kHz sinusoidal AC signal, shown in Fig. 9(b), (c), confirming clean switching functionality.

To contextualize the performance of the proposed gate dielectric engineering, the fabricated HEMT is benchmarked against state-of-the-art GaN MIS-HEMTs from other literature [2], [3], [10]–[22]. As shown in Fig. 10(a), the device achieves a superior combination of high $V_{\rm th}$ and low hysteresis. Meanwhile, as Fig, 10(b) shows, although the $R_{\rm on}$ is not the lowest among the benchmarks, it remains at a competitive level,

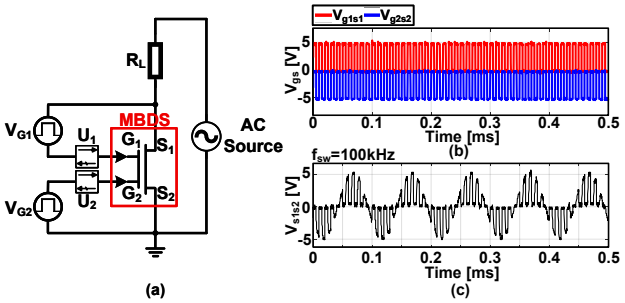

Fig. 9. (a) AC regulating test circuit, (b) gate signals of AC wave-chopping, and (c) S_1-S_2 voltage waveform during AC wave-chopping.

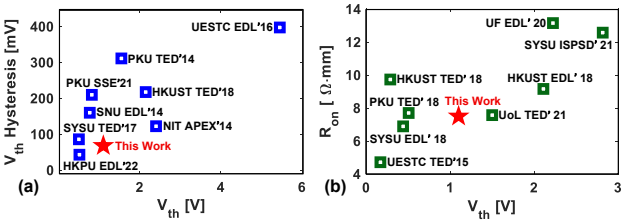

Fig. 10. Comparison of performance between HEMT processed with proposed GDE and benchmarks on (a) hysteresis vs V_{th} and (b) ΔV_{th} vs T_{bias} at 298K temperature.

underscoring the effectiveness of proposed GDE in enhancing interface quality.

IV. Conclusion

This work presents a multi-step gate dielectric engineering process for GaN MIS-MBDSs and MIS-HEMTs, combining N_2 RPP, an ALD-AlN interlayer, and O_2 RPP prior to Al_2O_3 deposition. The GDE-processed devices achieve a low V_{th} hysteresis of 62 mV, a low D_{it} of $< 2.5 \times 10^{12}$ $\text{cm}^{-2}\text{eV}^{-1}$ near the conduction band, and a breakdown voltage exceeding 2.5 kV. In addition, the GDE-processed devices also exhibit a low V_{th} shift in PBTI tests, with $\Delta V_{th} < 0.3$ V at 1000, and $\Delta V_{th} < 0.75$ V at 10000 s. Importantly, GDE-processed MBDSs show good symmetric characteristics and AC regulating functionality. Overall, this work provides a high-performance device platform for GaN MIS-MBDS and GaN-HEMT devices.

V. Acknowledgment

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